57413A

Advanced Micro Devices

Military First-In First-Out (FIFO) 64x5 Memory 25MHz (Standalone)

Conforms to Mil-Std-883, Class B*

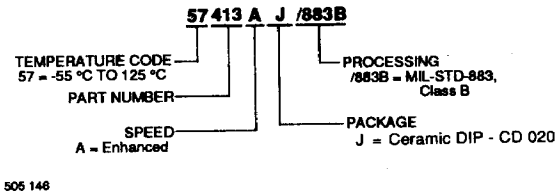
DISTINCTIVE CHARACTERISTICS

- **High-speed 25 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-Full and Almost-Full/Empty status flags**
- **Structured pinouts, Output pins directly opposite corresponding input pins**
- **Asynchronous operation**
- **TTL-compatible Inputs and Outputs**
- **Dose rate (transient upset) junction-isolated bipolar process $2x10^{10}$ RADs (Si)/s recovery time of 50 to 70 µs from 1 µs pulse**
- **Neutron fluence (permanent damage): $1x10^{13}$ N/cm2**

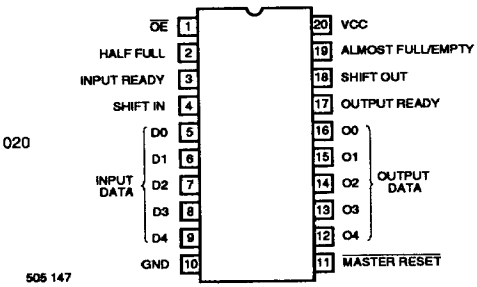
GENERAL DESCRIPTION

The 57413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at a 25 MHz input/output rate. The data is loaded and emptied on first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 12 mA) data outputs. This device can be connected in parallel to give FIFOs of any word length. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of the 57413A are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

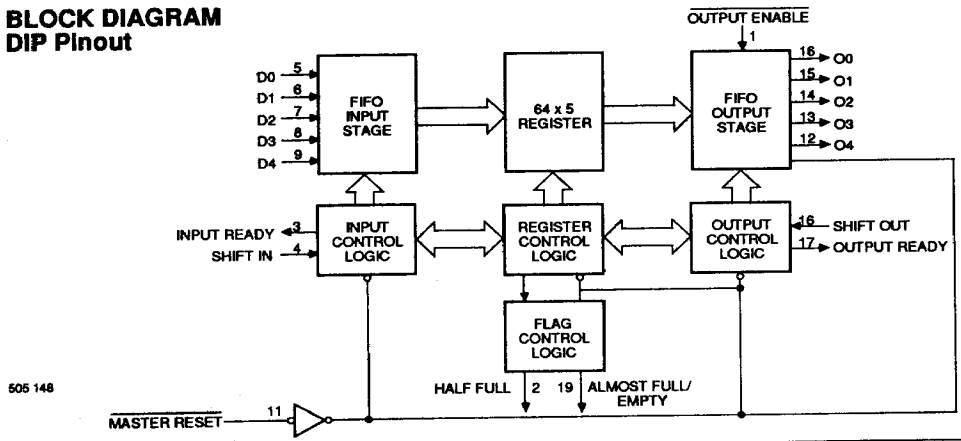
ORDERING INFORMATION



PIN CONFIGURATION



BLOCK DIAGRAM DIP Pinout



Publication # 11818 | Rev. A | Amendment /0
Issue Date: January 1989

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage range ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability. Absolute maximum ratings are for system design reference; parameters given are not tested.

Operating Conditions

Symbol	Parameter	Figure	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
t_{SIH}†	Shift in HIGH time	1	16		ns
t_{SIL}†	Shift in LOW time	1	20		ns
t_{IDS}	Input data setup time	1	2		ns
t_{IDH}	Input data hold time	1	25		ns
f_{IN}	Shift in rate	1	DC	25	MHz
f_{OUT}	Shift Out rate	4	DC	25	MHz
t_{SOH}†	Shift out HIGH time	4	10		ns
t_{SOL}	Shift out LOW time	4	27		ns
t_{MRW}	Master Reset pulse	8	35		ns
t_{MRS}**	Master Reset to SI	8	35		ns
V_{IL}*	Low level input voltage			0.8	V
V_{IH}*	High level input voltage		2.0		V
T_A***	Operating temperature		–55	125	°C

* V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

† See AC test and high speed application note.

*** Instant–On Case temperature.

505022

DC Characteristics Over Operating Conditions Conforms to MIL-STD-883; Group A, Subgroups 1, 2, & 3.

Symbol	Parameter	Test Conditions			Min	Max	Unit
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18 mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V			–250	µA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			50	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	12 mA		0.5	V
			I_{OL} (IR, OR)	8 mA†			
			I_{OL} (Flag outputs)	8 mA			
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	–3.0 mA	2.4		V
			I_{OH} (IR, OR)	–0.9 mA			
			I_{OH} (Flag outputs)	–0.9 mA			
I_{OS}*	Output short-circuit current	V_{CC} = MAX	V_O = 0 V		–20	–90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			20	µA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V			–20	µA
I_{CC}**	Supply current	V_{CC} = MAX, inputs low, outputs open				240	mA

* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
** See curve for I_{CC} vs. temp.
† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Switching Characteristics Over Operating Conditions Conforms to MIL-STD-883; Group A, Subgroups 9, 10, 11.

Symbol	Parameter	Figure	Min	Max	Unit
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		25	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	4		25	ns
t_{ODH}†	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		40	ns
t_{PT}	Data throughput or "fall through"	3, 6		750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	8		30	ns
t_{MRIRL}*	Master Reset ↓ Input Ready LOW	8		30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	8		55	ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.

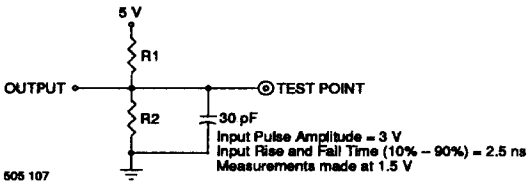
Switching Characteristics Over Operating Conditions (Cont.)

Symbol	Parameter	Figure	Min	Max	Unit
t_{IPH}	Input ready pulse HIGH	3	5		ns
t_{OPH}	Output ready pulse HIGH	6	5		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	4		20	ns
t_{AEH}*	Shift Out ↑ AF/E HIGH	9		145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	9		650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	10		650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	10		145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	11		380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	11		380	ns
t_{PHZ}**	Ouput Disable Delay	A		30	ns
t_{PLZ}**		A		30	ns
t_{PZL}	Output Enable Delay	A		30	ns
t_{PZH}		A		50	ns

Note: Input rise and fall time (10%–90%) = 2.5 ns.
* See timing diagram for explanation of parameters.
** Actual test limits mabe be different to compensate for ATE.

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, & 11.

Standard Test Load



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I_{OL}	R1	R2
12 mA	390 Ω	760 Ω
8 mA	600 Ω	1200 Ω

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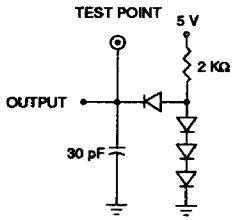
Design Test Load



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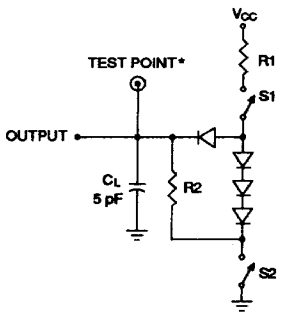
Three State Test Load*



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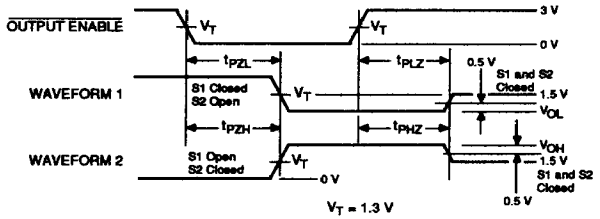
* Equivalent test loads may be used for automatic testing



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

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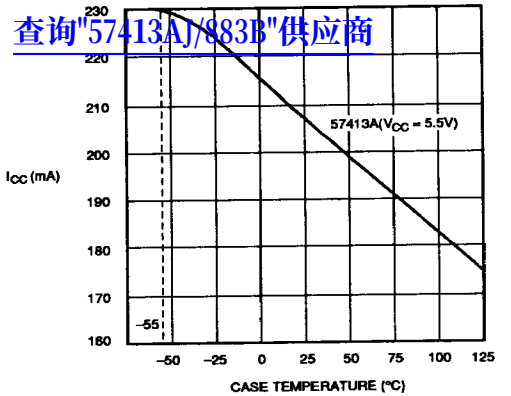
Figure A. Enable and Disable

Typical I_{CC} vs Temperature (V_{CC} = MAX)



505 151

Military Case Outlines

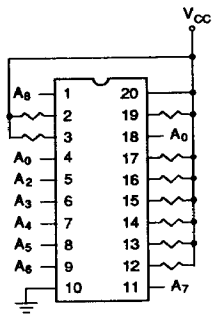
PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510F APPENDIX C CASE
J	D-8

505025B

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

Dynamic Burn-In Circuitry



505 152

$T_{ambient}$ = 125°C
V_{CC} = 5.25 ± 0.25 V
Square wave pulses on A_0 to A_8 are:

1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceding input, with A_0 beginning at 100 kHZ.
   e.g., A_0 = 100 kHz
   A_1 = 50 kHz ± 10%
   A_2 = 25 kHz ± 10%
   A_n = 1/2 A_{n-1} ± 10%

FUNCTIONAL DESCRIPTION

Data Input

After power up the Master Reset is pulsed low (Figure 8) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from D_x inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out), t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not high due to (a) too high a frequency, or (b) FIFO being full or effected by the Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{DRL}, and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

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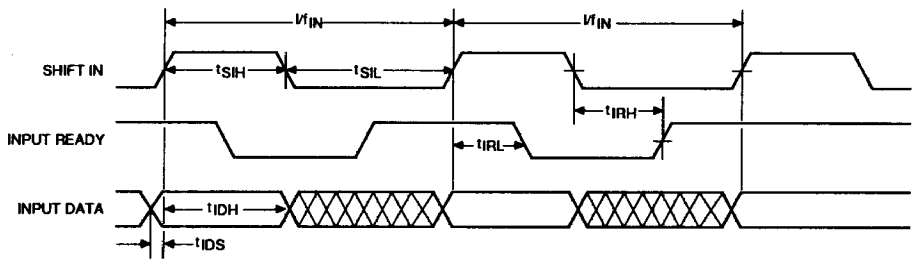

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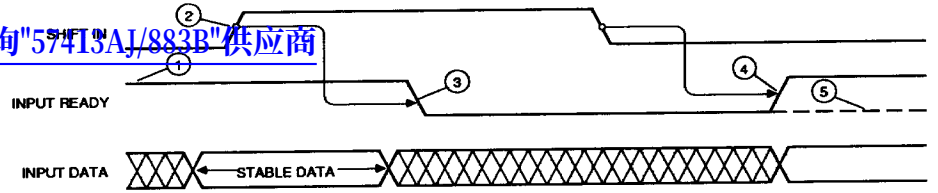
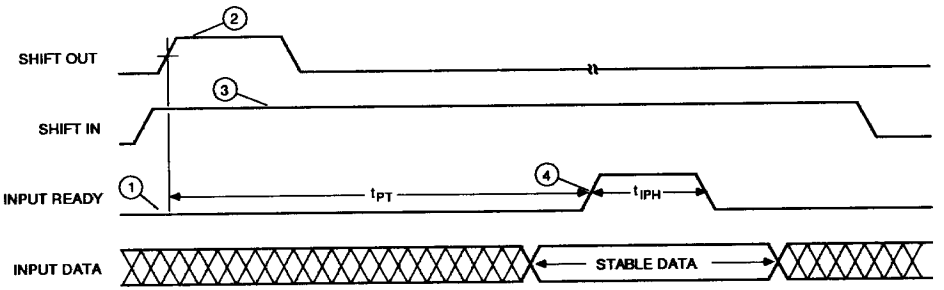
Figure 1. Input Timing



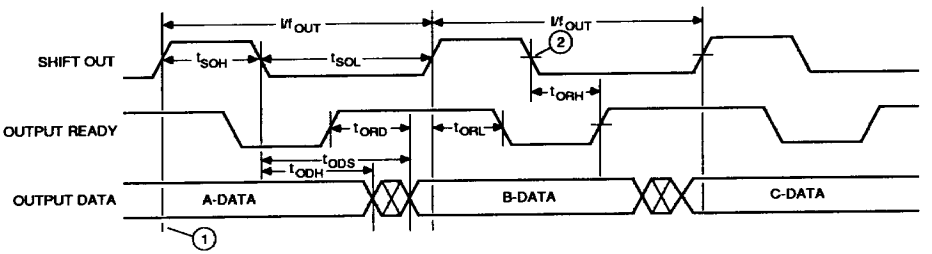
① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first word. The Data from the first word is released for "fall through" to second word.
③ Input Ready goes LOW indicating the first word is full.
④ Shift-In going LOW allows Input Ready to sense the status of the first word. The first word is now empty as indicated by Input Ready HIGH.
⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

Figure 2. The Mechanism of Shifting Data Into the FIFO 505 173



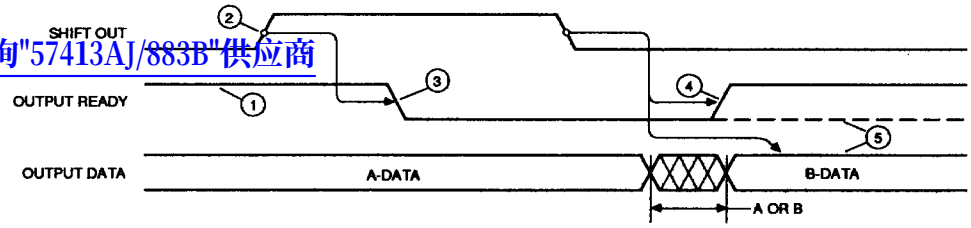
① FIFO is initially full.
② Shift-Out pulse is applied. An empty location starts "bubbling" to the front.
③ Shift-In is held HIGH.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH 505 155



① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, I.e., OR and SO ar both high together.

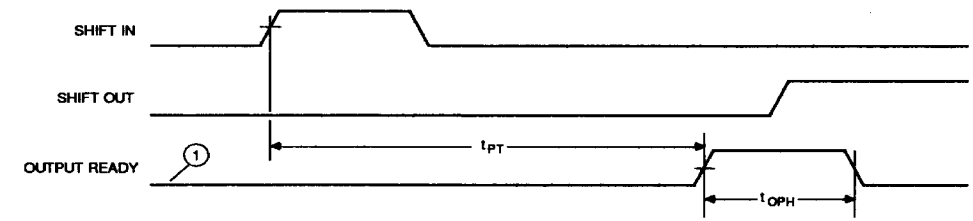
Figure 4. Output Timing 505 156



① Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing the contents of word 62 (B-DATA) to be released for fall through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data become invalid. Note: Shift-Out pulses applied when Output Ready is LOW will be ignored (See Figure 7).

505 157

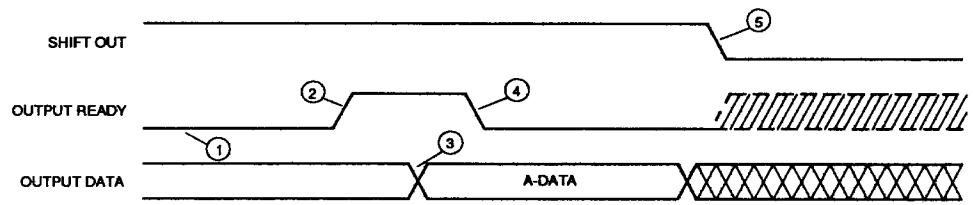
Figure 5. The Mechanism of Shifting Data Into the FIFO



① FIFO is Initially empty

505 158

Figure 6. t_{PT} and t_{OPH} Specification



① Word 63 is empty.
② Output Ready goes HIGH indicating arrival of the new data.
③ New data (A) arruves at the outputs (word 63).
④ Since Shift-Out is held HIGH, Output Data is subject to change. Output Ready will go HIGH or LOW.
⑤ As soon as Shift-Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or Low depending on whether there are any additional upsteam words in the FIFO.

505 159

Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH

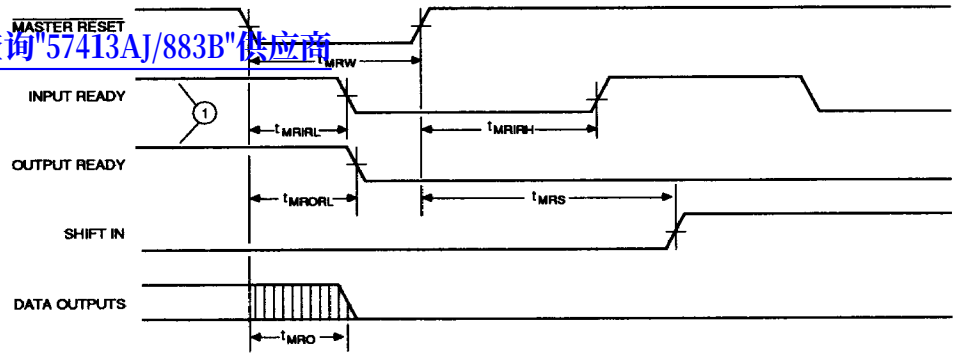
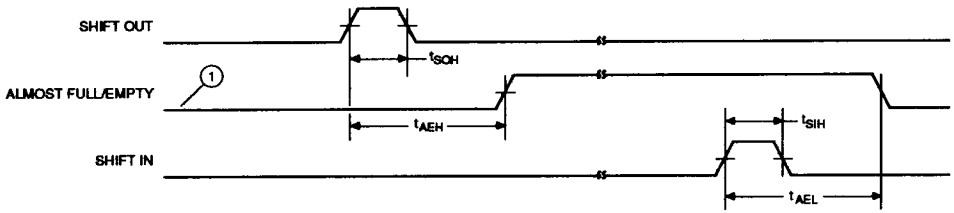
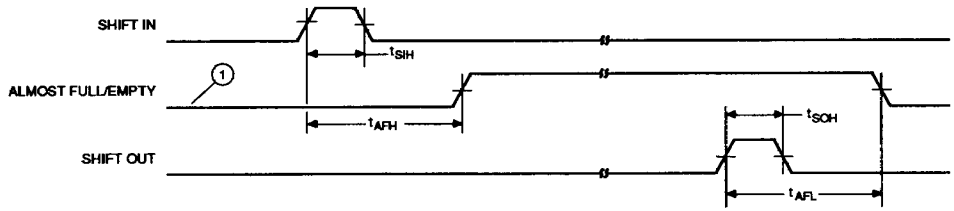


Figure 8. Master Reset Timing 505 160



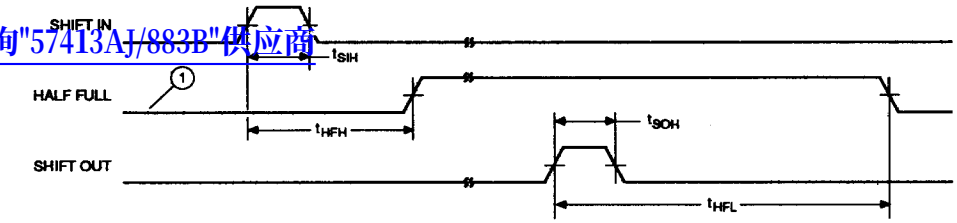
① FIFO contains 9 words (one more than almost empty).

Figure 9. t_{AEH}, t_{AEL} Specifications 505 161



① FIFO contains 55 words (one short of almost full).

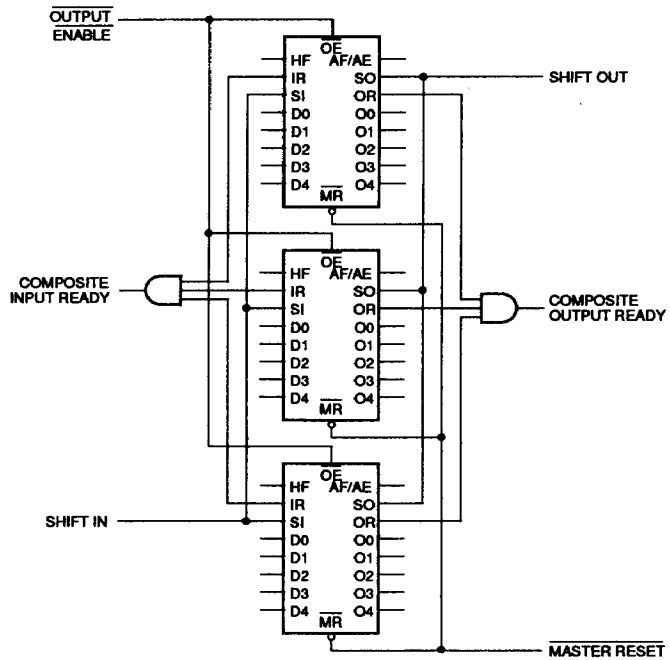
Figure 10. t_{AFH}, t_{AFL} Specifications 505 162



① FIFO contains 31 words (one short of half full).

505 163

Figure 11. t_{HFL}, t_{HFH} Specifications

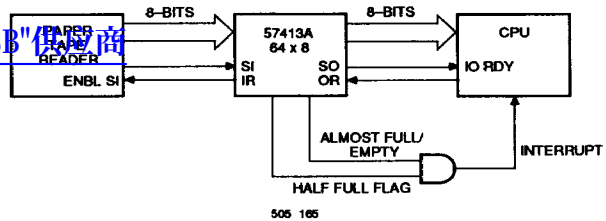


505 164

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite input and Output and Output Ready Flags. This requirement is due to the different fall through times of the FIFOs.

505 184

Figure 12. 64 x 15 FIFO with 57413A



Note: Expanding the FIFOs in word width is done by ANDing the IR and OR a shown in Figure 12.

Figure 13. Application for the 57413A "Slow and Steady Rate to Flat 'Blocked Rate' " 505 165