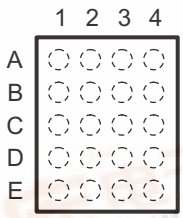
MMC, SD CARD, Memory Stick™ VOLTAGE-TRANSLATION TRANSCEIVER AND LDO VOLTAGE REGULATOR WITH ESD PROTECTION AND EMI FILTERING

FEATURES

- **Level Translator**
  - **V_{CCA} Range of 1.1 V to 3.6 V**
  - **Fast Propagation Delay (4 ns Max When Translating Between 1.8 V and 2.9 V)**
- **Low-Dropout (LDO) Regulator**
  - **200-mA LDO Regulator With Enable**
  - **2.9-V Output Voltage**
  - **3.05-V to 5.5-V Input Voltage Range**
  - **Very Low Dropout: 200 mV at 200 mA**
- **ESD Protection Exceeds JESD 22 (A Port)**
  - **2000-V Human-Body Model (A114-B)**
  - **1000-V Charged-Device Model (C101)**
- **±8-kV Contact Discharge IEC 61000-4-2 ESD (B Port)**

YFP PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4
A	DAT2A	V_{CCA}	WP/CD	DAT2B
B	DAT3A	V_{BATT}	V_{CCB} O/P	DAT3B
C	CMDA	GND	GND	CMDB
D	DAT0A	CLKA	CLKB	DAT0B
E	DAT1A	CLK-f	EN	DAT1B

DESCRIPTION/ORDERING INFORMATION

The TXS0206-29 is a complete solution for interfacing microprocessors with MultiMediaCards (MMCs), secure digital (SD) cards, and Memory Stick™ cards. It is comprised of a high-speed level translator, a low-dropout (LDO) voltage regulator, IEC level ESD protection, and EMI filtering circuitry.

The voltage-level translator has two supply voltage pins. V_{CCA} can be operated over the full range of 1.1 V to 3.6 V. V_{CCB} is set at 2.9 V and is supplied by an internal LDO. The integrated LDO accepts input voltages from 3.05V to as high as 5.5 V and outputs 2.9 V, 200 mA to the B-side circuitry and to the external memory card. The TXS0206-29 enables system designers to easily interface low-voltage microprocessors to memory cards operating at 2.9 V.

Memory card standards recommend high-ESD protection for devices that connect directly to the external memory card. To meet this need, the TXS0206-29 incorporates ±8-kV Contact Discharge protection on the card side.

Since memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the TXS0206-29 an ideal choice for these applications. The TXS0206-29 is offered in a 20-bump wafer chip scale package (WCSP). This package has dimensions of 1.96 mm × 1.56 mm, with a 0.4-mm ball pitch for effective board-space savings

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	WCSP – YFP (Pb-free)	Tape and reel	TXS0206-29YFPR	_ _ _ 3 V 2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The actual top-side marking has three preceding characters to denote year, month, and sequence code.

REFERENCE DESIGN

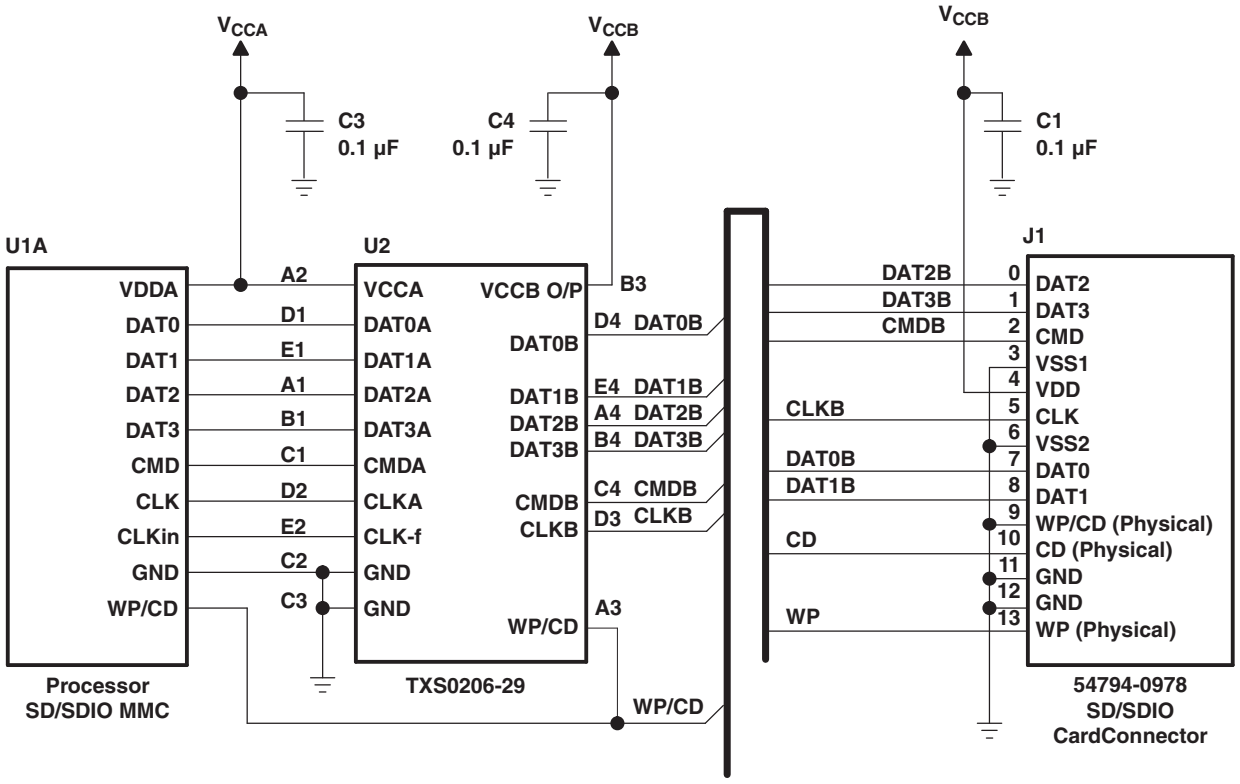


Figure 1. Interfacing With SD/SDIO Card

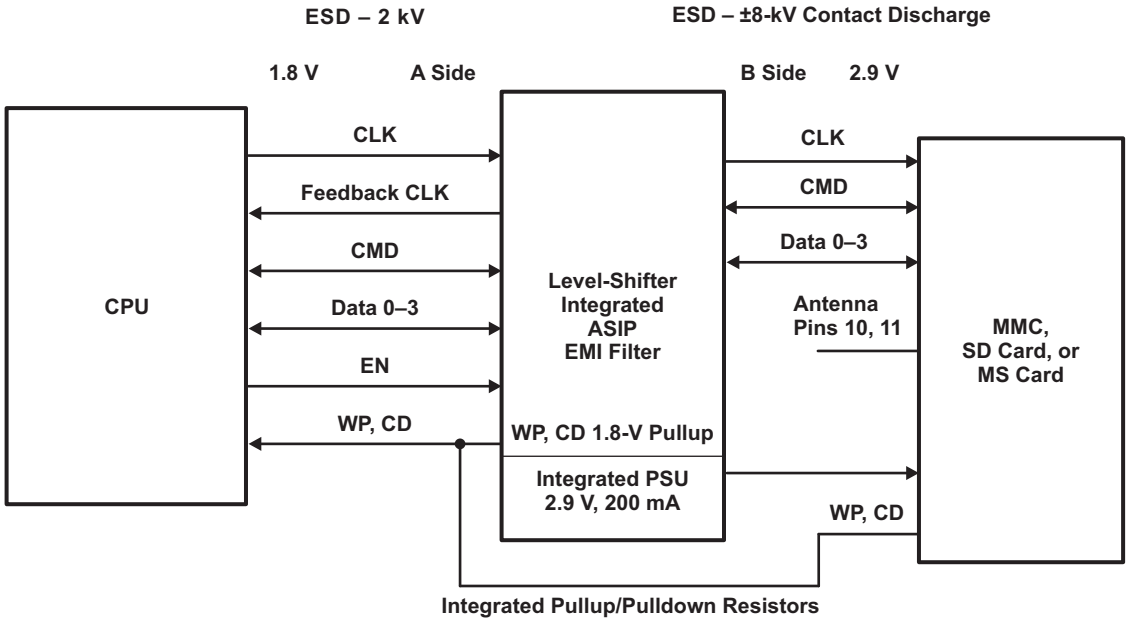


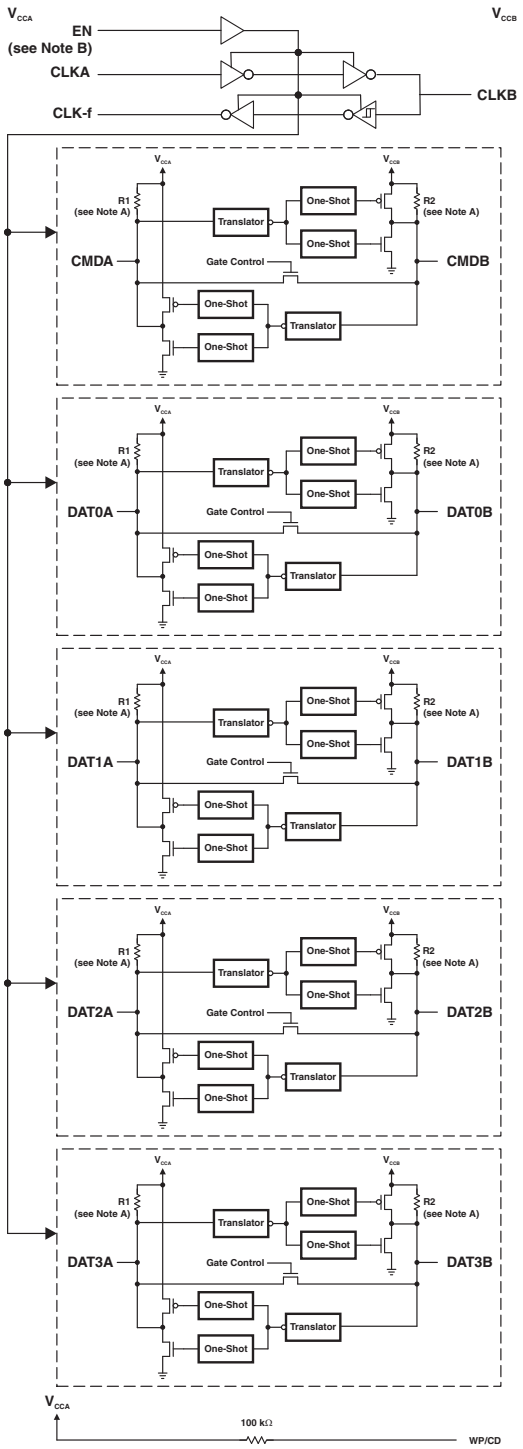
Figure 2. Typical Application Circuit

Table 1. LOGIC TABLE

EN	LDO	TRANSLATOR I/Os
L	Disabled	Disabled, pulled to V_{CCA}, V_{CCB} O/P through R_1 and R_2 at 70kΩ pullup resistors respectively
H	Active	Active

TERMINAL FUNCTIONS

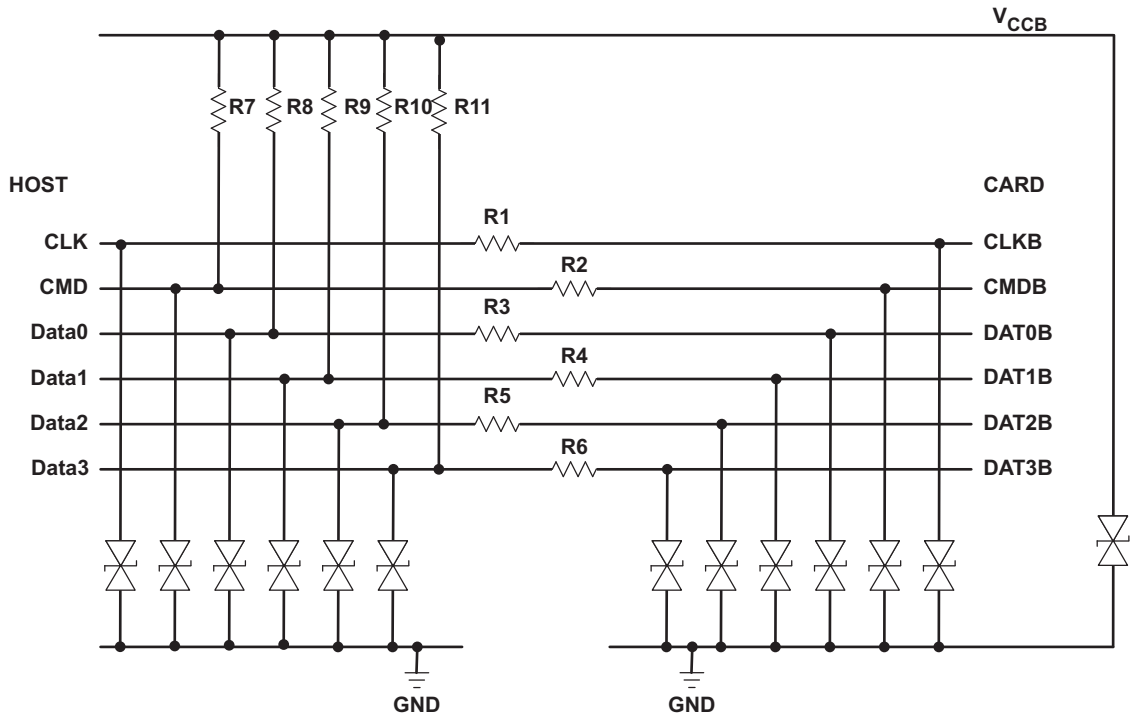
TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
A1	DAT2A	I/O	Data bit 2 connected to host. Referenced to V_{CCA}. Includes R_1 pullup resistor to V_{CCA} (see Note A).
A2	V_{CCA}	Power	A-port supply voltage. V_{CCA} powers all A-port I/Os and control inputs.
A3	WP/CD	Output	Connected to write protect on the mechanical connector. The WP pin has an internal 100-kΩ pullup resistor to V_{CCA}.
A4	DAT2B	I/O	Data bit 2 connected to memory card. Referenced to V_{CCB}O/P. Includes R_2 pullup resistor to V_{CCB}O/P (see Note A).
B1	DAT3A	I/O	Data bit 3 connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
B2	V_{BATT}	Input	LDO input voltage from Battery-Supply
B3	V_{CCB} O/P	Output	LDO output voltage and B-port supply voltage. V_{CCB}O/P powers all B-port I/Os.
B4	DAT3B	I/O	Data bit 3 connected to memory card. Referenced to V_{CCB}O/P. Includes R_2 pullup resistor to V_{CCB}O/P (see Note A).
C1	CMDA	I/O	Command bit connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
C2, C3	GND		Ground
C4	CMDB	I/O	Command bit connected to memory card. Referenced to V_{CCB}O/P. Includes R_2 pullup resistor to V_{CCB}O/P (see Note A).
D1	DAT0A	I/O	Data bit 0 connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
D2	CLKA	Input	Clock signal connected to host. Referenced to V_{CCA}.
D3	CLKB	Output	Clock signal connected to memory card. Referenced to V_{CCB}O/P.
D4	DAT0B	I/O	Data bit 0 connected to memory card. Referenced to V_{CCB}O/P. Includes R_2 pullup resistor to V_{CCB}O/P (see Note A).
E1	DAT1A	I/O	Data bit 1 connected to host. Referenced to V_{CCA} . Includes R_1 pullup resistor to V_{CCA} (see Note A).
E2	CLK-f	Output	Clock feedback to host for resynchronizing data to a processor. Leave unconnected if not used.
E3	EN	Input	Enable/disable control. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to V_{CCA}.
E4	DAT1B	I/O	Data bit 1 connected to memory card. Referenced to V_{CCB}O/P. Includes R_2 pullup resistor to V_{CCB}O/P (see Note A).



A. R_1 and R_2 resistor values are determined based upon the logic level applied to the A port or B port as follows:
R_1 and R_2 = 40 kΩ when a logic level low is applied to the A port or B port.
R_1 and R_2 = 4 kΩ when a logic level high is applied to the A port or B port.
R_1 and R_2 = 70 kΩ when the port is deselected (or in High-Z or 3-state).

B. EN controls all output buffers. When EN = low, all outputs are Hi-Z.

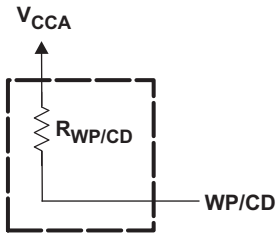
Figure 3. Logic Diagram



RESISTORS	
R1, R2, R3, R4, R5, R6	40 Ω
Tolerance	±20%
R7, R8, R9, R10, R11	40 kΩ
Tolerance	±30%

BIDIRECTIONAL ZENER DIODES	
Vbr min	14 V at 1 mA
Line capacitance	<20 pF

Figure 4. ASIP Block Diagram



RESISTORS	
$R_{WP/CD}$	100 kΩ
Tolerance	±30%

Figure 5. WP/CD Pullup Resistor

ABSOLUTE MAXIMUM RATINGS(1)
Level Translator

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL IMPEDANCE RATINGS

		TYP	UNIT
θ_{JA}	Package thermal impedance(1)	117	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ABSOLUTE MAXIMUM RATINGS(1)
LDO

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.3	6.5	V
V_{OUT}	Output voltage range	–0.3	4.6	V
	Peak output current		220	mA
	Continuous total power dissipation		TBD	mW
T_J	Junction temperature range	–55	150	°C
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1)
Level Translator

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	A-Port CMD and DATA I/Os	1.1 V to 1.95 V	2.9 V	V_{CCI} – 0.2	V_{CCI}	V
			1.95 V to 3.6 V		V_{CCI} – 0.4	V_{CCI}	
		B-Port and DATA I/Os	1.1 V to 1.95 V	2.9 V	V_{CCI} – 0.2	V_{CCI}	
			1.95 V to 3.6 V		V_{CCI} – 0.4	V_{CCI}	
		OE and CLKA	1.1 V to 3.6 V		V_{CCI} × 0.65	V_{CCI}	
V_{IL}	Low-level input voltage	A-Port CMD and DATA I/Os	1.1 V to 1.95 V	2.9 V	0	0.15	V
			1.95 V to 3.6 V		0	0.15	
		B-Port CMD and DATA I/Os	1.1 V to 1.95 V	2.9 V	0	0.15	
			1.95 V to 3.6 V		0	0.15	
		OE and CLKA	1.1 V to 3.6 V		0	V_{CCI} × 0.35	
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state					
I_{OH}	High-level output current (CLK-f output)		1.1 V to 1.3 V	2.9 V		–0.5	mA
			1.4 V to 1.6 V			–1	
			1.65 V to 1.95 V			–2	
			2.3 V to 2.7 V			–4	
			3 V to 3.6 V			–8	
I_{OL}	Low-level output current (CLK-f output)		1.1 V to 1.3 V	2.9 V		0.5	mA
			1.4 V to 1.6 V			1	
			1.65 V to 1.95 V			2	
			2.3 V to 2.7 V			4	
			3 V to 3.6 V			8	
I_{OH}	High-level output current (CLK output)			2.9 V		–8	mA
I_{OL}	Low-level output current (CLK output)			2.9 V		8	mA
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

RECOMMENDED OPERATING CONDITIONS
LDO

		MIN	MAX	UNIT
$I_{OUT(PK)}$	Peak output current	200		mA
C_{OUT}	Output capacitance	1	100	µF
T_J	Operating junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS
Level Translator

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}O/P	MIN	TYP(1)	MAX	UNIT
V_{OH}	A port (CLK-f output)	I_{OH} = –100 µA	1.1 V to 3.6 V	2.9 V	V_{CCA} × 0.8			V
		I_{OH} = –0.5 mA	1.1 V		0.8			
		I_{OH} = –1 mA	1.4 V		1.05			
		I_{OH} = –2 mA	1.65 V		1.2			
		I_{OH} = –4 mA	2.3 V		1.75			
		I_{OH} = –8 mA	3 V		2.3			
	A port (DAT and CMD outputs)	I_{OH} = –20 µA	1.1 V to 3.6 V		V_{CCA} × 0.8			
V_{OL}	A port (CLK-f output)	I_{OL} = 100 µA	1.1 V to 3.6 V	2.9 V			V_{CCA} × 0.8	V
		I_{OL} = 0.5 mA	1.1 V				0.35	
		I_{OL} = 1 mA	1.4 V				0.35	
		I_{OL} = 2 mA	1.65 V				0.45	
		I_{OL} = 4 mA	2.3 V				0.55	
		I_{OL} = 8 mA	3 V				0.7	
	A port (DAT and CMD outputs)	I_{OL} = 135 µA	1.1 V to 3.6 V	2.9 V			0.4	V
		I_{OL} = 180 µA					0.4	
		I_{OL} = 220 µA					0.4	
		I_{OL} = 300 µA					0.4	
		I_{OL} = 400 µA					0.55	
V_{OH}	B port (CLK output)	I_{OH} = –100 µA	1.1 V to 3.6 V	2.9 V	V_{CCB}O/P × 0.8			V
		I_{OH} = –8 mA			2.3			
	B port (DAT output)	I_{OH} = –20 µA		2.9 V	V_{CCB}O/P × 0.8			
V_{OL}	CLKB output port	I_{OL} = 100 µA	1.1 V to 3.6 V	2.9 V			V_{CCB}O/P × 0.8	V
		I_{OL} = 8 mA					0.7	
	B port (DAT and CMD outputs)	I_{OL} = 135 µA	1.1 V to 3.6 V	2.9 V			0.4	V
		I_{OL} = 180 µA					0.4	
		I_{OL} = 220 µA					0.4	
		I_{OL} = 300 µA					0.4	
		I_{OL} = 400 µA					0.55	
I_I	Control inputs	V_I = V_{CCA} or GND	1.1 V to 3.6 V	2.9 V			±1	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.1 V to 3.6 V	2.9 V			6	µA
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.1 V to 3.6 V	2.9 V			5	µA
C_{io}	A port					5.5	6.5	pF
	B port					15	17.5	
C_i	Control inputs	V_I = V_{CCA} or GND				3.5	4.5	pF
	Clock input					3	4	

(1) All typical values are at T_A = 25°C.

ELECTRICAL CHARACTERISTICS
LDO

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{BATT}	Input voltage			V_{OUT} + V_{DO}		5.5	V
V_{OUT}	Output voltage	Nominal T_A = 25°C			2.9		V
		All conditions		2.75		3.05	
ΔV_{OUT}	Output voltage tolerance	Nominal T_A = 25°C			±3		%
V_{DO}	Dropout voltage	I_{OUT} = 200 mA			200	250	mV
I_{GND}	Ground-pin current	I_{OUT} = 0				40	µA
		I_{OUT} < 100 mA				200	
		100 mA ≤ I_{OUT} ≤ 200 mA				400	
$I_{OUT(SC)}$	Short-circuit current	R_L = 0 Ω			300		mA
PSRR	Power-supply rejection ratio	V_{IN} = 3.05 V, V_{OUT} = 2.9 V, C_{NR} = 0.01 µF, I_{OUT} = 200 mA	f = 1 kHz		50		dB
			f = 10 kHz		40		
t_{STR}	Start-up time	V_{OUT} = 2.9 V, I_{OUT} = 200 mA, C_{OUT} = 2.2 µF				200	µs

(1) All typical values are at T_A = 25°C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCB} = 2.9 V ± 5% (unless otherwise noted)

			V_{CCA} = 1.2 V ± 0.1 V		V_{CCA} = 1.5 V ± 0.1 V		V_{CCA} = 1.8 V ± 0.15 V		V_{CCA} = 2.5 V ± 0.2 V		V_{CCA} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Command	Push-pull driving		40		60		60		60		60	Mbps
		Open-drain driving		1		1		1		1		1	
	Clock	Push-pull driving		60		60		60		60		60	MHz
	Data			40		60		60		60		60	Mbps
t_W Pulse duration	Command	Push-pull driving	25		17		17		17		17		ns
		Open-drain driving	1		1		1		1		1		µs
	Clock	Push-pull driving	8.3		8.3		8.3		8.3		8.3		ns
	Data		25		17		17		17		17		ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCB} = 2.9 V ± 5% (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCA} = 1.2 V ± 0.1 V		V_{CCA} = 1.5 V ± 0.1 V		V_{CCA} = 1.8 V ± 0.15 V		V_{CCA} = 2.5 V ± 0.2 V		V_{CCA} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CMDA	CMDB	Push-pull driving		10.8		6.1		4.6		3.7		3.8	ns
			Open-drain driving (H-to-L)	3.2	10.6	2.7	6.6	2.4	5.5	2.1	4.4	2	4.1	
			Open-drain driving (L-to-H)	71	175	83	180	89	201	98	249	101	233	
	CMDB	CMDA	Push-pull driving		12		6.8		5.2		4.1		3.4	
			Open-drain driving (H-to-L)	2.9	9.4	2.1	7.3	2	6.4	2	5.7	2.2	4.6	
			Open-drain driving (L-to-H)	77	243	87	214	93	215	99	261	105	248	
	CLKA	CLKB	Push-pull driving		11.7		6.2		4.7		3.7		3.5	
	DATxA	DATxB	Push-pull driving		11.1		6.2		4.7		3.7		3.7	
	DATxB	DATxA			11.5		6.2		5		3.9		6.2	
	CLKA	CLK-f	Push-pull driving		24.7		13		8.9		6.8		4.8	
t_{en}	EN	B-port	Push-pull driving		1		1		1		1		1	µs
	EN	A-port	Push-pull driving		1		1		1		1		1	
t_{dis}	EN	B-port	Push-pull driving		40		39		35		38		34	ns
	EN	A-port	Push-pull driving		40		38		38		38		36	
t_{rA}	CMDA rise time		Push-pull driving	1.6	12.2	0.4	8.3	1.1	5.9	1.9	3.3	0.8	4.2	ns
			Open-drain driving	32	120	44	127	52	150	62	201	74	194	
	CLK-f rise time		Push-pull driving	0.6	12.7	0.5	7.2	0.4	4.5	0.7	1.5	0.7	1.4	
	DATxA rise time			1.6	11.6	0.6	8.4	1	6.3	1.8	4.2	1.1	3.3	
t_{rB}	CMDB rise time		Push-pull driving	1.7	6.7	0.5	5.6	1	5.2	1.5	5.2	1.9	5	ns
			Open-drain driving	66	214	71	196	73	184	76	214	79	185	
	CLKB rise time		Push-pull driving	1.7	4.8	1.5	4.9	1.5	4.9	1.6	5	1.6	5.1	
	DATxB rise time			0.4	6.8	0.6	5	0.2	5.2	0.9	5.3	1	14	
t_{fA}	CMDA fall time		Push-pull driving	0.8	4	0.8	2.3	0.2	3.1	0.3	1.5	1	2.3	ns
			Open-drain driving	1.6	3.9	1.6	3.7	1.6	3.7	1.6	3.7	1.6	3.9	
	CLK-f fall time		Push-pull driving	1	4	0.4	6.8	0.1	1.5	0.3	2.8	0.6	1.3	
	DATxA fall time			1	3.9	0.1	3.8	0.2	2.7	0.3	2.9	0.4	1.8	
t_{fB}	CMDB fall time		Push-pull driving	1.5	4.5	1.4	5.4	1.6	5	1.6	5.6	0.8	6.3	ns
			Open-drain driving	1	4.3	1	2.3	0.8	1.9	0.8	1.6	0.9	1.3	
	CLKB fall time		Push-pull driving	1.6	4	1.6	4.1	1.7	4.2	1.7	4.5	0.9	5.1	
	DATxB fall time			1	4.8	2.3	4.3	0.8	4.9	0.2	4.9	0.8	6.9	
$t_{SK(O)}$	Channel-to-channel skew		Push-pull driving		1		1		1		1		1	ns
Max data rate	Command		Push-pull driving		40		60		60		60		60	Mbps
			Open-drain driving		1		1		1		1		1	
	Clock		Push-pull driving		60		60		60		60		60	MHz
	Data				40		60		60		60		60	Mbps

OPERATING CHARACTERISTICS

T_A = 25°C, V_{CCB} = 2.9 V

PARAMETER			TEST CONDITIONS	V_{CCA} TYP						UNIT
				1.2 V	1.5 V	1.8 V	2.5 V	3 V	3.3 V	
C_{pdA} (1)	A-port input, B-port output	CLK Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	15	15	15	15.7	17.1	17.1	pF
		DATA Enabled		6.3	6.4	6.5	6.5	6.5	6.5	
	B-port input, A-port output	DATA Enabled		12.5	12.3	12.3	12.5	14	14	
	A-port input, B-port output	CLK Disabled		0.2	0.2	0.2	0.3	0.3	0.3	
		DATA Disabled		1.2	1.2	1.2	1.2	1.2	1.2	
	B-port input, A-port output	DATA Disabled		0.2	0.2	0.2	0.3	0.3	0.3	
C_{pdB} (1)	A-port input, B-port output	DATA Enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	31.2	30.6	30.3	29.5	28.5	28.5	pF
	B-port input, A-port output	CLK Enabled		28.1	27.2	27	26.9	27	27	
		DATA Enabled		12.9	12.8	12.9	13.2	13.2	13.2	
	A-port input, B-port output	DATA Disabled		0.6	0.5	0.5	0.5	0.5	0.6	
	B-port input, A-port output	CLK Disabled		0.6	0.5	0.5	0.5	0.5	0.6	
		DATA Disabled		1.2	1.2	1.2	1	1	1	

(1) Power dissipation capacitance per transceiver

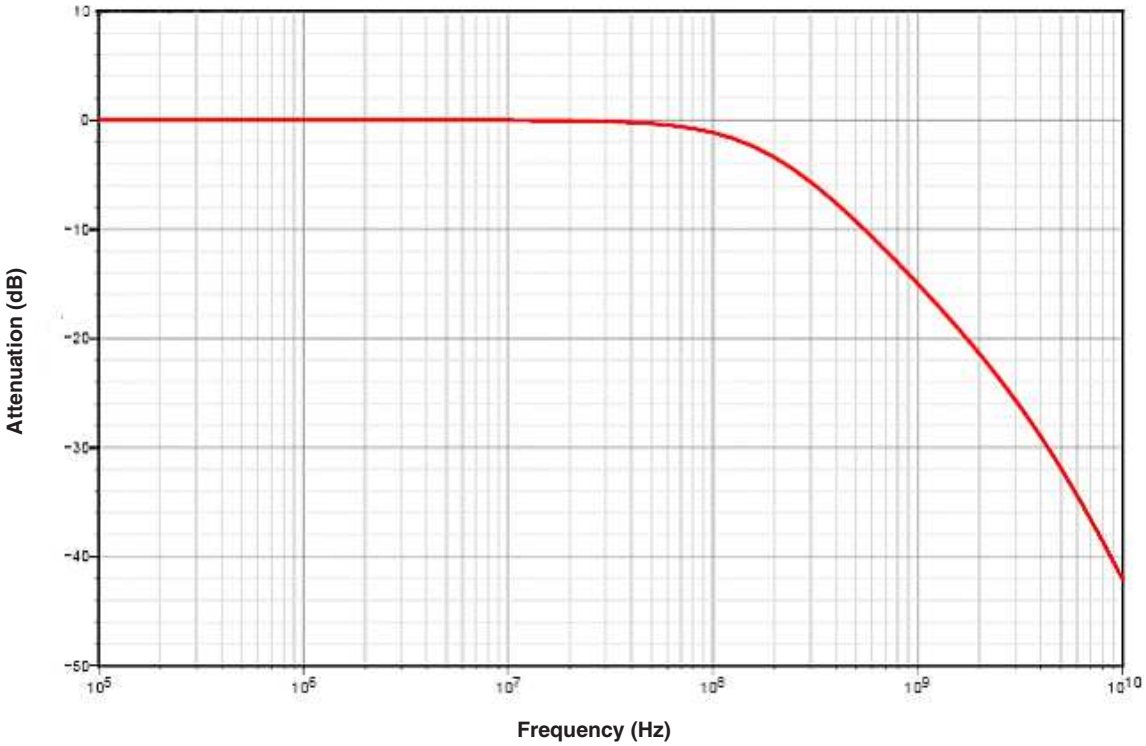


Figure 6. Typical ASIP EMI Filter Frequency Response

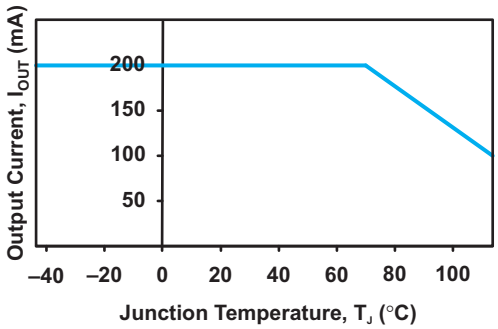
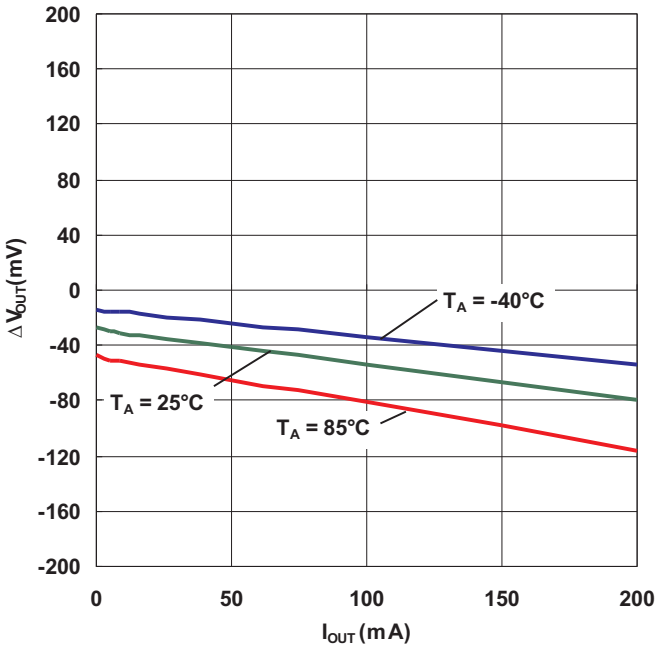


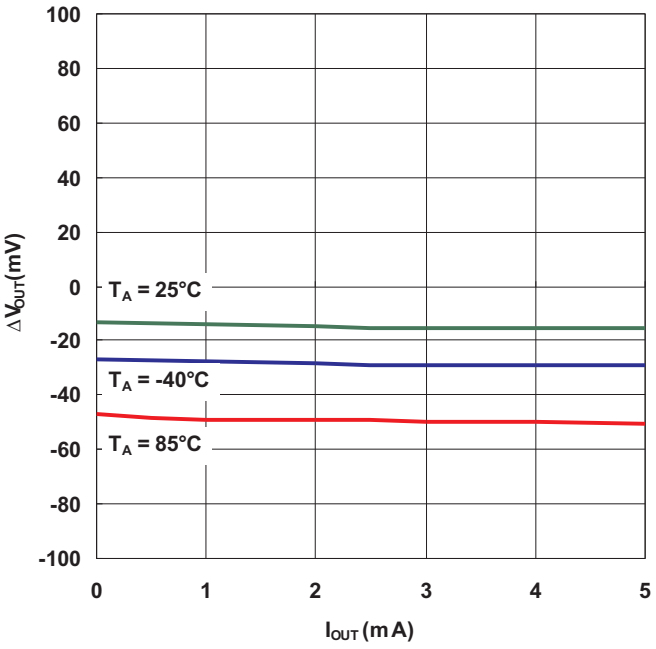
Figure 7. LDO Output Current Derating

TYPICAL CHARACTERISTICS

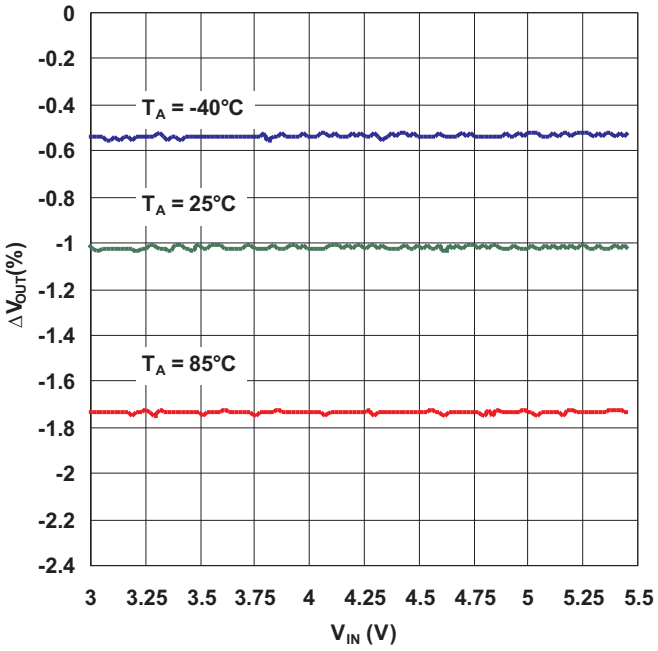
LOAD REGULATION



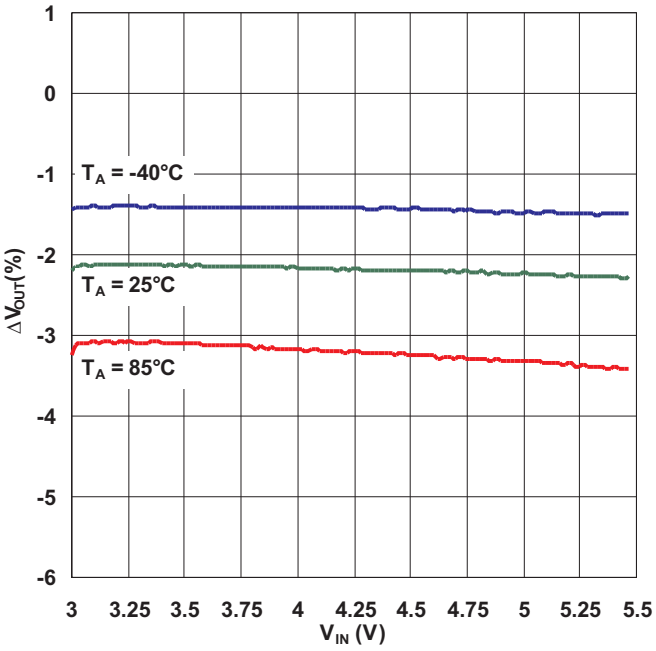
LOAD REGULATION, LIGHT LOADS



LINE REGULATION
(I_{OUT} = 5 mA)

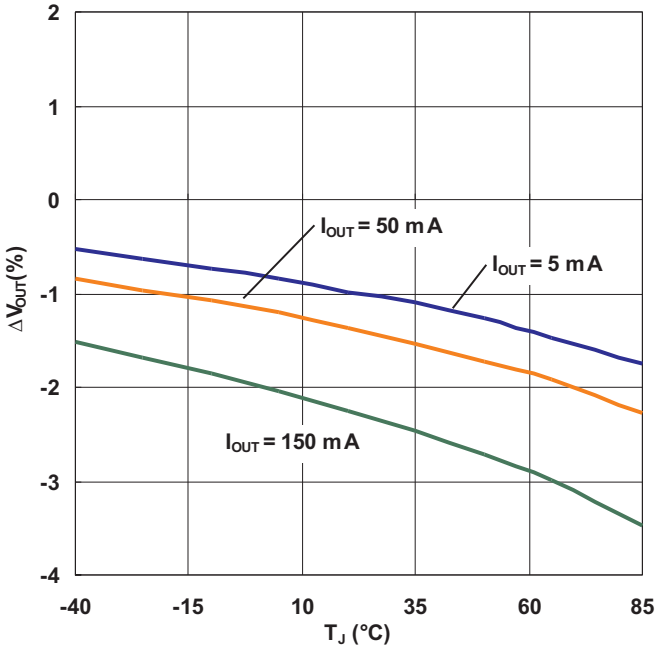


LINE REGULATION
(I_{OUT} = 150 mA)

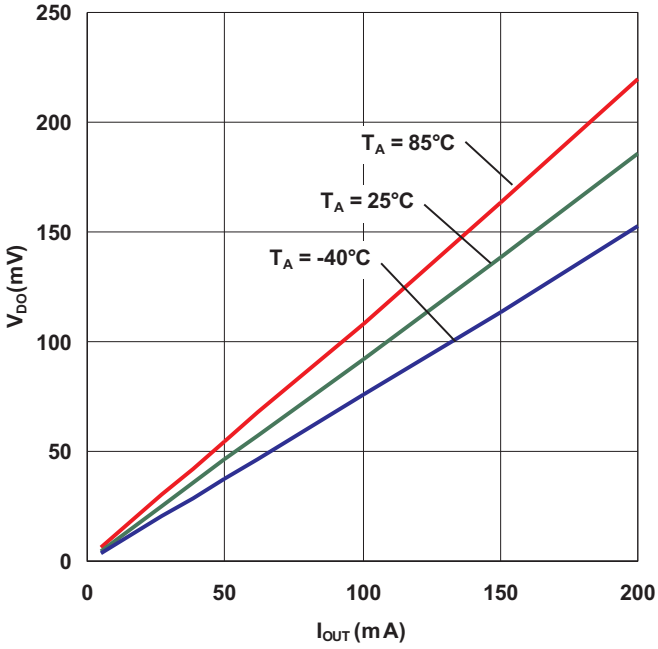


TYPICAL CHARACTERISTICS (continued)

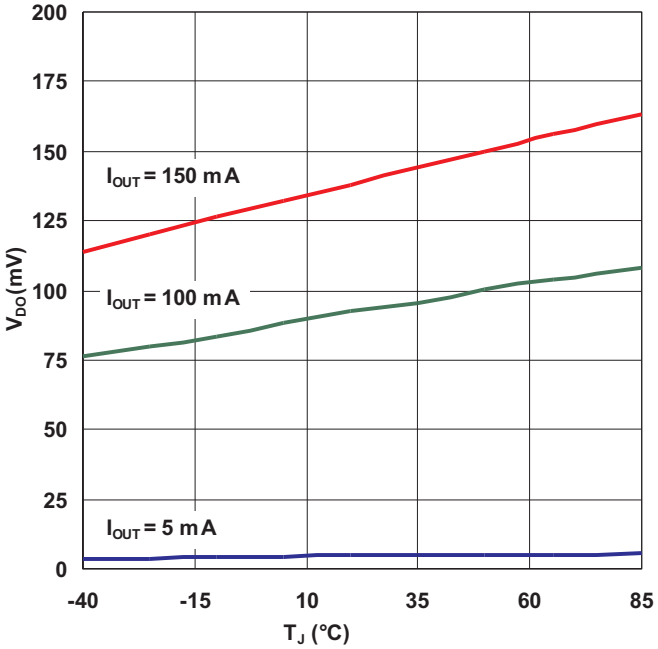
OUTPUT VOLTAGE vs TEMPERATURE



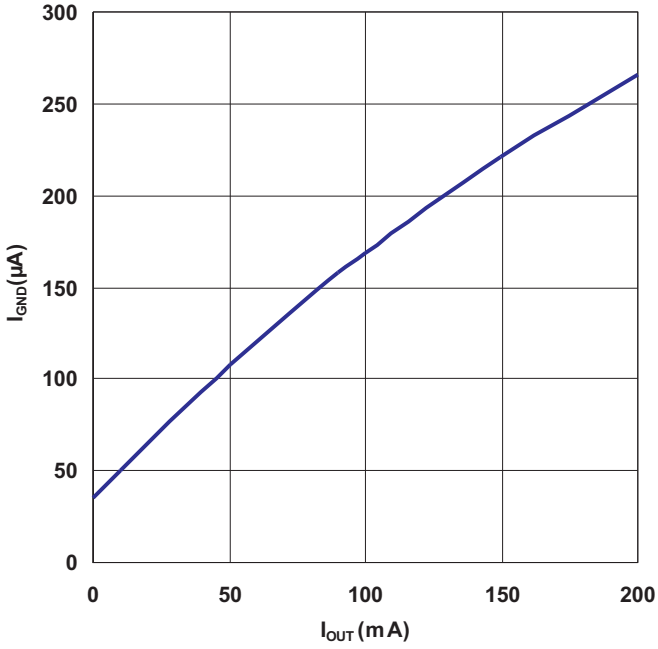
DROPOUT VOLTAGE vs OUTPUT CURRENT



DROPOUT VOLTAGE vs TEMPERATURE

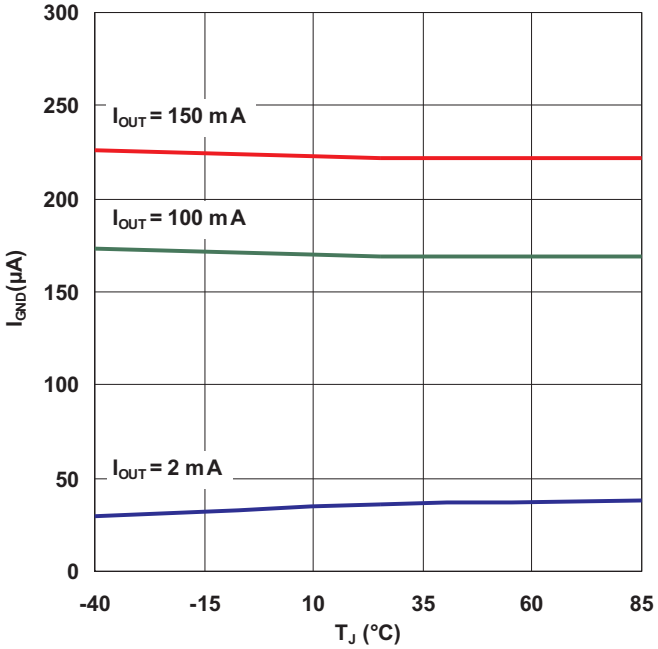


GROUND PIN CURRENT vs OUTPUT CURRENT

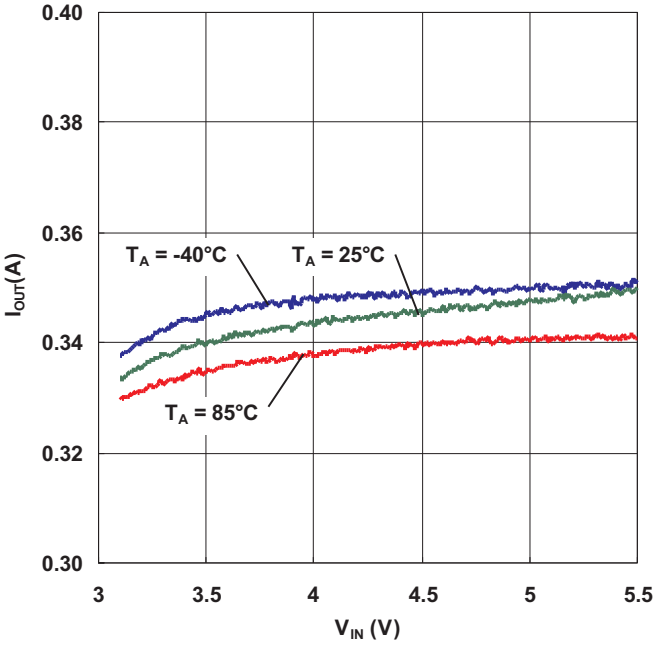


TYPICAL CHARACTERISTICS (continued)

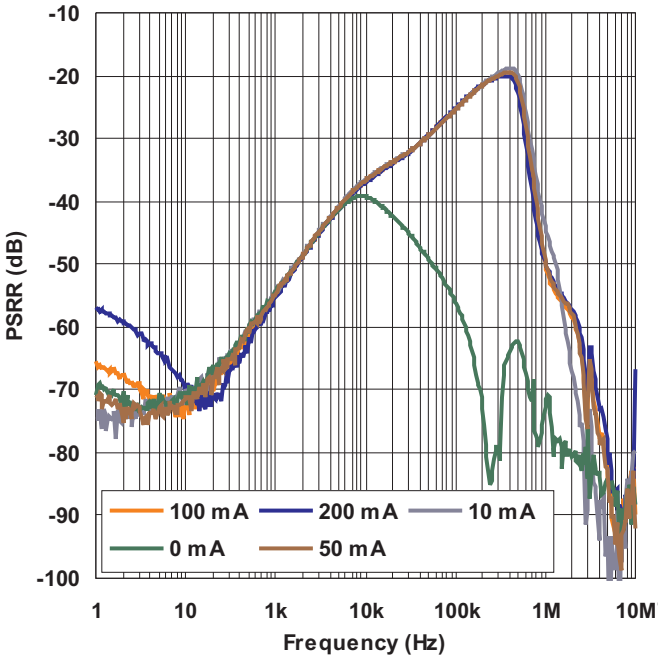
GROUND PIN CURRENT vs TEMPERATURE (ENABLE)



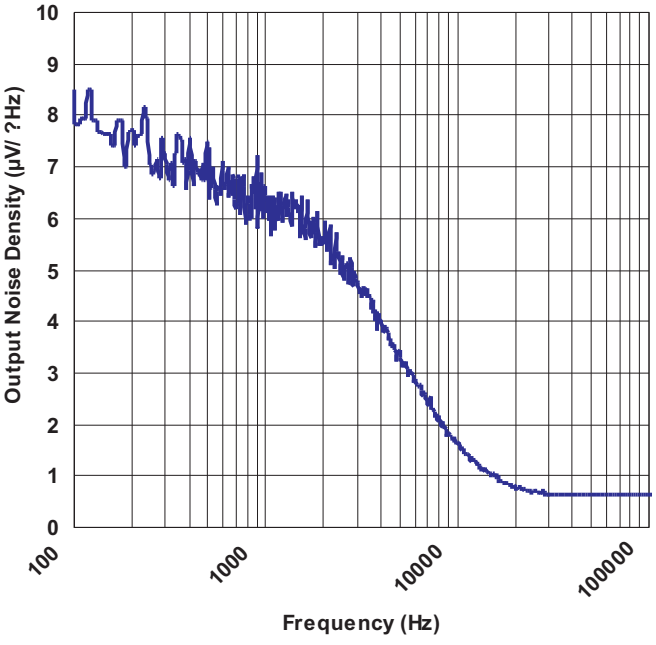
CURRENT LIMIT vs INPUT VOLTAGE



POWER SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} - V_{OUT} = 1 V)

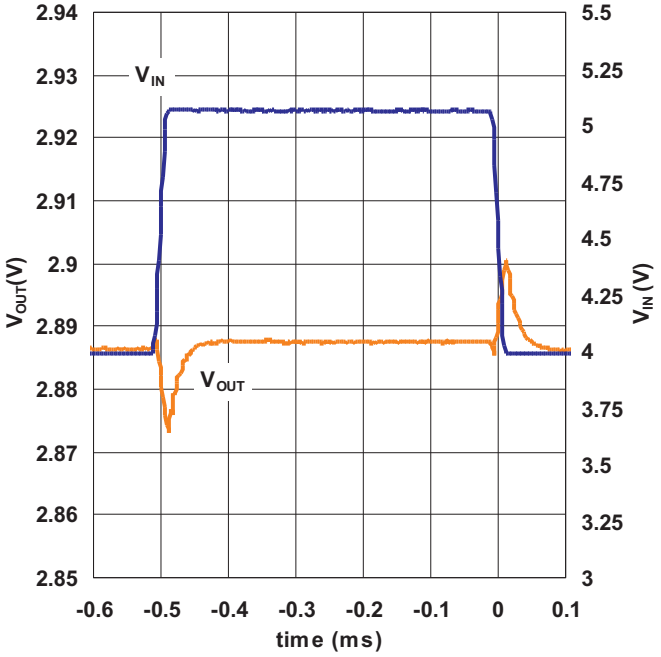


OUTPUT SPECTRAL NOISE DENSITY (C_{OUT} = 1 µF)

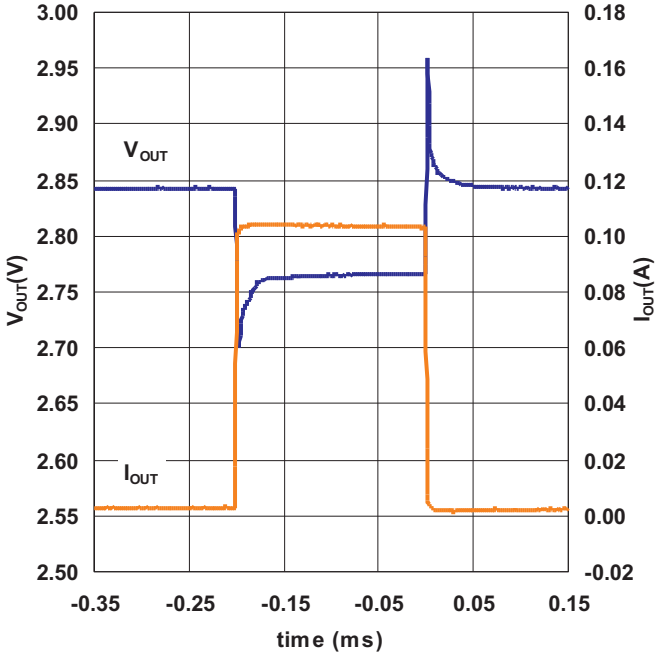


TYPICAL CHARACTERISTICS (continued)

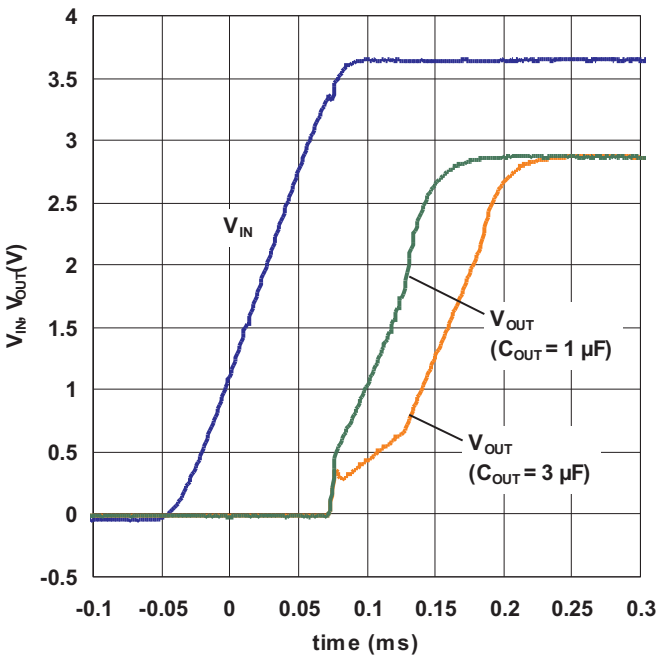
LINE TRANSIENT RESPONSE
(C_{OUT} = 1 µF)



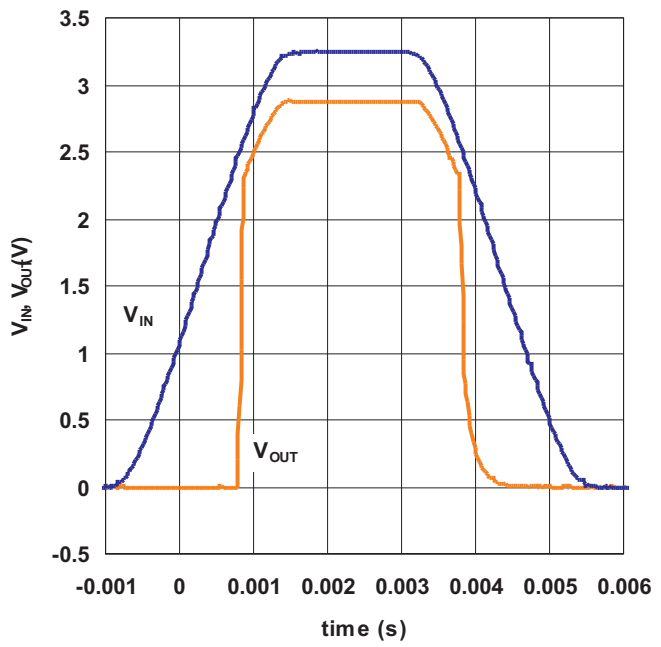
LOAD TRANSIENT RESPONSE
(C_{OUT} = 1 µF, V_{IN} = 3.3 V, I_{OUT} = 0 to 100 mA)



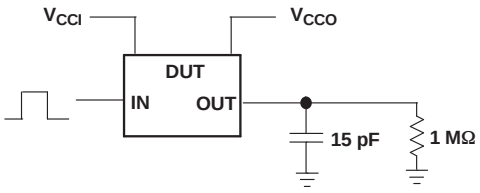
TURN-ON RESPONSE



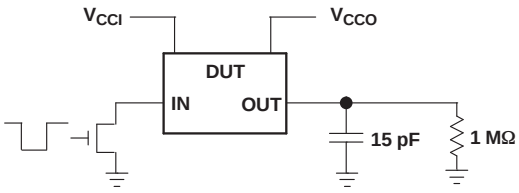
POWER-UP/POWER-DOWN
(C_{OUT} = 1 µF, I_{OUT} = 150 mA)



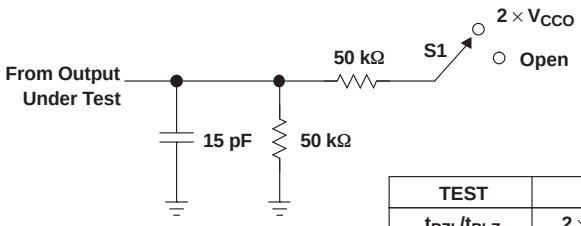
PARAMETER MEASUREMENT INFORMATION



DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER

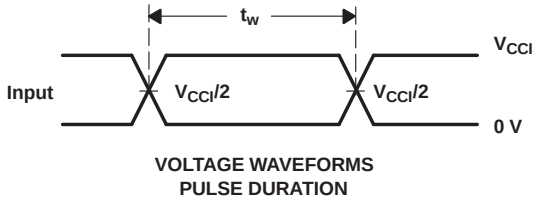


DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER

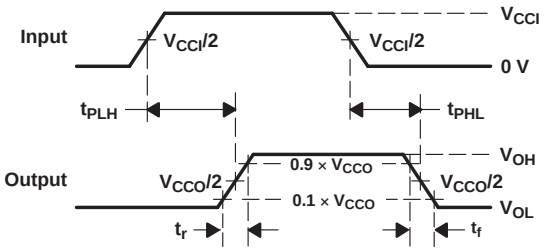


TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open

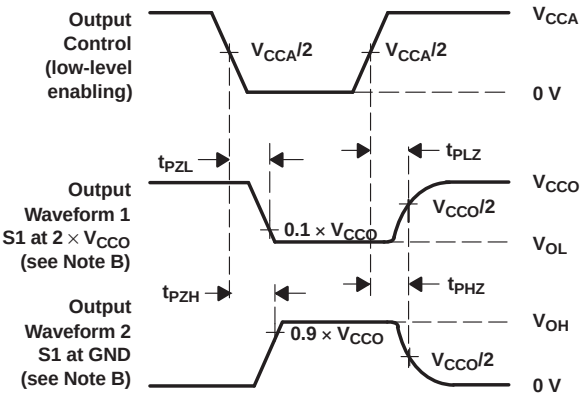
LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 8. Load Circuit and Voltage WaveformsN

PRINCIPLES OF OPERATION

Applications

The TXS0206-29 device is a complete application-specific voltage-translator designed to bridge the digital-switching compatibility gap and interface logic threshold levels between a micrprocessor with MMC, SD, and Memory Stick™ cards. It is intended to be used in a point-to-point topology when interfacing these devices that may or may not be operating at different interface voltages.

Architecture

The CLKA, CLKB, and CLK-f subsystem interfaces consist of a fully-buffered voltage translator design that has its output transistors to source and sink current optimized for drive strength.

The SDIO lines comprise a semi-buffered auto-direction-sensing based translator architecture (see Figure 9) that does not require a direction-control signal to control the direction of data flow of the A to B ports (or from B to A ports).

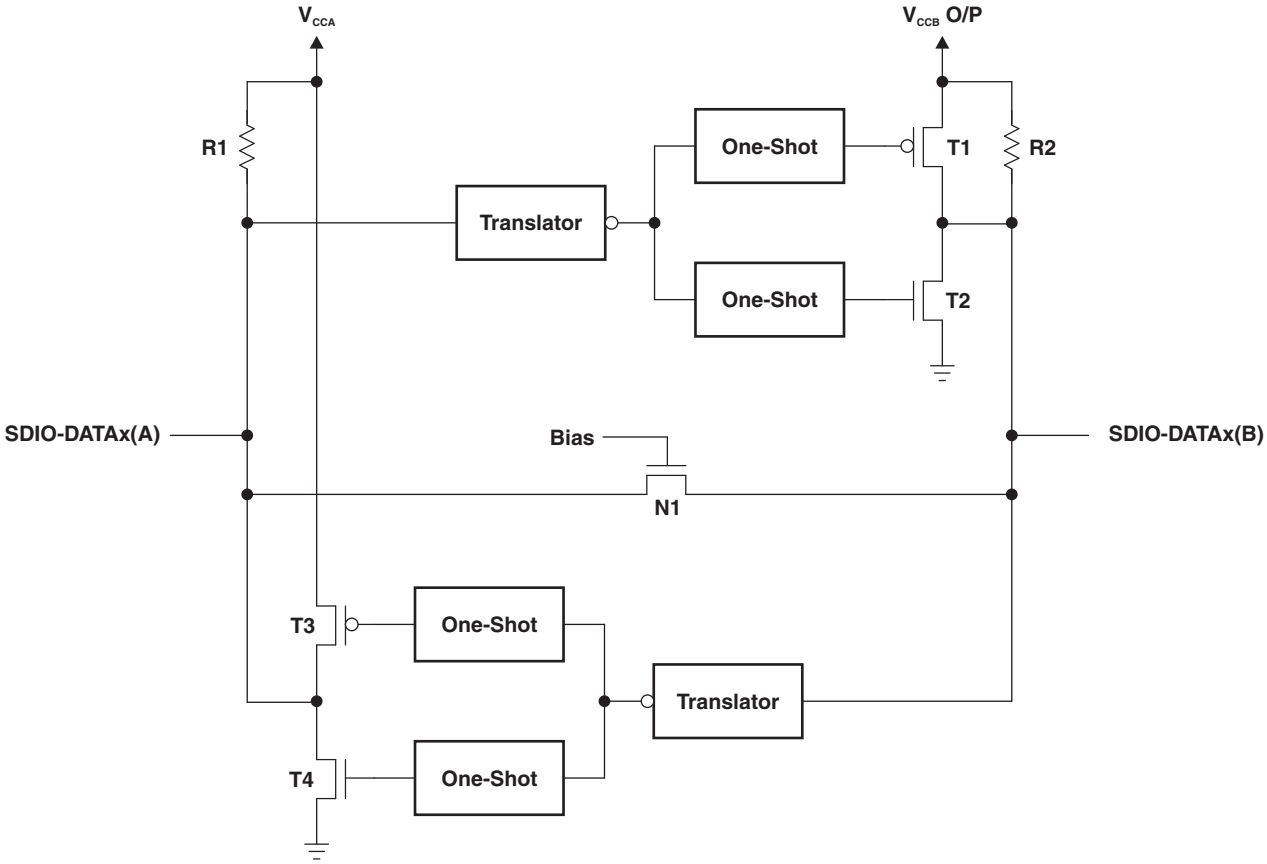


Figure 9. Architecture of an SDIO Switch-Type Cell

Each of these bidirectional SDIO channels independently determines the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The following two key circuits are employed to facilitate the "switch-type" voltage translation function:

1. Integrated pullup resistors to provide dc-bias and drive capabilities
2. An N-channel pass-gate transistor topology (with a high R_{ON} of ~300 Ω) that ties the A-port to the B-port
3. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at a level that optimizes the switch characteristics for maximum data rate as well as minimal static supply leakage. Data can flow in either direction without guidance from a control signal.

The edge-rate acceleration circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device.

During a low-to-high signal rising-edge, the O.S. circuits turn on the PMOS transistors (T_1, T_3) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal pullup resistors during the low-to-high transition to speed up the rising-edge signal.

During a high-to-low signal falling-edge, the O.S. circuits turn on the NMOS transistors (T_2, T_4) and its associated driver output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first.

To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn-off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

Once the O.S. is triggered and switched off, both the A and B ports must go to the same state (i.e. both High or both Low) for the one-shot to trigger again. In a DC state, the output drivers maintain a Low state through the pass transistor. The output drivers maintain a High through the "smart pullup resistors" that dynamically change value based on whether a Low or a High is being passed through the SDIO lines, as follows:

- R_{PU1} and R_{PU2} values are a nominal 40 kΩ when the output is driving a low
- R_{PU1} and R_{PU2} values are a nominal 4 kΩ when the output is driving a high
- R_{PU1} and R_{PU2} values are a nominal 70 kΩ when the device is disabled via the EN pin or by pulling the either V_{CCA} or V_{CCB}O/P to 0 V.

The reason for using these "smart" pullup resistors is to allow the TXS0206-29 to realize a lower static power consumption (when the I/Os are low), support lower V_{OL} values for the same size pass-gate transistor, and improved simultaneous switching performance.

Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level driver interfaced to the SDIO pins. Since the high bandwidth of these bidirectional SDIO circuits necessitates the need for a port to quickly change from an input to an output (and vice-vera), they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the smart pullup resistor values.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge rate and output impedance of the external device driving the SDIO I/Os, as well as the capacitive loading on these lines.

Similarly, the t_{pd} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{pd}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXS0206-29 SDIO output sees, so it is recommended that this lumped-load capacitance be considered and kept below 50 pF to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

When using the TXS0206-29 device with MMCs, SD, and Memory Stick™ to ensure that a valid receiver input voltage high (V_{IH}) is achieved, the value of any pulldown resistors (external or internal to a memory card) must not be >10-kΩ value. The impact of adding too heavy a pulldown resistor (i.e. <10-kΩ value) to the data and command lines of the TXS0206-29 device and the resulting 4-kΩ pullup & 10-kΩ pulldown voltage divider network has a direct impact on the V_{IH} of the signal being sent into the memory card and its associated logic.

The resulting V_{IH} voltage for the 10-kΩ pulldown resistor value would be:

V_{CC} × 10 kΩ / (10 kΩ+ 4 kΩ) = 0.714 × V_{CC}

This is marginally above a valid input high voltage for a 1.8-V signal (i.e., 0.65 × V_{CC}).

The resulting V_{IH} voltage for 20-kΩ pulldown resistor value would be:

V_{CC} × 20 kΩ / (20 kΩ + 4 kΩ) = 0.833 × V_{CC}

Which is above the valid input high voltage for a 1.8-V signal of 0.65 × V_{CC}.

.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TXS0206-29YFPR	ACTIVE	DSBGA	YFP	20	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

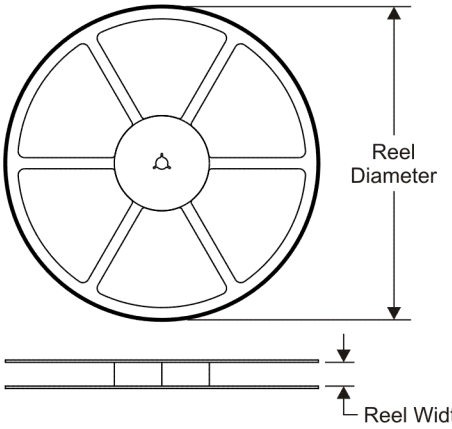
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

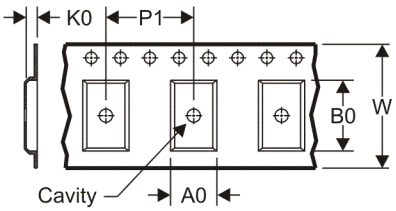
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

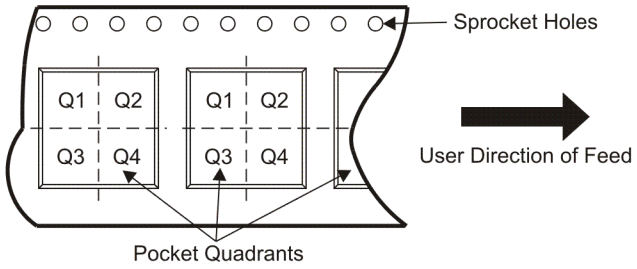


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

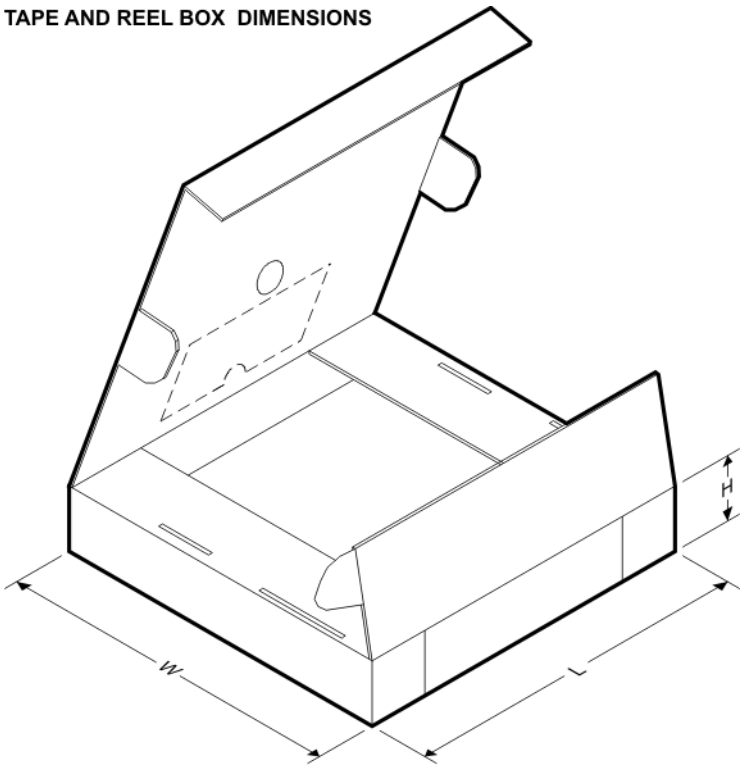
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0206-29YFPR	DSBGA	YFP	20	3000	180.0	8.4	1.65	2.05	0.6	4.0	8.0	Q1

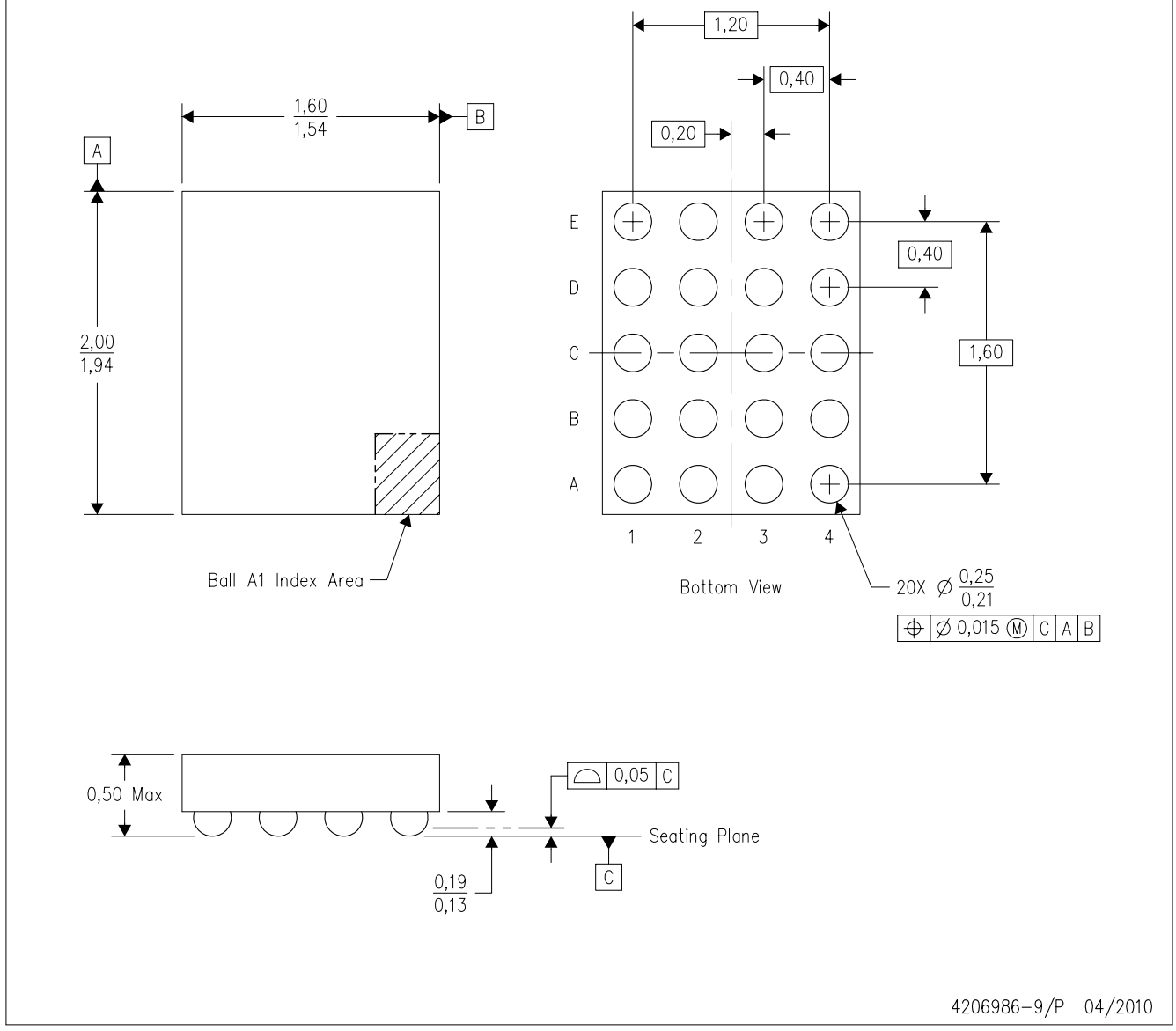
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0206-29YFPR	DSBGA	YFP	20	3000	220.0	220.0	34.0

YFP (R–XBGA–N20) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This is a Pb–free solder ball design.

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