HARRIS SEMICONDUCTOR

T-51-09-12

AD7545
12-Bit Buffered Multiplying CMOS DAC

GENERAL DESCRIPTION

The AD7545 is a low cost monolithic 12-bit CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12- and 16-bit bus systems. Loading of the input latches is under the control of the $\overline{CS}$ and $\overline{WR}$ inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

FEATURES

- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Low Power
- Low Cost

ORDERING INFORMATION

Part Number	Temperature Range	Package
AD7545JN	0°C to +70°C	20 Pin Plastic DIP
AD7545KN	0°C to +70°C	20 Pin Plastic DIP
AD7545AN	-40°C to +85°C	20 Pin Plastic DIP
AD7545BN	-40°C to +85°C	20 Pin Plastic DIP
AD7545AD	-40°C to +85°C	20 Pin Ceramic DIP
AD7545BD	-40°C to +85°C	20 Pin Ceramic DIP
AD7545SD	-55°C to +125°C	20 Pin Ceramic DIP
AD7545SQ/883	-55°C to +125°C	20 Pin Ceramic DIP

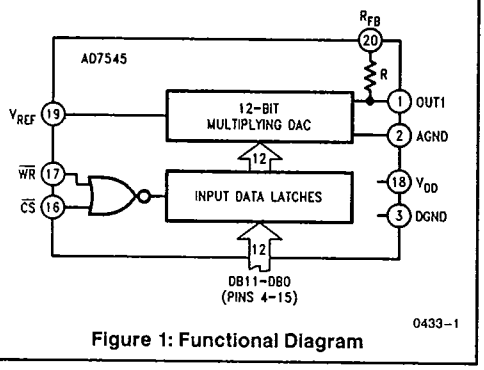


Figure 1: Functional Diagram

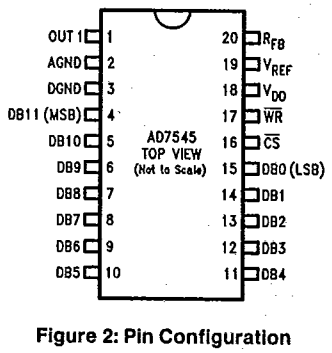


Figure 2: Pin Configuration

6

NOTE: All typical values have been characterized but are not tested.

300152-001

ABSOLUTE MAXIMUM RATINGS

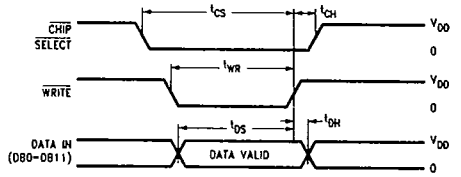
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... −0.3V, +17V
Digital Input Voltage to DGND ..... −0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND ..... ±25V
V_{PIN1} to DGND ..... −0.3V, V_{DD} +0.3V
AGND to DGND ..... −0.3V, V_{DD} +0.3V
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above 75°C by ..... 6 mW/°C

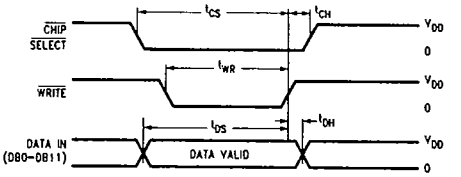
T-51-09-12

Operating Temperature
Commercial
(J, K) Grades ..... 0°C to +70°C
Industrial
(A, B) Grades ..... −40°C to +85°C
Extended
(S) Grades ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



A: Typical Write Cycle



B: Preferred Write Cycle

MODE SELECTION

WRITE MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.

HOLD MODE:
Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20 ns
V_{DD} = +15V; $t_r = t_f$ = 40 ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Since input data latches are transparent for $\overline{CS}$ and $\overline{WR}$ both low, it is preferred to have data valid before $\overline{CS}$ and $\overline{WR}$ both go low. This prevents undesirable changes at the analog output while the data inputs settle.

Figure 3: Write Cycle Timing Diagram

CIRCUIT INFORMATION—D/A CONVERTER SECTION

Figure 4 shows a simplified circuit of the D/A converter section of the AD7545. Note that the ladder termination resistor is connected to AGND. R is typically 11 kΩ.

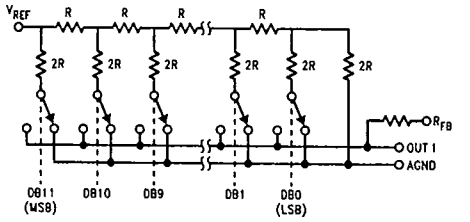


Figure 4: Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state. One of the current switches is shown in Figure 5.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70 pF (all switches to AGND) to 200 pF (all switches to OUT1).

The input resistance at V_{REF} (Figure 4) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

NOTE: All typical values have been characterized but are not tested.

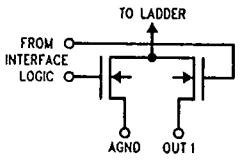


Figure 5: N-Channel Current Steering Switch

CIRCUIT INFORMATION— DIGITAL SECTION

Figure 6 shows the digital structure for one bit.

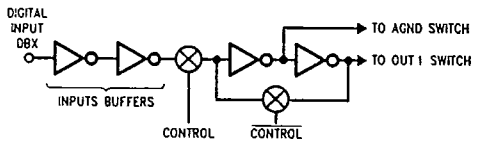


Figure 6: Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range 5V ≤ V_{DD} ≤ 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

APPLICATION

Output Offset: CMOS current-steering D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND connection is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{\text{WR}}$ and $\overline{\text{CS}}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{\text{WR}}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse ($\overline{\text{WR}}$) so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by isolating the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid isolation at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5V. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

6

NOTE All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified

Parameter	Test Conditions Comments	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units
			T_A = +25°C	T_{min}, T_{max} (Note 1)	T_A = +25°C	T_{min}, T_{max} (Note 1)	
STATIC PERFORMANCE							
Resolution		All	12	12	12	12	Bits
Relative Accuracy		J, A, S K, B	±2 ±1	±2 ±1	±2 ±1	±2 ±1	LSB max LSB max
Differential Nonlinearity	10-Bit Monotonic T_{min} to T_{max} 12-Bit Monotonic T_{min} to T_{max}	J, A, S K, B	±4 ±1	±4 ±1	±4 ±1	±4 ±1	LSB max LSB max
Gain Error (Using Internal RFB) (Note 2)	DAC Register Loaded with 1111 1111 1111 Gain Error is Adjustable Using the Circuits of Figures 7 and 8	J, A, S K, B	±20 ±10	±20 ±10	±25 ±15	±25 ±15	LSB max LSB max
Gain Temperature Coefficient (Note 3) ΔGain/ΔTemperature	Typical Value is 2 ppm/°C for V_{DD} = +5V	All	±5	±5	±10	±10	ppm/°C max
DC Supply Rejection ΔGain/ΔV_{DD}	ΔV_{DD} = ±5%	All	0.015	0.03	0.01	0.02	% per % max
Output Leakage Current at OUT1	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V	J, K A, B S	10 10 10	50 50 200	10 10 10	50 50 200	nA max nA max nA max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified (Continued)

Parameter	Test Conditions Comments	Version	V_{DD} = +5V Limits T_A = +25°C	V_{DD} = +5V Limits T_{min}, T_{max} (Note 1)	V_{DD} = +15V Limits T_A = +25°C	V_{DD} = +15V Limits T_{min}, T_{max} (Note 1)	Units
DYNAMIC PERFORMANCE							
Current Settling Time (Note 3)	To ½ LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.	All	2	2	2	2	µs max
Propagation Delay (Note 3) (from Digital Input Change to 90% of final Analog Output)	OUT1 LOAD = 100Ω C_{EXT} = 13 pF (Note 4)	All	300		250		ns max
Digital to Analog Glitch Impulse	V_{REF} = AGND	All	400		250		nV sec typ
AC Feedthrough (Note 5) At OUT1	V_{REF} = ±10V, 10 kHz Sinewave	All	5	5	5	5	mVp-p typ
REFERENCE INPUT							
Input Resistance (Pin 19 to GND)	Input Resistance TC = −300 ppm/°C typ Typical Input Resistance = 11 kΩ	All	7 25	7 25	7 25	7 25	kΩ min kΩ max
ANALOG OUTPUTS							
Output Capacitance (Note 3) C_{OUT1} C_{OUT1}	 DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V	 All All	 70 200	 70 200	 70 200	 70 200	 pF max pF max
DIGITAL INPUTS							
Input High Voltage V_{IH}		All	2.4	2.4	13.5	13.5	V min
Input Low Voltage V_{IL}		All	0.8	0.8	1.5	1.5	V max
Input Current (Note 6) I_{IN}	V_{IN} = 0 or V_{DD}	All	±1	±10	±1	±10	µA max
Input Capacitance (Note 3) DB0–DB11 $\overline{WR}$, $\overline{CS}$	 V_{IN} = 0 V_{IN} = 0	 All All	 7 20	 7 20	 7 20	 7 20	 pF max pF max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified (Continued)

Parameter	Test Conditions/Comments	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units
			T_A = +25°C	T_{min}, T_{max} (Note 1)	T_A = +25°C	T_{min}, T_{max} (Note 1)	
SWITCHING CHARACTERISTICS (Note 3)							
Chip Select to Write Setup Time t_{CS}	See Figure 3	All	280 200	380 270	180 120	200 150	ns min ns typ
Chip Select to Write Hold Time t_{CH}	See Figure 3	All	0	0	0	0	ns min
Write Pulse Width t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$ See Figure 3	All	250 175	400 280	160 100	240 170	ns min ns typ
Data Setup Time t_{DS}	See Figure 3	All	140 100	210 150	90 60	120 80	ns min ns typ
Data Hold Time t_{DH}	See Figure 3	All	10	10	10	10	ns min
POWER SUPPLY							
I_{DD}	All Digital Inputs V_{IL} or V_{IH} All Digital Inputs 0V or V_{DD} All Digital Inputs 0V or V_{DD}	All	2 100 10	2 500 10	2 100 10	2 500 10	mA max µA max µA typ

NOTE 1: Temperature Ranges as follows: J, K versions: 0°C to +70°C
A, B versions: −20°C to +85°C
S version: −55°C to +125°C

2: This includes the effect of 5 ppm max gain TC.

3: Parameter not tested. Parameter guaranteed by design, simulation, or characterization.

4: DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.

5: Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

6: Logic inputs are MOS gates. Typical input current (+25°C) is less than 1 nA.

Specifications subject to change without notice.

NOTE: All typical values have been characterized but are not tested.

BASIC APPLICATIONS

Figures 7 and 8 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that the circuits of Figures 7 and 8 have constant input impedance at the V_{REF} terminal.

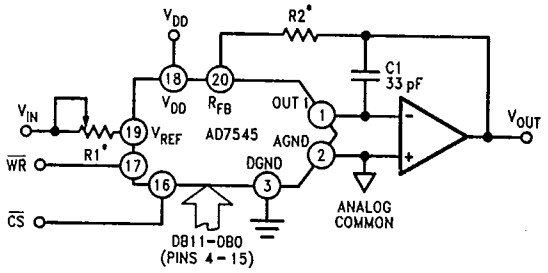
The circuit of Figure 7 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 7.

Table 1: Recommended Trim Resistor Values vs. Grades for $V_{DD} = +5V$

TRIM RESISTOR	J/A/S	K/B
R1	500Ω	200Ω
R2	150Ω	68Ω

Table 2. Unipolar Binary Code Table for Circuit of Figure 7

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0V



*Refer to Table 1

Figure 7: Unipolar Binary Operation

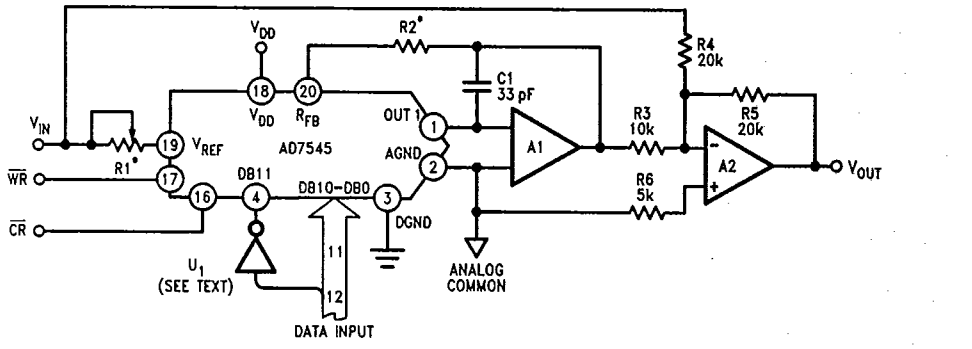
6

NOTE: All typical values have been characterized but are not tested.

Figure 8 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

Table 3: 2's Complement Code Table for Circuit of Figure 8

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \bullet \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0V
1111	1111	1111	$-V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \bullet \left\{\frac{2048}{2048}\right\}$



*For Values of R1 and R2 See Table 1.

Figure 8: Bipolar Operation (2's Complement Code)

The choice of the operational amplifiers in Figures 7 and 8 depends on the application and the trade off between required precision and speed. Below is a list of operational amplifiers which are good candidates for many applications. The main selection criteria for these operational amplifiers is to have low V_{OS}, low V_{OS} drift, low bias current and low settling time.

These amplifiers need to maintain the low nonlinearity and monotonic operation of the D/A while providing enough speed for maximum converter performance.

Operational Amplifiers:

HA5127 Ultra Low Noise, Precision
HA5137 Ultra Low Noise, Precision, Wide Band
HA5147 Ultra Low Noise, Precision, High Slew Rate
HA5170 Precision, JFET Input

NOTE All typical values have been characterized but are not tested.