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LPC2101/2102/2103

Single-chip 16-bit/32-bit microcontrollers; 8 kB/16 kB/32 kB flash with ISP/IAP, fast ports and 10-bit ADC

Rev. 01 — 18 January 2006 Preliminary data sheet

1. General description

The LPC2101/2102/2103 microcontrollers are based on a 16-bit/32-bit ARM7TDMI-S CPU with real-time emulation that combines the microcontroller with 8 kB, 16 kB or 32 kB of embedded high-speed flash memory. A 128-bit wide memory interface and a unique accelerator architecture enable 32-bit code execution at the maximum clock rate. For critical performance in interrupt service routines and DSP algorithms, this increases performance up to 30 % over Thumb mode. For critical code size applications, the alternative 16-bit Thumb mode reduces code by more than 30 % with minimal performance penalty.

Due to their tiny size and low power consumption, the LPC2101/2102/2103 are ideal for applications where miniaturization is a key requirement. A blend of serial communications interfaces ranging from multiple UARTs, SPI to SSP and two I^2C-buses, combined with on-chip SRAM of 2 kB/4 kB/8 kB, make these devices very well suited for communication gateways and protocol converters. The superior performance also makes these devices suitable for use as math coprocessors. Various 32-bit and 16-bit timers, an improved 10-bit ADC, PWM features through output match on all timers, and 32 fast GPIO lines with up to nine edge or level sensitive external interrupt pins make these microcontrollers particularly suitable for industrial control and medical systems.

2. Features

2.1 Key features

- 16-bit/32-bit ARM7TDMI-S microcontroller in a tiny LQFP48 package.
- 2 kB/4 kB/8 kB of on-chip static RAM and 8 kB/16 kB/32 kB of on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 70 MHz operation.
- ISP/IAP via on-chip bootloader software. Single flash sector or full chip erase in 100 ms and programming of 256 bytes in 1 ms.
- EmbeddedICE RT offers real-time debugging with the on-chip RealMonitor software.
- The 10-bit A/D converter provides eight analog inputs, with conversion times as low as 2.44 µs per channel and dedicated result registers to minimize interrupt overhead.
- Two 32-bit timers/external event counters with combined seven capture and seven compare channels.
- Two 16-bit timers/external event counters with combined three capture and seven compare channels.
- Low power Real-Time Clock (RTC) with independent power and dedicated 32 kHz clock input.
- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-buses (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.

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- Vectored interrupt controller with configurable priorities and vector addresses.
- Up to thirty-two 5 V tolerant fast general purpose I/O pins.
- Up to 13 edge or level sensitive external interrupt pins available.
- 70 MHz maximum CPU clock available from programmable on-chip PLL with a possible input frequency of 10 MHz to 25 MHz and a settling time of 100 µs.
- On-chip integrated oscillator operates with an external crystal in the range from 1 MHz to 25 MHz.
- Power saving modes include Idle mode, Power-down mode with RTC active, and Power-down mode.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or RTC.

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
LPC2101FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2102FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2103FBD48	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
LPC2103FA44	PLCC44	plastic leaded chip carrier; 44 leads	SOT187-2

3.1 Ordering options

Table 2: Ordering options

Type number	Flash memory	RAM	ADC	Temperature range (°C)
LPC2101FBD48	8 kB	2 kB	8 inputs	–40 to +85
LPC2102FBD48	16 kB	4 kB	8 inputs	–40 to +85
LPC2103FBD48	32 kB	8 kB	8 inputs	–40 to +85
LPC2103FA44	32 kB	8 kB	8 inputs	–40 to +85

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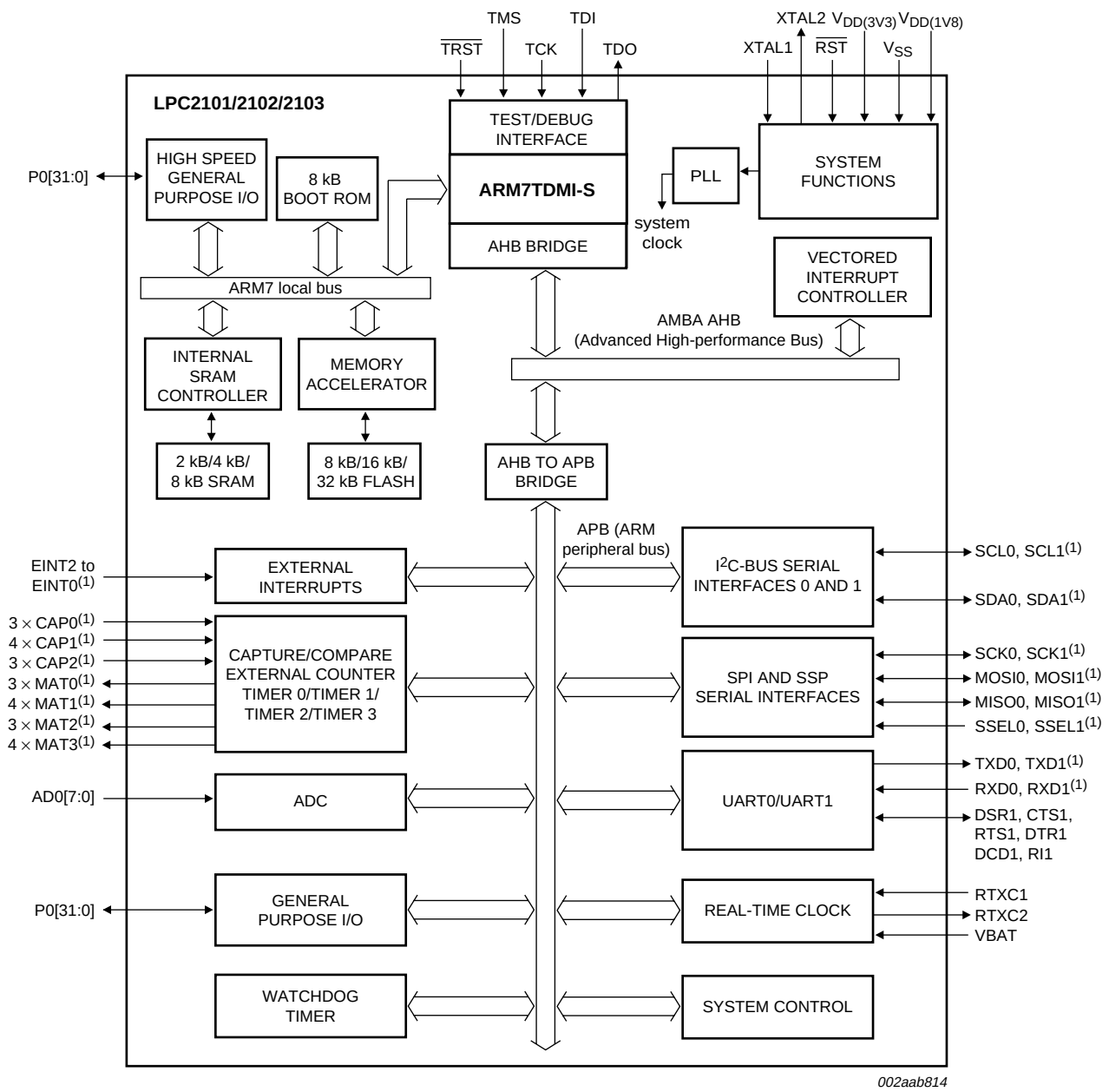
4. Block diagram



(1) Pins shared with GPIO.

Fig 1. Block diagram

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5. Pinning information

5.1 Pinning

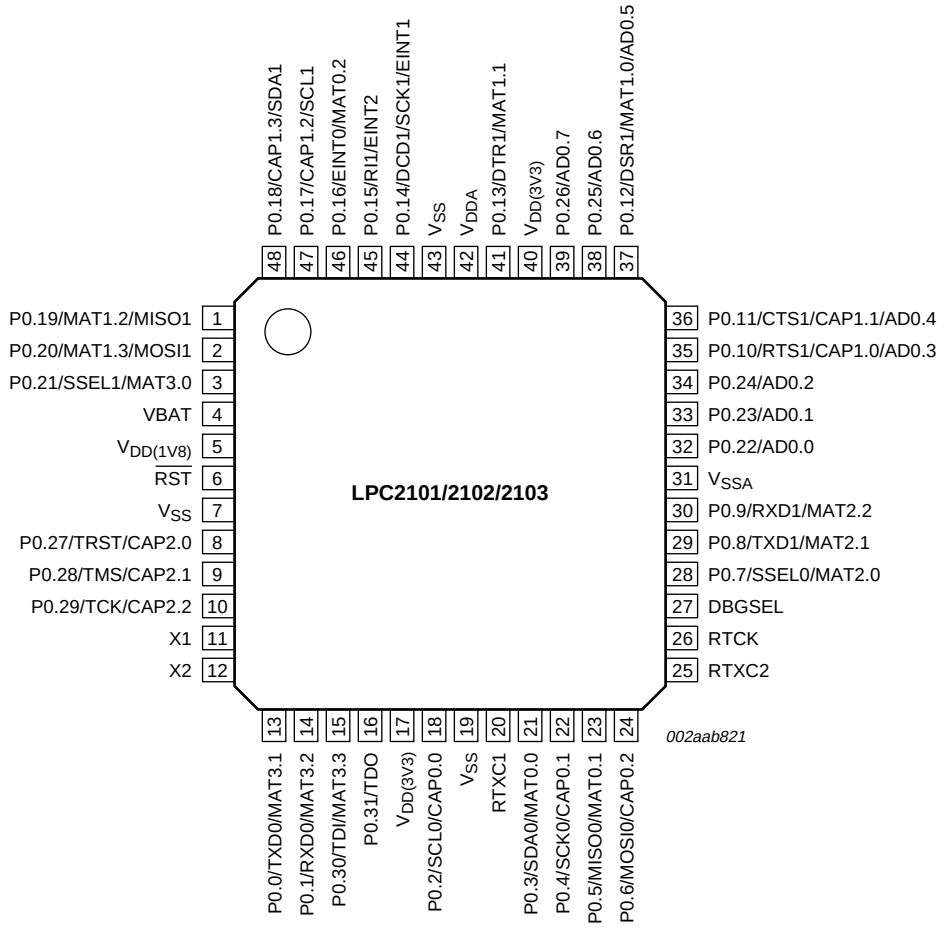

Fig 2. LQFP48 pin configuration

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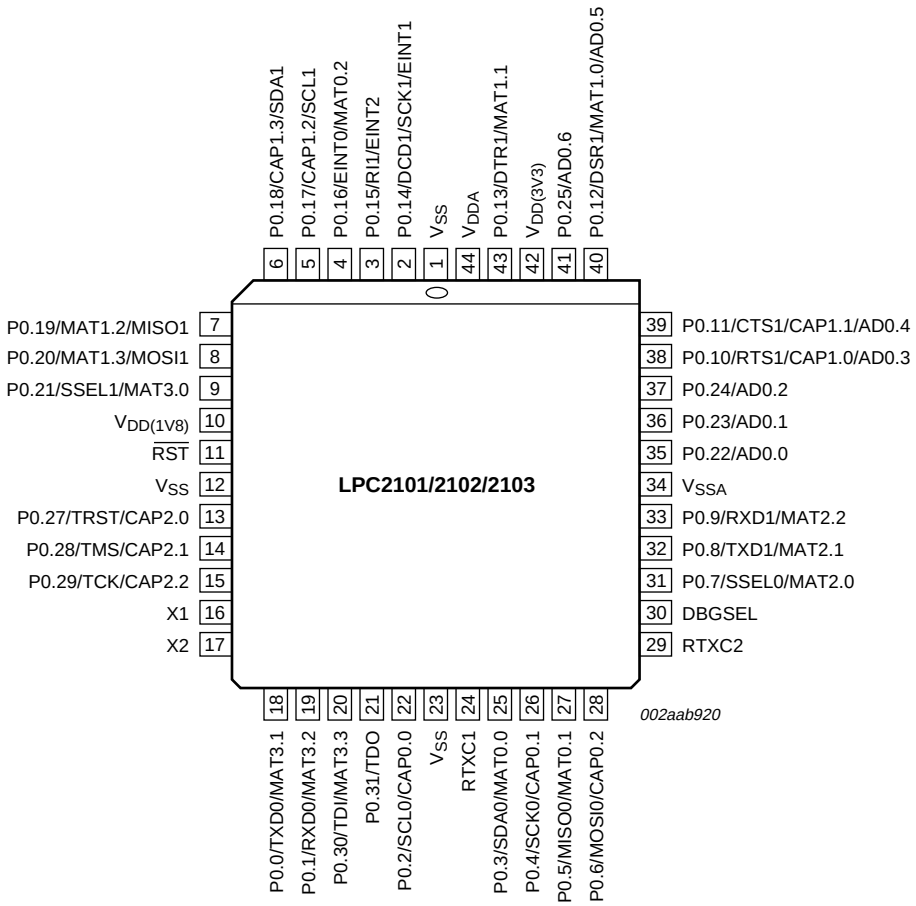

Fig 3. PLCC44 pin configuration

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5.2 Pin description

Table 3: Pin description

Symbol	LQFP48	PLCC44	Type	Description
P0.0 to P0.31			I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. A total of 31 pins of the Port 0 can be used as general purpose bidirectional digital I/Os while P0.31 is an output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0.0/TXD0/ MAT3.1	13 [1]	18 [1]	I/O	**P0.0 —** General purpose Input/output digital pin (GPIO).
			O	**TXD0 —** Transmitter output for UART0.
			O	**MAT3.1 —** PWM output 1 for Timer 3.
P0.1/RXD0/ MAT3.2	14 [2]	19 [2]	I/O	**P0.1 —** General purpose Input/output digital pin (GPIO).
			I	**RXD0 —** Receiver input for UART0.
			O	**MAT3.2 —** PWM output 2 for Timer 3.
P0.2/SCL0/ CAP0.0	18 [3]	22 [3]	I/O	**P0.2 —** General purpose Input/output digital pin (GPIO).
			I/O	**SCL0 —** I^2C0 clock Input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0	21 [3]	25 [3]	I/O	**P0.3 —** General purpose Input/output digital pin (GPIO).
			I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0.0 —** PWM output for Timer 0, channel 0.
P0.4/SCK0/ CAP0.1	22 [4]	26 [4]	I/O	**P0.4 —** General purpose Input/output digital pin (GPIO).
			I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0.1 —** Capture input for Timer 0, channel 1.
P0.5/MISO0/ MAT0.1	23 [4]	27 [4]	I/O	**P0.5 —** General purpose Input/output digital pin (GPIO).
			I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0.1 —** PWM output for Timer 0, channel 1.
P0.6/MOSI0/ CAP0.2	24 [4]	28 [4]	I/O	**P0.6 —** General purpose Input/output digital pin (GPIO).
			I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.7/SSEL0/ MAT2.0	28 [2]	31 [2]	I/O	**P0.7 —** General purpose Input/output digital pin (GPIO).
			I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**MAT2.0 —** PWM output for Timer 2, channel 0.
P0.8/TXD1/ MAT2.1	29 [4]	32 [4]	I/O	**P0.8 —** General purpose Input/output digital pin (GPIO).
			O	**TXD1 —** Transmitter output for UART1.
			O	**MAT2.1 —** PWM output for Timer 2, channel 1.
P0.9/RXD1/ MAT2.2	30 [2]	33 [2]	I/O	**P0.9 —** General purpose Input/output digital pin (GPIO).
			I	**RXD1 —** Receiver input for UART1.
			O	**MAT2.2 —** PWM output for Timer 2, channel 2.

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Table 3: Pin description *...continued*

Symbol	LQFP48	PLCC44	Type	Description
P0.10/RTS1/ CAP1.0/AD0.3	35 [4]	38 [4]	I/O	**P0.10 —** General purpose Input/output digital pin (GPIO).
			O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1.0 —** Capture input for Timer 1, channel 0.
			I	**AD0.3 —** ADC 0, input 3.
P0.11/CTS1/ CAP1.1/AD0.4	36 [3]	39 [3]	I/O	**P0.11 —** General purpose Input/output digital pin (GPIO).
			I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1.1 —** Capture input for Timer 1, channel 1.
			I	**AD0.4 —** ADC 0, input 4.
P0.12/DSR1/ MAT1.0/AD0.5	37 [4]	40 [4]	I/O	**P0.12 —** General purpose Input/output digital pin (GPIO).
			I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1.0 —** PWM output for Timer 1, channel 0.
			I	**AD0.5 —** ADC 0, input 5.
P0.13/DTR1/ MAT1.1	41 [4]	43 [4]	I/O	**P0.13 —** General purpose Input/output digital pin (GPIO).
			O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1.1 —** PWM output for Timer 1, channel 1.
P0.14/DCD1/ SCK1/EINT1	44 [3]	2 [3]	I/O	**P0.14 —** General purpose Input/output digital pin (GPIO).
			I	**DCD1 —** Data Carrier Detect input for UART1.
			I/O	**SCK1 —** Serial Clock for SPI1. SPI clock output from master or input to slave.
			I	**EINT1 —** External interrupt 1 input.
P0.15/RI1/ EINT2	45 [4]	3 [4]	I/O	**P0.15 —** General purpose Input/output digital pin (GPIO).
			I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0.16/EINT0/ MAT0.2	46 [2]	4 [2]	I/O	**P0.16 —** General purpose Input/output digital pin (GPIO).
			I	**EINT0 —** External interrupt 0 input.
			O	**MAT0.2 —** PWM output for Timer 0, channel 2.
P0.17/CAP1.2/ SCL1	47 [1]	5 [1]	I/O	**P0.17 —** General purpose Input/output digital pin (GPIO).
			I	**CAP1.2 —** Capture input for Timer 1, channel 2.
			I/O	**SCL1 —** I^2C1 clock Input/output. Open-drain output (for I^2C-bus compliance).
P0.18/CAP1.3/ SDA1	48 [1]	6 [1]	I/O	**P0.18 —** General purpose Input/output digital pin (GPIO).
			I	**CAP1.3 —** Capture input for Timer 1, channel 3.
			I/O	**SDA1 —** I^2C1 data Input/output. Open-drain output (for I^2C-bus compliance).
P0.19/MAT1.2/ MISO1	1 [1]	7 [1]	I/O	**P0.19 —** General purpose Input/output digital pin (GPIO).
			O	**MAT1.2 —** PWM output for Timer 1, channel 2.
			I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
P0.20/MAT1.3/ MOSI1	2 [2]	8 [2]	I/O	**P0.20 —** General purpose Input/output digital pin (GPIO).
			O	**MAT1.3 —** PWM output for Timer 1, channel 3.
			I/O	**MOSI1 —** Master Out Slave for SSP. Data output from SSP master or data input to SSP slave.

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Table 3: Pin description *...continued*

Symbol	LQFP48	PLCC44	Type	Description
P0.21/SSEL1/ MAT3.0	3 [4]	9 [4]	I/O	**P0.21 —** General purpose Input/output digital pin (GPIO).
			I	**SSEL1 —** Slave Select for SPI1. Selects the SPI interface as a slave.
			O	**MAT3.0 —** PWM output for Timer 3, channel 0.
P0.22/AD0.0	32 [4]	35 [4]	I/O	**P0.22 —** General purpose Input/output digital pin (GPIO).
			I	**AD0.0 —** ADC 0, input 0.
P0.23/AD0.1	33 [1]	36 [1]	I/O	**P0.23 —** General purpose Input/output digital pin (GPIO).
			I	**AD0.1 —** ADC 0, input 1.
P0.24/AD0.2	34 [1]	37 [1]	I/O	**P0.24 —** General purpose Input/output digital pin (GPIO).
			I	**AD0.2 —** ADC 0, input 2.
P0.25/AD0.6	38 [1]	41 [1]	I/O	**P0.25 —** General purpose Input/output digital pin (GPIO).
			I	**AD0.6 —** ADC 0, input 6.
P0.26/AD0.7	39 [1]	n.c.	I/O	**P0.26 —** General purpose Input/output digital pin (GPIO).
			I	**AD0.7 —** ADC 0, input 7.
P0.27/TRST/ CAP2.0	8 [4]	13 [4]	I/O	**P0.27 —** General purpose Input/output digital pin (GPIO).
			I	**TRST —** Test Reset for JTAG interface.
			I	**CAP2.0 —** Capture input for Timer 2, channel 0.
P0.28/TMS/ CAP2.1	9 [4]	14 [4]	I/O	**P0.28 —** General purpose Input/output digital pin (GPIO).
			I	**TMS —** Test Mode Select for JTAG interface.
			I	**CAP2.1 —** Capture input for Timer 2, channel 1.
P0.29/TCK/ CAP2.2	10 [4]	15 [4]	I/O	**P0.29 —** General purpose Input/output digital pin (GPIO).
			I	**TCK —** Test Clock for JTAG interface.
			I	**CAP2.2 —** Capture input for Timer 2, channel 2.
P0.30/TDI/ MAT3.3	15 [4]	20 [4]	I/O	**P0.30 —** General purpose Input/output digital pin (GPIO).
			I	**TDI —** Test Data In for JTAG interface.
			O	**MAT3.3 —** PWM output 3 for Timer 3.
P0.31/TDO	16 [4]	21 [4]	O	**P0.31 —** General purpose output only digital pin (GPIO).
			O	**TDO —** Test Data Out for JTAG interface.
RTXC1	20 [5]	24 [5]	I	Input to the RTC oscillator circuit.
RTXC2	25 [5]	29 [5]	O	Output from the RTC oscillator circuit.
RTCK	26 [5]	n.c.	I/O	**Returned test clock output:** Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up.
X1	11	16	I	Input to the oscillator circuit and internal clock generator circuits.
X2	12	17	O	Output from the oscillator amplifier.
DBGSEL	27	30	I	**Debug select:** When LOW, the part operates normally. When HIGH, debug mode is entered. Input with internal pull-down.
$\overline{RST}$	6	11	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
V_{SS}	7, 19, 43	1, 12, 23	I	**Ground:** 0 V reference.

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Table 3: Pin description *...continued*

Symbol	LQFP48	PLCC44	Type	Description
V_{SSA}	31	34	I	**Analog ground:** 0 V reference. This should be nominally the same voltage as V_{SS} but should be isolated to minimize noise and error.
V_{DDA}	42	44	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the on-chip PLL. This pin also provides a voltage reference level for the ADC.
$V_{DD(1V8)}$	5	10	I	**1.8 V core power supply:** This is the power supply voltage for internal circuitry.
$V_{DD(3V3)}$	17, 40	42	I	**3.3 V pad power supply:** This is the power supply voltage for the I/O ports.
VBAT	4	n.c.	I	**RTC power supply:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] Pad provides special analog functionality.

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6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The particular flash implementation in the LPC2101/2102/2103 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30 % over Thumb mode.

6.2 On-chip flash program memory

The LPC2101/2102/2103 incorporate a 8 kB, 16 kB or 32 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. The entire flash memory is available for user code as the bootloader resides in a separate memory.

The LPC2101/2102/2103 flash memory provides a minimum of 100,000 erase/write cycles and 20 years of data-retention memory.

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6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bits, 16-bits, and 32-bits. The LPC2101/2102/2103 provide 2 kB, 4 kB or 8 kB of static RAM.

6.4 Memory map

The LPC2101/2102/2103 memory map incorporates several distinct regions, as shown in Figure 4.

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.17 “System control”.

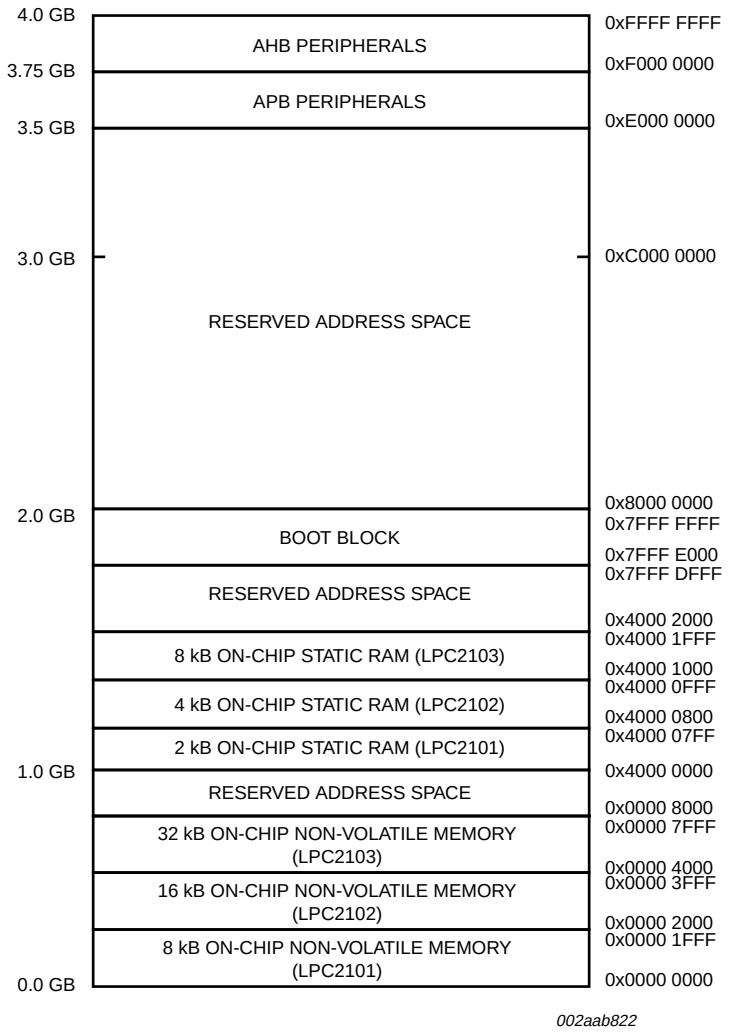

Fig 4. LPC2101/2102/2103 memory map

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6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as FIQ, vectored IRQ, and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

After reset all pins of Port 0 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their JTAG functionality. The pins associated with the I^2C0 interface are open-drain.

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6.7 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2101/2102/2103 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit A/D converter

The LPC2101/2102/2103 contain one analog to digital converter. It is a single 10-bit successive approximation analog to digital converter with eight channels.

6.8.1 Features

- Measurement range of 0 V to 3.3 V.
- Each converter capable of performing more than 400,000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Every analog input has a dedicated result register to reduce interrupt overhead.

6.9 UARTs

The LPC2101/2102/2103 each contain two UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2101/2102/2103 include a fractional baud rate generator for both UARTs. Standard baud rates such as 115200 can be achieved with any crystal frequency above 2 MHz.

6.9.1 Features

- 16 byte Receive and Transmit FIFOs.
- Register locations conform to ‘550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes

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- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.10 I^2C-bus serial I/O controllers

The LPC2101/2102/2103 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., LCD driver) or a transmitter with the capability to both receive and send information such as serial memory. Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2101/2102/2103 supports bit rates up to 400 kbit/s (Fast I^2C).

6.10.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can also be used for test and diagnostic purposes.

6.11 SPI serial I/O controller

The LPC2101/2102/2103 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends 8 bits to 16 bits of data to the slave, and the slave always sends 8 bits to 16 bits of data to the master.

6.11.1 Features

- Compliant with SPI specification.
- Synchronous, Serial, Full Duplex, Communication.

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- Combined SPI master and slave.
- Maximum data bit rate of one eighth of the input clock rate.

6.12 SSP serial I/O controller

The LPC2101/2102/2103 each contain one SSP. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. However, only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with data frames of 4 bits to 16 bits flowing from the master to the slave and from the slave to the master. Often only one of these data streams carries meaningful data.

6.12.1 Features

- Compatible with Motorola SPI, 4-wire TI's SSI and National Semiconductor's Microwire buses.
- Synchronous Serial Communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four bits to 16 bits per frame.

6.13 General purpose 32-bit timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

The LPC2101/2102/2103 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

6.13.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- External event counter or timer operation.
- Four 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.

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- Set HIGH on match.
- Toggle on match.
- Do nothing on match.

6.14 General purpose 16-bit timers/external event counters

The Timer/Counter is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes three capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with ‘or’ and ‘and’, as well as ‘broadcast’ functions among them.

The LPC2101/2102/2103 can count external events on one of the capture inputs if the minimum external pulse is equal or longer than a period of the PCLK. In this configuration, unused capture lines can be selected as regular timer capture inputs or used as external interrupts.

6.14.1 Features

- Two 16-bit timer/counters with a programmable 16-bit prescaler.
- External event counter or timer operation.
- Three 16-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.15 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

6.15.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.

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- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{PCLK} \times 256 \times 4$) to ($T_{PCLK} \times 2^{32} \times 4$) in multiples of $T_{PCLK} \times 4$.

6.16 Real-time clock

The Real-Time Clock (RTC) is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.16.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable Reference Clock Divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.17 System control

6.17.1 Crystal oscillator

On-chip integrated oscillator operates with external crystal in range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.17.2 “PLL” for additional information.

6.17.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 70 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 µs.

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6.17.3 Reset and wake-up timer

Reset has two sources on the LPC2101/2102/2103: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the wake-up timer (see wake-up timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined reset values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up timer.

The wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.17.4 Code security

This feature of the LPC2101/2102/2103 allow an application to control whether it can be debugged or protected from observation.

If after reset on-chip bootloader detects a valid checksum in flash and reads 0x8765 4321 from address 0x1FC in flash, debugging will be disabled and thus the code in flash will be protected from observation. Once debugging is disabled, it can only be enabled by performing a full chip erase using the ISP.

6.17.5 External interrupt inputs

The LPC2101/2102/2103 include up to three edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as three independent interrupt signals. The External Interrupt Inputs can optionally be used to wake-up the processor from Power-down mode.

Additionally all 10 capture input pins can also be used as external interrupts without the option to wake the device up from Power-down mode.

6.17.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

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6.17.7 Power control

The LPC2101/2102/2103 supports two reduced power modes: Idle mode and Power-down mode.

In Idle mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

Selecting an external 32 kHz clock instead of the PCLK as a clock-source for the on-chip RTC will enable the microcontroller to have the RTC active during Power-down mode. Power-down current is increased with RTC active. However, it is significantly lower than in Idle mode.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings during active and Idle mode.

6.17.8 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.18 Emulation and debugging

The LPC2101/2102/2103 support emulation and debugging via a JTAG serial port.

6.18.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even

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entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

6.18.2 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC, which is present in the EmbeddedICE logic. The LPC2101/2102/2103 contain a specific configuration of RealMonitor software programmed into the on-chip boot ROM memory.

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7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			–0.5	4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		–0.5	4.6	V
V_{IA}	analog input voltage		[4]	–0.5	5.1	V
V_I	input voltage	5 V tolerant I/O pins	[5] [6]	–0.5	6.0	V
		other I/O pins	[5]	–0.5	V_{DD} + 0.5 [7]	V
I_{DD}	supply current		[8]	-	100 [9]	mA
I_{SS}	ground current		[10]	-	100 [9]	mA
T_{stg}	storage temperature		[11]	–40	125	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core and internal rail.

[3] External rail.

[4] On ADC related pins.

[5] Including voltage on outputs in 3-state mode.

[6] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[7] Not to exceed 4.6 V.

[8] Per supply pin.

[9] The peak current is limited to 25 times the corresponding maximum current.

[10] Per ground pin.

[11] Dependent on package type.

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8. Static characteristics

Table 5: Static characteristics

T_a = –40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3.0	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT			2.0 [4]	3.3	3.6	V
Standard port pins, $\overline{RESET}$, RTCK							
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	$V_I = V_{DD(3V3)}$; no pull-down		-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down		-	-	3	µA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V < (1.5V_{DD(3V3)})$ T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[5] [6] [7]	0	-	5.5	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-state input voltage			2.0	-	-	V
V_{IL}	LOW-state input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-state output voltage	I_{OH} = –4 mA	[8]	$V_{DD(3V3)}$ – 0.4	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = –4 mA	[8]	-	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD(3V3)}$ – 0.4 V	[8]	–4	-	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[8]	4	-	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V	[9]	-	-	–45	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DDA}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [10]		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V	[11]	–15	–50	–85	µA
		$V_{DD(3V3)} < V_I$ < 5 V [10]		0	0	0	µA
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V, T_a = 25 °C, code `while(1){}` executed from flash, no active peripherals CCLK = 10 MHz		**<tbd>**	7	**<tbd>**	mA
		CCLK = 70 MHz (other parameters as above)		**<tbd>**	41	**<tbd>**	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V, T_a = +25 °C		**<tbd>**	7	**<tbd>**	µA
		$V_{DD(1V8)}$ = 1.8 V, T_a = +85 °C		**<tbd>**	**<tbd>**	**<tbd>**	µA

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Table 5: Static characteristics *...continued*

T_a = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
I_{BATpd}	Power-down mode battery supply current [12]	RTC clock = 32 kHz (from RTXC pins), T_a = +25 °C					
		$V_{DD(1V8)}$ = 1.8 V, VBAT = 2.5 V		-	7	<tbd>	µA
		$V_{DD(1V8)}$ = 1.8 V, VBAT = 3.0 V		-	8	<tbd>	µA
I_{BATact}	active mode battery supply current [12]	CCLK = 70 MHz, PCLK = 17.5 MHz, PCLK enabled to RTCK, RTC clock = 32 kHz (from RTXC pins), T_a = +25 °C					
		$V_{DD(1V8)}$ = 1.8 V, VBAT = 3.0 V		<tbd>	<tbd>	<tbd>	µA
I^2C-bus pins							
V_{IH}	HIGH-state input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-state input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.5V_{DD(3V3)}$	-	V
V_{OL}	LOW-state output voltage	I_{OLS} = 3 mA	[8]	-	-	0.4	V
I_{LI}	input leakage current [13]	$V_I = V_{DD(3V3)}$		-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			0	-	1.8	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			0	-	1.8	V
$V_{i(RTXC1)}$	input voltage on pin RTXC1			0	-	1.8	V
$V_{o(RTXC2)}$	output voltage on pin RTXC2			0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Core and internal rail.

[3] External rail.

[4] The RTC typically fails when VBAT drops below 1.6 V.

[5] Including voltage on outputs in 3-state mode.

[6] $V_{DD(3V3)}$ supply voltages must be present.

[7] 3-state outputs go into 3-state mode when $V_{DD(3V3)}$ is grounded.

[8] Accounts for 100 mV voltage drop in all supply lines.

[9] Only allowed for a short time period.

[10] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[11] Applies to P1.25:16.

[12] On pin VBAT.

[13] To V_{SS}.

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Table 6: ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_a = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1] [2] [3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1] [4]	-	-	±2	LSB
E_O	offset error		[1] [5]	-	-	±3	LSB
E_G	gain error		[1] [6]	-	-	±0.5	%
E_T	absolute error		[1] [7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The A/D is monotonic, there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 5.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 5.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 5.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 5.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated A/D and the ideal transfer curve. See Figure 5.

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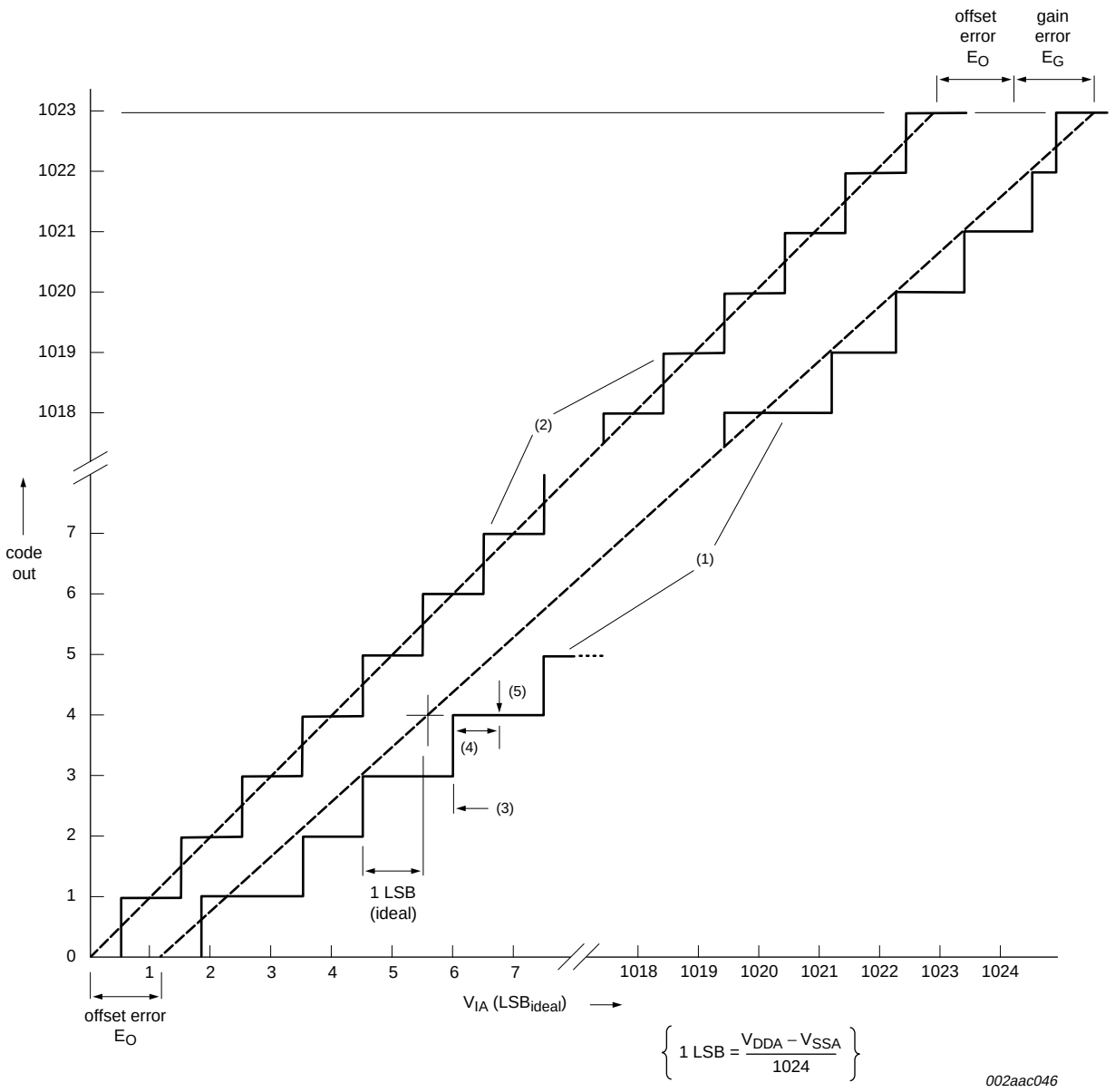

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. A/D conversion characteristics

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9. Dynamic characteristics

Table 7: Dynamic characteristics

T_a = 0 °C to +70 °C for commercial applications, −40 °C to +85 °C for industrial applications, $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges [1]

Symbol	Parameter	Conditions	Min	Typ [2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2 and P0.3)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2 and P0.3)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$ [3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

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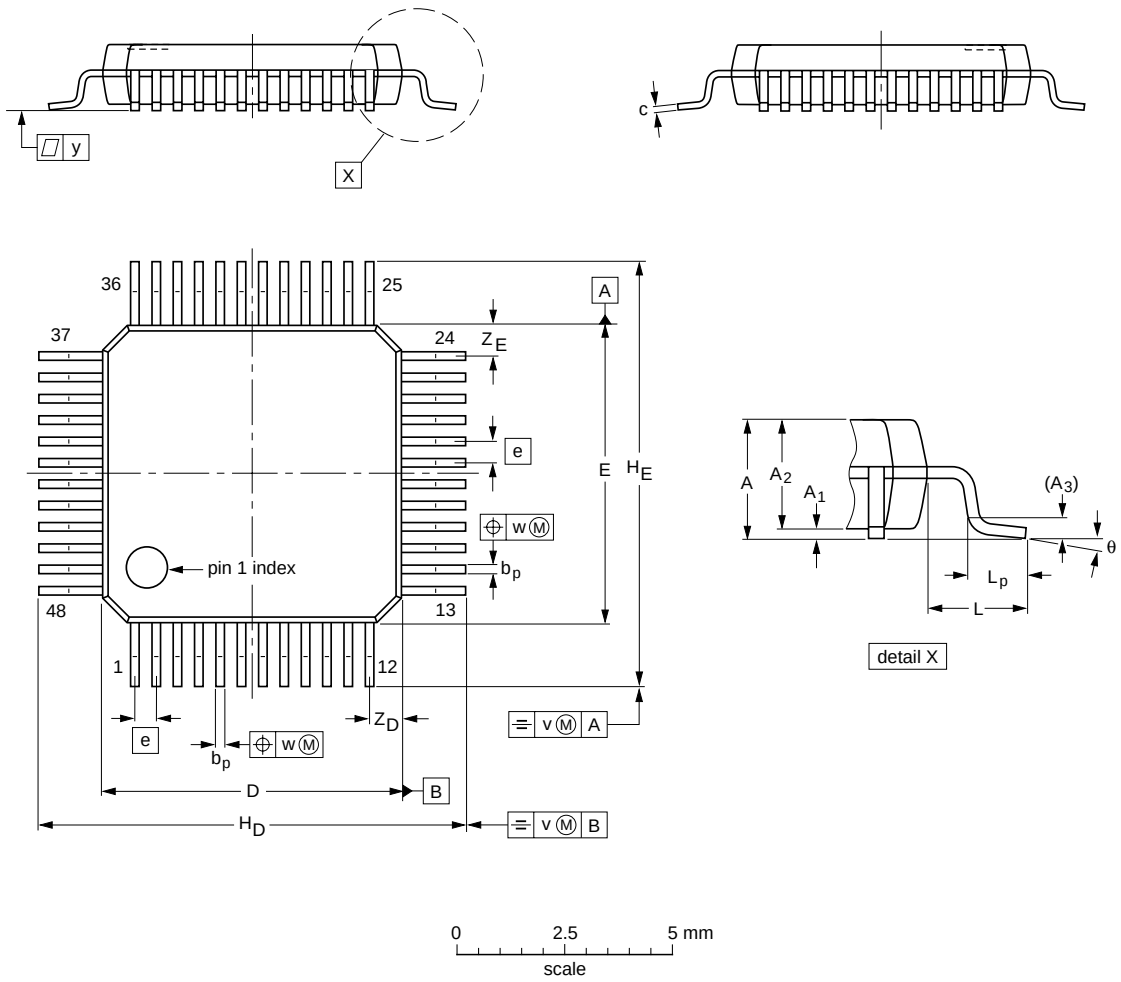
10. Package outline

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT313-2	136E05	MS-026				~~00-01-19~~ 03-02-25

Fig 6. Package outline SOT313-2 (LQFP48)

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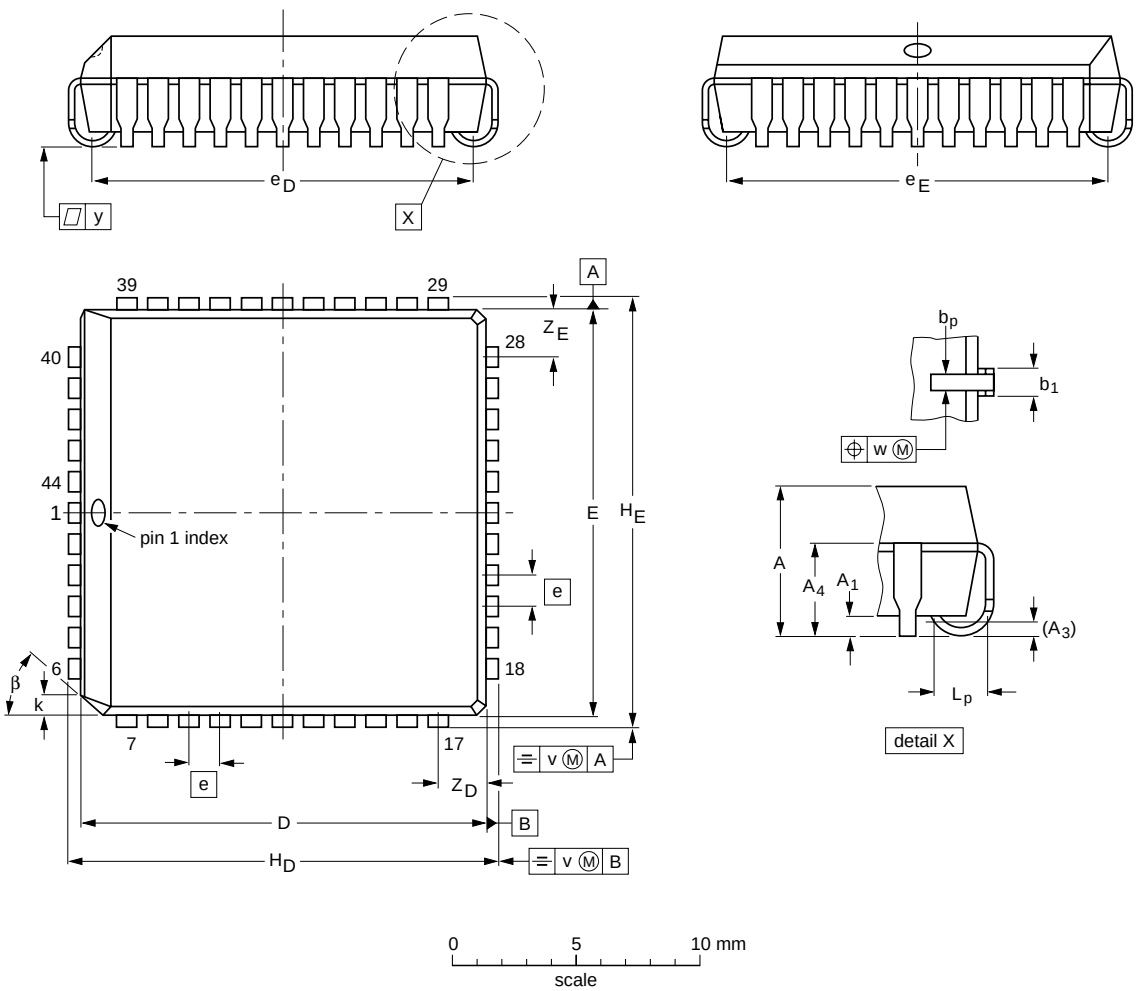
PLCC44: plastic leaded chip carrier; 44 leads **SOT187-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	D(1)	E(1)	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	Z_D(1) max.	Z_E(1) max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.63 0.59	0.63 0.59	0.695 0.685	0.695 0.685	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT187-2	112E10	MS-018	EDR-7319			~~99-12-27~~ 01-11-14

Fig 7. Package outline SOT187-2 (PLCC44)

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11. Abbreviations

Table 8: Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
DCC	Debug Communications Channel
DSP	Digital Signal Processor
FIFO	First In, First Out
FIQ	Fast Interrupt Request
GPIO	General Purpose Input/Output
IAP	In-Application Programming
IRQ	Interrupt Request
ISP	In-System Programming
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSP	Serial Synchronous Port
UART	Universal Asynchronous Receiver/Transmitter
VIC	Vectored Interrupt Controller

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12. Revision history

Table 9: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
LPC2101_2102_2103_1	20060118	Preliminary data sheet	-	-	-

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13. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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18. Contents

1 General description . . . 1
2 Features . . . 1
2.1 Key features . . . 1
3 Ordering information . . . 2
3.1 Ordering options . . . 2
4 Block diagram . . . 3
5 Pinning information . . . 4
5.1 Pinning . . . 4
5.2 Pin description . . . 6
6 Functional description . . . 10
6.1 Architectural overview . . . 10
6.2 On-chip flash program memory . . . 10
6.3 On-chip static RAM . . . 11
6.4 Memory map . . . 11
6.5 Interrupt controller . . . 12
6.5.1 Interrupt sources . . . 12
6.6 Pin connect block . . . 12
6.7 Fast general purpose parallel I/O . . . 13
6.7.1 Features . . . 13
6.8 10-bit A/D converter . . . 13
6.8.1 Features . . . 13
6.9 UARTs . . . 13
6.9.1 Features . . . 13
6.10 I^2C-bus serial I/O controllers . . . 14
6.10.1 Features . . . 14
6.11 SPI serial I/O controller . . . 14
6.11.1 Features . . . 14
6.12 SSP serial I/O controller . . . 15
6.12.1 Features . . . 15
6.13 General purpose 32-bit timers/external event counters . . . 15
6.13.1 Features . . . 15
6.14 General purpose 16-bit timers/external event counters . . . 16
6.14.1 Features . . . 16
6.15 Watchdog timer . . . 16
6.15.1 Features . . . 16
6.16 Real-time clock . . . 17
6.16.1 Features . . . 17
6.17 System control . . . 17
6.17.1 Crystal oscillator . . . 17
6.17.2 PLL . . . 17
6.17.3 Reset and wake-up timer . . . 18
6.17.4 Code security . . . 18
6.17.5 External interrupt inputs . . . 18
6.17.6 Memory mapping control . . . 18
6.17.7 Power control . . . 19
6.17.8 APB bus . . . 19
6.18 Emulation and debugging . . . 19
6.18.1 EmbeddedICE . . . 19
6.18.2 RealMonitor . . . 20
7 Limiting values . . . 21
8 Static characteristics . . . 22
9 Dynamic characteristics . . . 26
10 Package outline . . . 27
11 Abbreviations . . . 29
12 Revision history . . . 30
13 Data sheet status . . . 31
14 Definitions . . . 31
15 Disclaimers . . . 31
16 Trademarks . . . 31
17 Contact information . . . 31

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Date of release: 18 January 2006
Document number: LPC2101_02_03_1

Published in the Netherlands