Semiconductor Corporation

CS1232

T-65-13

Micromonitor

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

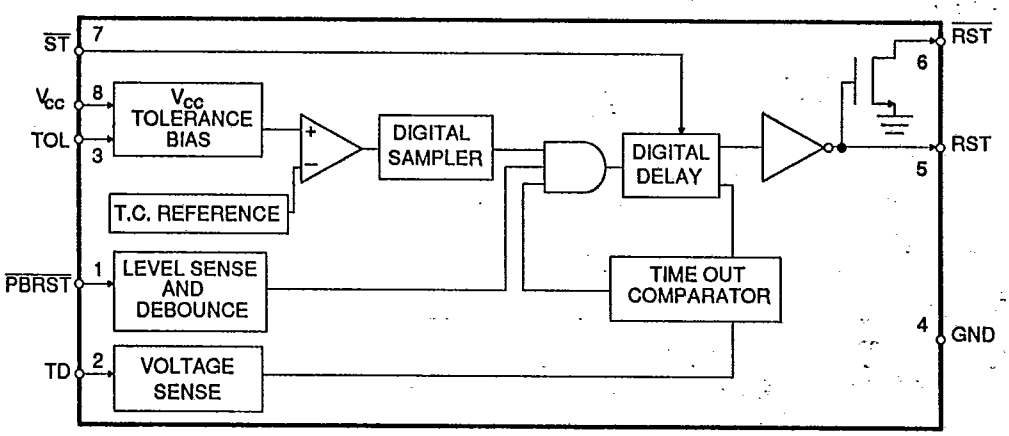
The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232- P	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232- S	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter	Symbol	min	typ	max	Units
V_{CC} Trip Point (TOL = GND) (Note 1)	V_{CCTP}	4.50	4.62	4.74	V
V_{CC} Trip Point (TOL = V_{CC}) (Note 1)	V_{CCTP}	4.25	4.37	4.49	V
Operating Current (Note 2)	I_{CC}	–	0.4	2.0	mA

Notes: 1. All Voltages Referenced To Ground
2. Measured with outputs open

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	min	typ	max	Units
Operating Temperature	CS1232		0	–	+ 70	°C
	CS1232-I		– 40	–	+ 85	°C
Supply Voltage (Note 1)		V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter	Symbol	min	typ	max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)	V_{IH}	2.0	–	V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level (Note 1)	V_{IL}	– 0.3	–	+ 0.8	V
Output High Current @2.4 V RST only	I_{OH}	– 1.0	– 2.0	–	mA
Output Low Current @0.4 V RST, $\overline{RST}$	I_{OL}	2.0	3.0	–	mA
Input Leakage (Note 3)	I_{IL}	– 1.0	–	+ 1.0	uA
Input Capacitance T_A = 25 °C	C_{IN}	–	–	5	pF
Output Capacitance T_A = 25 °C	C_{OUT}	–	–	7	pF

Note: 3. $\overline{PBRST}$ is internally pulled up to Vcc with an internal impedance of 100 kΩ typical.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	min	typ	max	Units
Voltage on any Pin Relative to Ground	– 1.0	–	+7.0	V
Input Current	–	–	±10	mA
Storage Temperature	– 55	–	+125	°C
Soldering Temperature	260 °C for 10 Sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

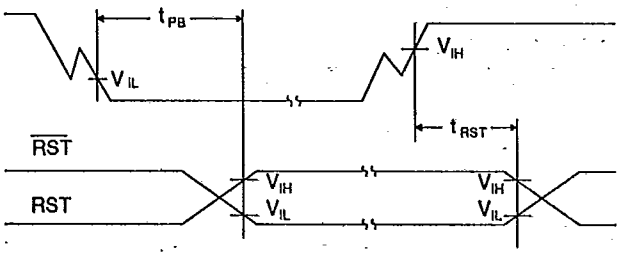
SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	min	typ	max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	20	–	–	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	–	–	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	–	–	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	–	–	us
V_{CC} Detect to RST and $\overline{RST}$ (Note 4)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	–	–	ns
$\overline{ST}$ Pulse Period TD pin at Ground TD pin floating TD pin connected to V_{CC} (Note 5)	t_{TD}	 62.5 250 500	 – – –	 250 1000 2000	 ms ms ms

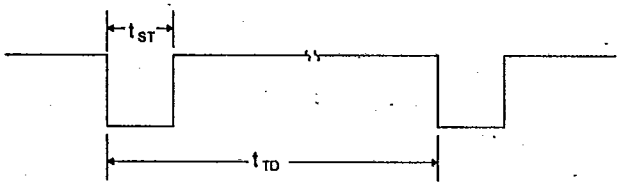
Note: 4. t_R = 5 µs

5. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.

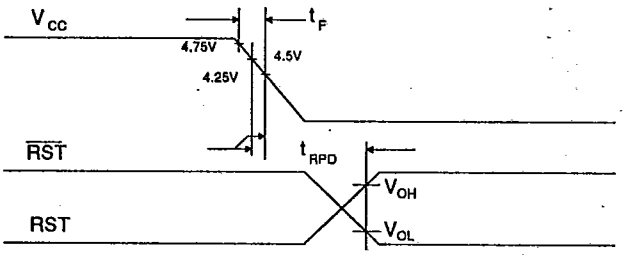
6. $\overline{RST}$ is an N-channel open drain output.



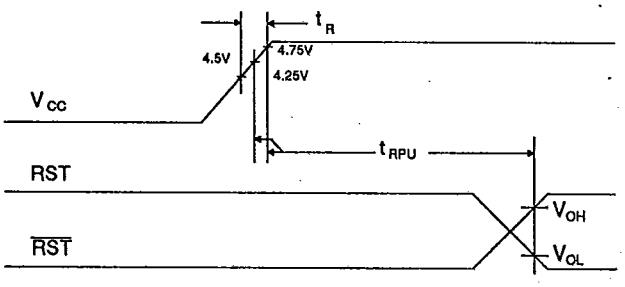
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for V_{CC}; when the V_{CC} level drops below the TOL defined level, the comparator outputs the signals RST and $\overline{RST}$. The threshold level is set to typically 4.37 V if TOL is connected to V_{CC}, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that V_{CC} is valid. Upon return of power, RST and $\overline{RST}$ are active for 250 ms (minimum) to allow stabilization.

PUSHBUTTON RESET CONTROL

$\overline{PBRST}$ is normally connected to a reset pushbutton (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and $\overline{RST}$. The delay begins when $\overline{PBRST}$ is released from from the low state. $\overline{PBRST}$ has an internal 100 kΩ pull-up resistor.

WATCHDOG TIMER

When RST and $\overline{RST}$ become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and $\overline{RST}$ are forced active when $\overline{ST}$ is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms is TD is not connected, or 1.2 seconds with TD connected to V_{CC}. RST and $\overline{RST}$ are driven active for 250 ms (minimum) if no high-to-low transition occurs on the $\overline{ST}$ input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the $\overline{ST}$ input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

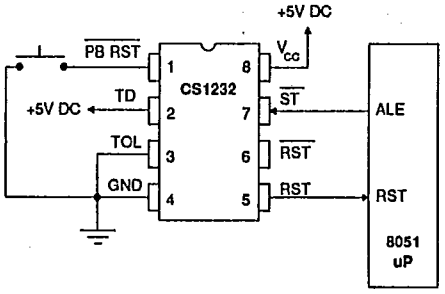


Figure 1. Pushbutton Reset

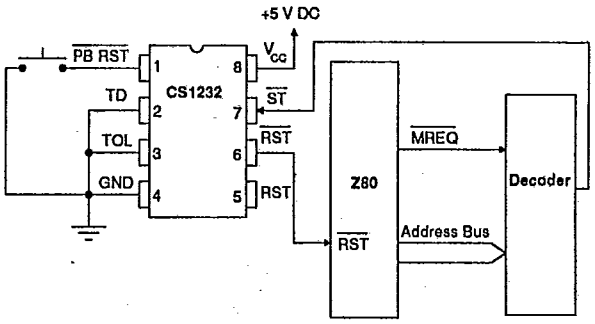


Figure 2. Watchdog Timer

PUSH BUTTON RESET INPUT	$\overline{PBRST}$	1	Vcc	+5 VOLT POWER
TIME DELAY SET	TD	2	$\overline{ST}$	STROBE INPUT
SELECTS Vcc DETECT LEVEL	TOL	3	$\overline{RST}$	RESET OUTPUT (Active Low, Open Drain
GROUND	GND	4	RST	RESET OUTPUT (Active High)

CS1232 (8-pin)

NO CONNECTION	NC	1	NC	NO CONNECT
PUSH BUTTON RESET INPUT	$\overline{PBRST}$	2	Vcc	+5 VOLT POWER
NO CONNECT	NC	3	NC	NO CONNECTION
TIME DELAY SET	TD	4	$\overline{ST}$	STROBE INPUT
NO CONNECT	NC	5	NC	NO CONNECT
SELECTS Vcc DETECT LEVEL	TOL	6	$\overline{RST}$	RESET OUTPUT (Active Low, Open Drain
NO CONNECT	NC	7	NC	NO CONNECT
GROUND	GND	8	RST	RESET OUTPUT (Active High)

CS1232 (16-pin)