BOOST CONVERTER FOR BATTERY BACKUP CHARGING WITH ADJUSTABLE CONSTANT CURRENT AND SNOOZE MODE

Check for Samples: TPS61251

FEATURES

- **Resistor Programmable Input Current Limit**
  - **±10% Current Accuracy at 500mA over Full Temperature Range**
  - **Programmable from 100mA up to 1500mA**
- **Snooze Mode Draws Only 2 μA (typ.) Quiescent Current**
- **Designed to Charge Large Capacitor Values in the Farad Range**
- **Up to 92% Efficiency**
- **Power Good Indicates Appropriate Output Voltage Level even in Shut Down**
- **V_{IN} Range from 2.3V to 6.0V**
- **Adjustable Output Voltage up to 6.5V**
- **100% Duty-Cycle Mode When $V_{IN} > V_{OUT}$**
- **Load Disconnect and Reverse Current Protection**
- **Short Circuit Protection**
- **Typical Operating Frequency 3.5 MHz**
- **Available in a 2×2-mm QFN-8 Package**

APPLICATIONS

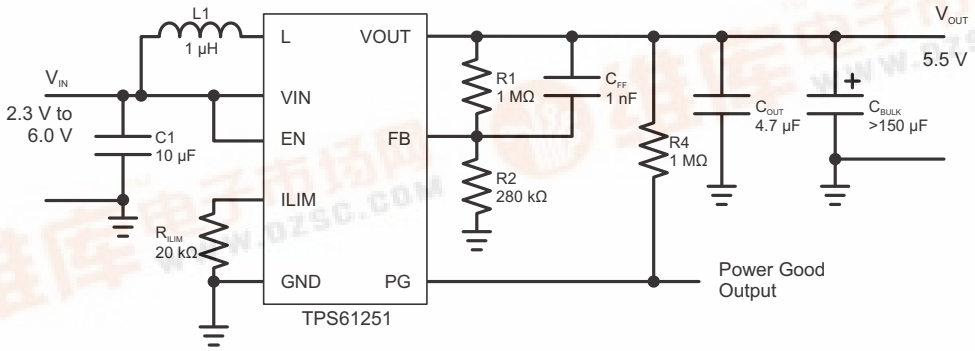
- **Current Limited Applications With High Peak Power Loads (SSD, PCMCIA Tx Bursts, Memory, GPRS/GSM Tx)**
- **Li-Ion Applications**
- **Battery Backup Applications**
- **Audio Applications**
- **RF-PA Buffer**

DESCRIPTION

The TPS61251 device provides a power supply solution for products powered by either a three-cell, NiCd or NiMH battery, or a one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones, solid state drives (SSD) and wireless modems. The converter is designed to charge large capacitors in the Farad range to support battery back up applications. During capacitor charging the TPS61251 is working as a constant current source until V_{OUT} has reached its programmed value. The charge current can be programmed by an external resistor R_{ILIM} and provides a ±10% accuracy for the average input current limit.

The TPS61251 in combination with a reservoir capacitor allows the converter to provide high current pules that would exceed the capability of the suppling circuit (PC slot, USB) and keeps the slot power safely within its capabilities. During light loads the device will automatically enters an enhanced power save mode (Snooze Mode), which allows the converter to maintain the required output voltage, while only drawing 2 μA from the battery. This will allow maximum efficiency at lowest quiescent currents.

TPS61251 allows the use of small inductors and input capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery and will not discharge either the battery nor the charged bulk capacitor. The TPS61251 is available in a 8-pin QFN package measuring 2×2 mm (DSG).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE DEVICE OPTIONS

T_A	OUTPUT VOLTAGE(1)	PACKAGE MARKING	PACKAGE	PART NUMBER(2)
–40°C to 85°C	Adjustable	QTH	8-Pin QFN	TPS61251GSG

(1) Contact TI for other fixed output voltage options
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range(2)	VIN, VOUT, SW, EN, PG, FB, ILIM	–0.3	7	V
Temperature range	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C
ESD rating(3)	Human Body Model - (HBM)		2	kV
	Charge Device Model - (CDM)		0.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61251 DSG 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	80.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	93.5	
θ_{JB}	Junction-to-board thermal resistance	54.2	
ψ_{JT}	Junction-to-top characterization parameter	0.9	
ψ_{JB}	Junction-to-board characterization parameter	59.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	20	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VIN	2.3		6.0	V
Output voltage at VOUT	3.0		6.5	V
Programable input current limit set by R_{ILIM}	100		1500	mA
Operating free air temperature range, T_A	–40		85	°C
Operating junction temperature range, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

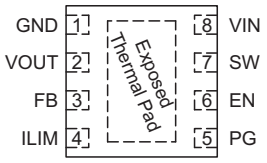
Over recommended free air temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V, V_{OUT} = 5.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC/DC STAGE						
V_{FB}	Feedback voltage		1.182	1.2	1.218	V
	Maximum line regulation	2.3 V ≤ V_{IN} ≤ 6.0 V		0.5		%
	Maximum load regulation			0.5		%
f	Oscillator frequency			3500		kHz
$r_{DS(on)}$	High side switch on resistance			200		mΩ
	Low side switch on resistance			130		mΩ
	Reverse leakage current into V_{OUT}	EN = GND			3.5	µA
$I_{IN(DC)}$	Programmable input average switch current limit	ILIM pin set to V_{IN}		1500		mA
		ILIM pin set to GND		100		mA
		R_{ILIM} = 20 kΩ (500mA)	-10		+10	%
I_Q	Quiescent current	PFM enabled, device is not switching		30		µA
		SNOOZE mode, I_{OUT} = 0 mA, current into V_{IN} pin		2		µA
I_{SD}	Shutdown current (1)	V_{IN} turned on when EN is connected to GND and no voltage is present at V_{OUT}		0.85	3.5	µA
OVP	Input over voltage protection threshold	Falling		6.4		V
		Rising		6.5		V
CONTROL STAGE						
V_{UVLO}	Under voltage lockout threshold	Falling		2.0	2.1	V
		Hysteresis		0.1		V
V_{IL}	EN input low voltage	2.3 V ≤ V_{IN} ≤ 6.0 V			0.4	V
V_{IH}	EN input high voltage	2.3 V ≤ V_{IN} ≤ 6.0 V	1.0			V
	EN, PG input leakage current	Clamped on GND or V_{IN}			0.5	µA
	Power Good threshold voltage	Rising referred to V_{FB}	92.5	95	97.5	%
		Falling referred to V_{OUT}		2.3		V
	Power good delay			50		µs
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

(1) When the power good threshold is triggered the first time a comparator is turned on to observe the output voltage increasing the shutdown current.

DEVICE INFORMATION

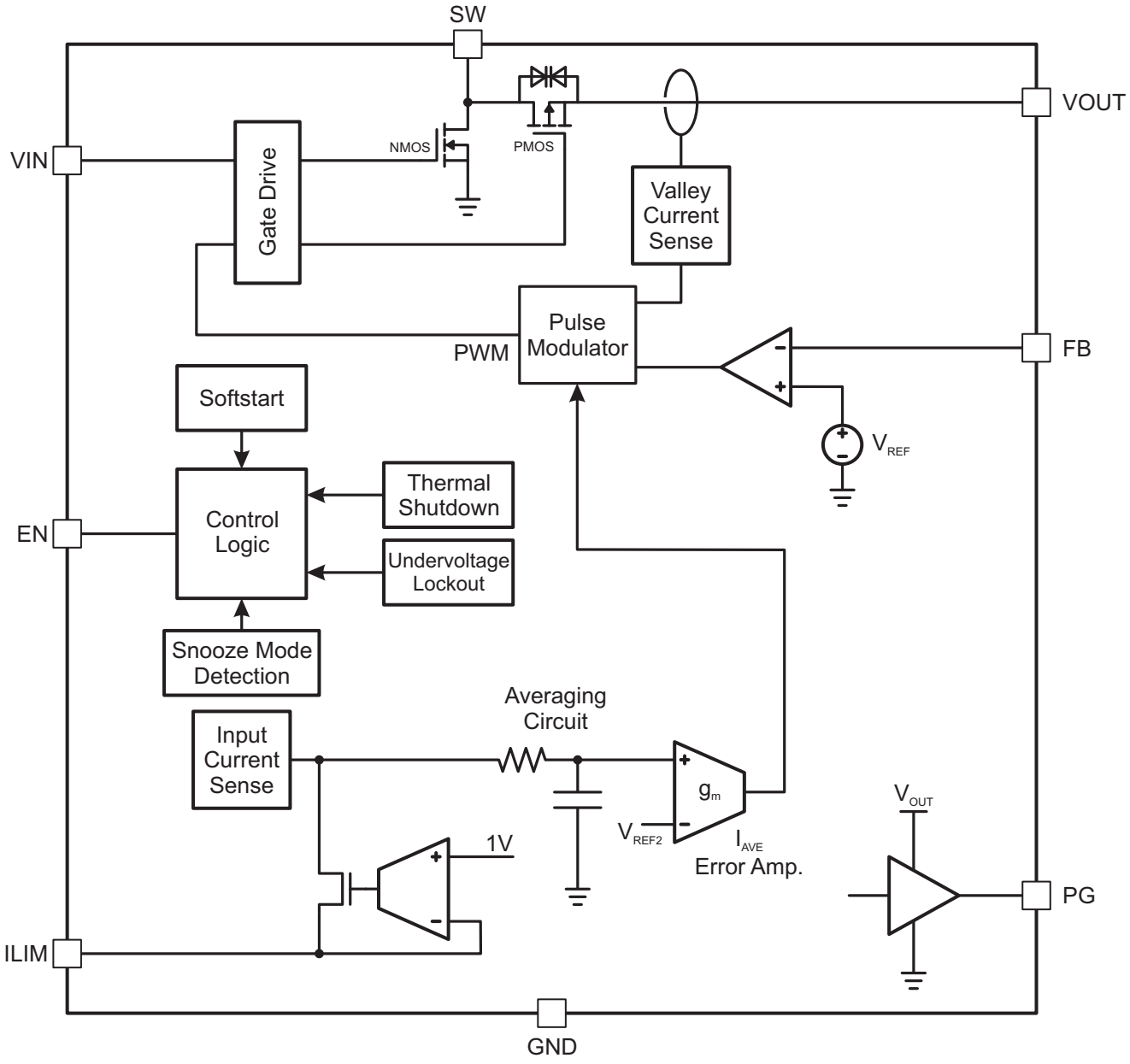
PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	6	I	Enable input. (1 enabled, 0 disabled)
FB	3	I	Voltage feedback pin
GND	1		Ground
ILIM	4	I	Adjustable average input current limit. Can be connected to V_{IN} for maximum current limit or to GND for minimum current limit.
PG	5	O	Output power good (1 good, 0 failure; open drain)
SW	7	I	Connection for Inductor
VIN	8	I	Supply voltage for power stage
VOUT	2	O	Boost converter output
Exposed Thermal Pad			Must be soldered to achieve appropriate power dissipation and for mechanical reasons. Must be connected to GND.

FUNCTIONAL BLOCK DIAGRAM (TPS61251)



PARAMETER MEASUREMENT INFORMATION

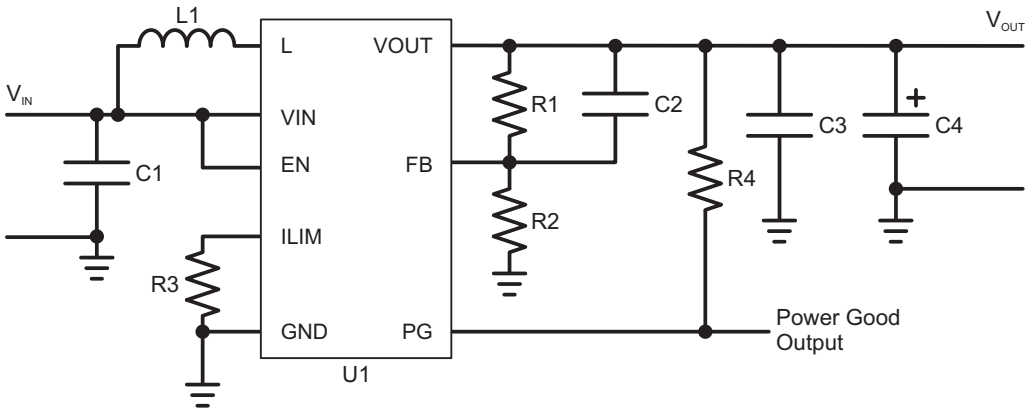


Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
U1	TPS61251	Texas Instruments
L1	1.0 µH, 2.1 A, 27mΩ, 2.8 mm x 2.8 mm x 1.5 mm	DEM2815C, TOKO
C1	1 x 4.7 µF, 10 V, 0805, X7R ceramic	GRM21BR71A475KA73, Murata
C2	1 x 1000 pF, 50 V, 0603, COG ceramic	GRM1885C1H102JA01B, Murata
C3	1 × 4.7 µF, 10 V, 0805, X7R ceramic	GRM21BR71A475KA73, Murata
C4	20 x 100 uF, 6.3 V, 1206, X5R	GRM31CR60J107ME39B, Murata
R1	Depending on the output voltage of TPS61252, 1% (all waveform measurements with 5.5 V output voltage uses 1000 kΩ)	
R2	Depending on the output voltage of TPS61252, 1% (all waveform measurements with 5 V output voltage uses 280 kΩ)	
R3	Depending on the input current limit of TPS61252, 1%	
R4	1 MΩ, 1%	any

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DESCRIPTION		FIGURE
Efficiency	vs Output current (V_{OUT} = 5.5 V, I_{LIM} = 1.5 A, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 1
	vs Output current in 100% Duty-Cycle Mode (V_{OUT} = 5.5V, I_{LIM} = 1.5 A, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 2
	vs Input voltage (V_{OUT} = 5.5V, I_{LOAD} = {0.01;0.1; 1.0; 10; 100; 500 mA}, R1 = 2320 kΩ and R2 = 649 kΩ)	Figure 3
Maximum output current	vs Input voltage (V_{OUT} = 5.5 V, I_{LIM} = {100; 200; 500; 1000; 1500 mA}, R1 = 1000 kΩ and R2 = 280 kΩ)	Figure 4
Output voltage	vs Output current (V_{OUT} = 5.5 V, I_{LIM} = 1.5 A, R1 = 1000 kΩ and R2 = 280 kΩ)	Figure 5
Waveforms	Load transient response (Tantal Capacitor 2.3mF with >60 mΩ ESR, V_{OUT} = 5.5V, V_{IN} = 3.6V, I_{LIM} = 1000mA, Load change from 50 mA to 550 mA)	Figure 6
	Load transient response (6 x 330uF Polymer Tantal <5 mΩ ESR in total, V_{OUT} = 5.5V, V_{IN} = 3.6V, I_{LIM} = 1000mA, Load change from 500 mA to 1500 mA)	Figure 7
	Startup after enable (V_{OUT} = 5.5V, V_{IN} = 3.6V, I_{LIM} = 1000mA)	Figure 8
	Startup after enable (V_{OUT} = 5.5V, V_{IN} = 3.6V, I_{LIM} = 500mA)	Figure 9

EFFICIENCY vs OUTPUT CURRENT

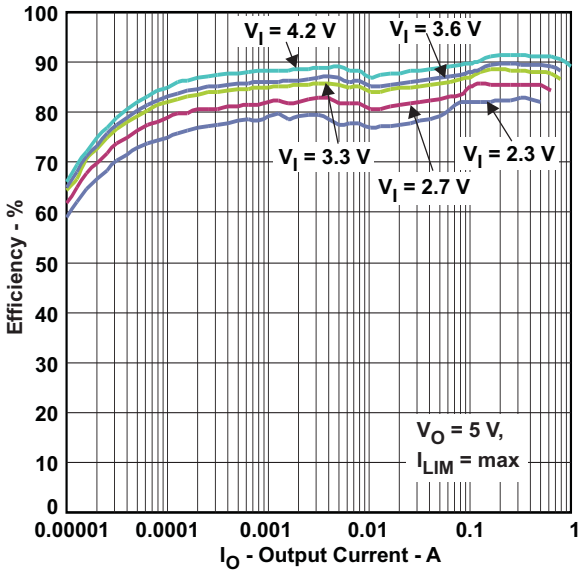


Figure 1.

EFFICIENCY vs OUTPUT CURRENT IN 100% DUTY-CYCLE MODE

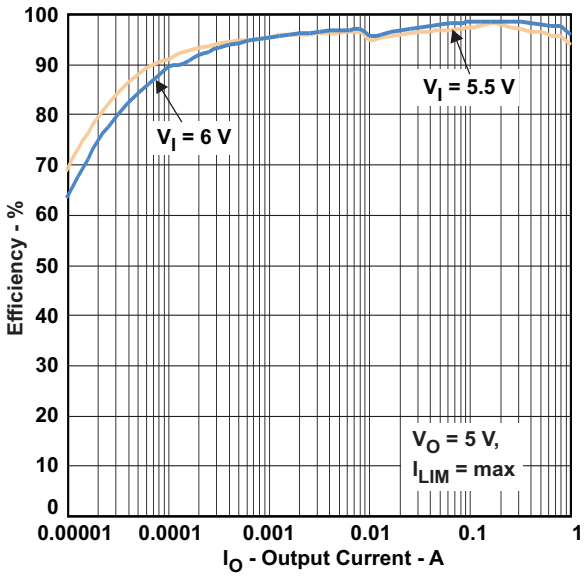


Figure 2.

EFFICIENCY
vs
INPUT VOLTAGE

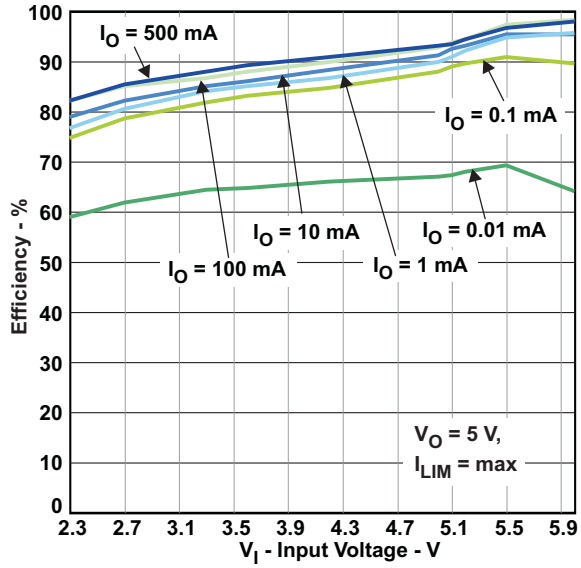


Figure 3.

MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

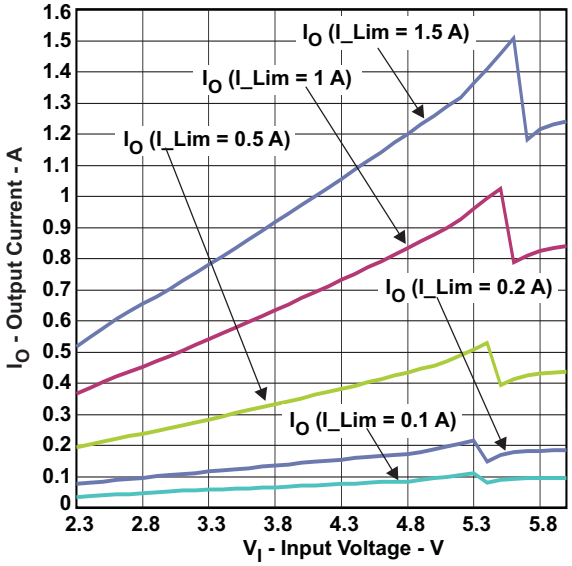


Figure 4.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

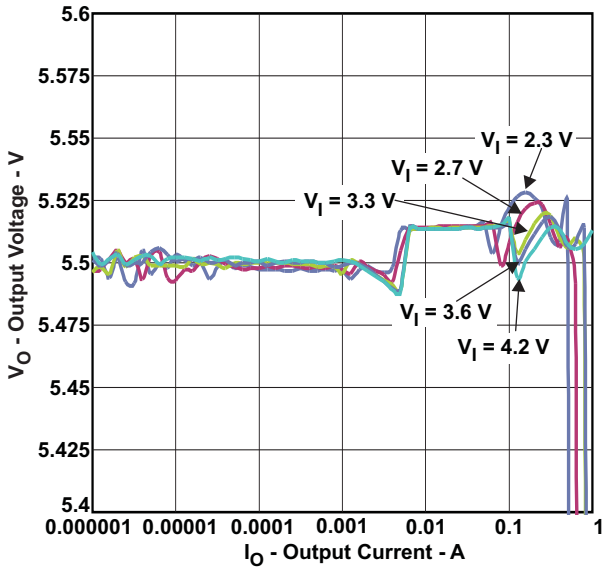


Figure 5.

LOAD TRANSIENT RESPONSE (Tantal Capacitor)

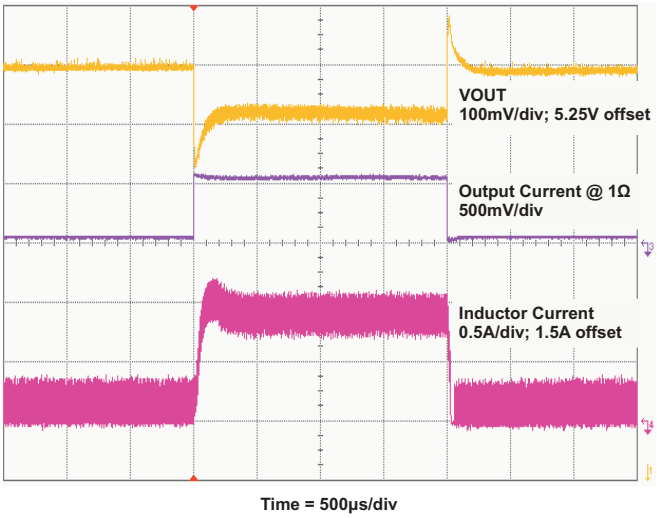


Figure 6.

LOAD TRANSIENT RESPONSE (Low ESR Polymer Tantal)

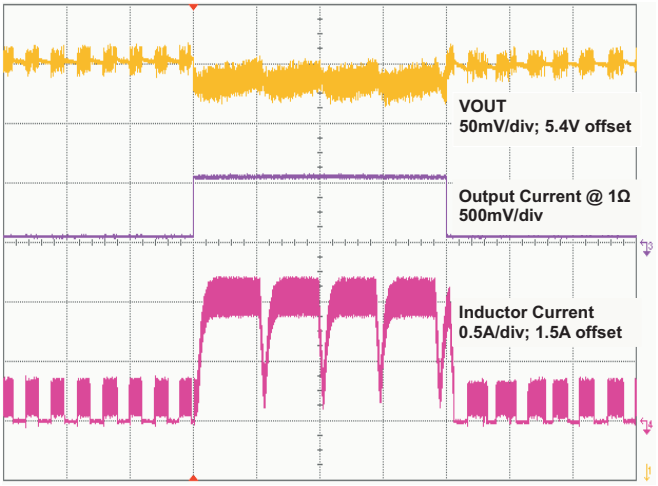


Figure 7.

STARTUP AFTER ENABLE I_{LIM} = 1000mA, NO LOAD

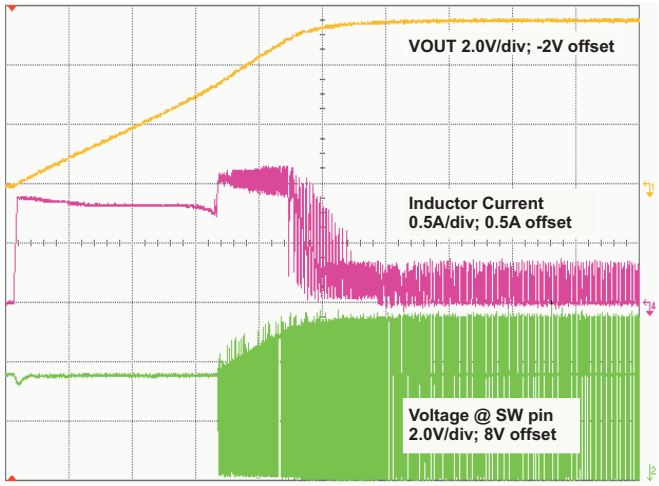


Figure 8.

STARTUP AFTER ENABLE I_{LIM} = 500mA, NO LOAD

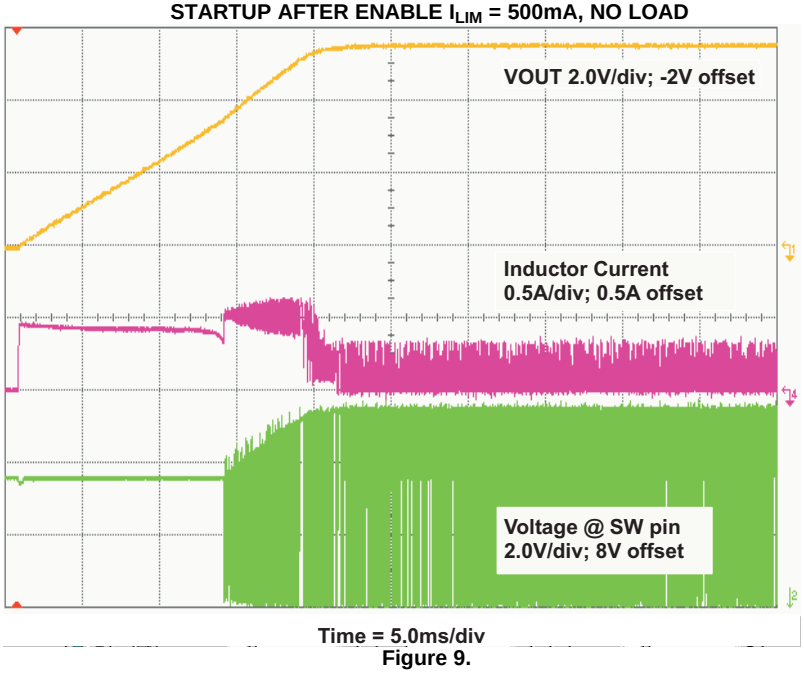


Figure 9.

DETAILED DESCRIPTION

OPERATION

The TPS61251 Boost Converter operates as a quasi-constant frequency adaptive on-time controller. In a typical application the frequency will be 3.5 MHz and is defined by the input to output voltage ratio and does not vary from moderate to heavy load currents. At light load the converter will automatically enter Power Save Mode and operates in PFM (Pulse Frequency Modulation) mode. During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which offers excellent line and load regulation and the use of small ceramic input capacitors.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side NMOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the peak current is reached, the current comparator trips, the on-timer is reset turning off the switch, and the current through the inductor then decays to an internally set valley current limit. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

The TPS61251 directly and accurately controls the average input current through intelligent adjustment of the valley current limit, allowing an accuracy of ±10%. Together with an external bulk capacitor the TPS61251 allows an application to be interfaced directly to its load, without overloading the input source due to appropriate set average input current limit .

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless to guarantee accurate output voltage regulation even with very low ESR the regulation loop can switch to a pure comparator regulation scheme. During this operation the output voltage is regulated between two thresholds. The upper threshold is defined by the programmed output voltage and the lower value is about 10 mV lower. If the upper threshold is reached the off-time is increased to reduce the current in the inductor. Therefore the output voltage will slightly drop until the lower threshold is tripped. Now the off-time will be reduced to increase the current in the inductor to charge up the output voltage to the steady-state value. The current swing during this operation mode is strongly depending on the current drawn by the load but will not exceed the programmed current limit. The output voltage during comparator operation stays within the specified accuracy with minimum voltage ripple.

This architecture with adaptive slope compensation provides excellent transient load response and requiring minimal output filtering. Internal softstart and loop compensation simplifies the design process while minimizing the number of external components.

CURRENT LIMIT OPERATION

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off-time through sensing of the voltage drop across the synchronous rectifier. The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1 as shown below:

$$I_{OUT(CL)} = (1 - D) \cdot I_{IN(DC)} \quad (1)$$

The duty cycle (D) can be estimated by following Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

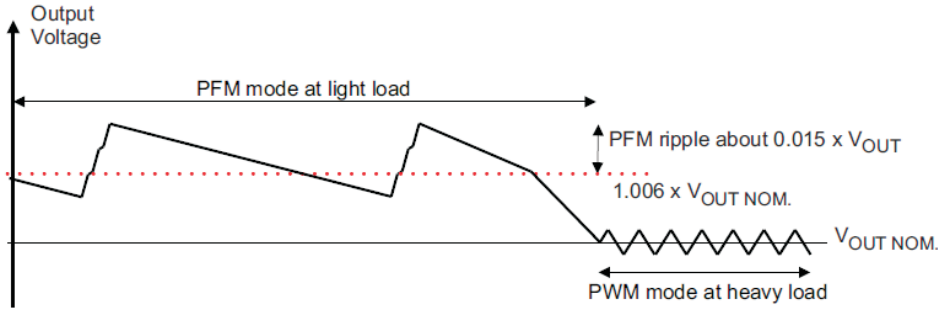
SOFTSTART

The TPS61251 has an internal charging circuit that controls the current during the output capacitor charging and prevents the converter from inrush current that exceeds the set current limit. For typical 100 µs the current is ramped to the set current limit. After reaching the current limit threshold the output capacitor is charged with a constant current until the programmed output voltage is reached. During the phase where $V_{IN} > V_{OUT}$ the rectifying switch is controlled by the current limit circuit and works as a linear regulator in constant current mode. If then $V_{IN} = V_{OUT}$ the converter starts switching and boosting up the voltage to its nominal output voltage by still

charging the capacitor with a constant current set by resistor R_{ILIM}. During constant current charging power dissipation in the TPS61251 is increased resulting in a thermal rise or heating of the device. If the output capacitor is very large charging time can be long and thermal rise high. To prevent overheating of the device during the charge phase the current will be limited to a lower value when device temperature is high. Please refer to THERMAL REGULATION.

POWER-SAVE MODE

The TPS61251 integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. During the power save operation when the output voltage is above the set threshold the converter turns off some of the inner circuits to save energy.



The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

SNOOZE MODE

During this enhanced power save mode, the converter will still maintain the output voltage with a tolerance of ±2%. The operating current in snooze mode, is however, drastically reduced to a typical value of 2 μA. This will be achieved by turning off as much as possible of the inner regulation circuits. Load current in snooze mode is limited to 2 mA. If the load current increases above 2 mA, the controller recognizes a further drop of the output voltage and the device turns on again in order to charge the output capacitor to the programmed output voltage again.

100% DUTY-CYCLE MODE

If $V_{IN} > V_{OUT}$ the TPS61251 offers the lowest possible input-to-output voltage difference while still maintaining current limit operation with the use of the 100% duty-cycle mode. In this mode, the PMOS switch is constantly turned on. During this operation the output voltage follows the input voltage and will not fall below the programmed value if the input voltage decreases below V_{OUT}. The output voltage drop during 100% mode depends on the load current and input voltage, and the resulting output voltage is calculated as:

$$V_{OUT} = V_{IN} - \left(DCR + r_{DS(on)}\right) \cdot I_{OUT} \quad (3)$$

with:

DCR is the DC resistance of the inductor

$r_{DS(on)}$ is the typical on-resistance of the PMOS switch

ENABLE

The device is enabled by setting EN pin to a voltage above 1 V. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the softstart is activated and the output voltage ramps up. The output voltage reaches its nominal value as fast as the current limit settings and the load condition allows it.

The EN input can be used to control power sequencing in a system with several DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

UNDER-VOLTAGE LOCKOUT (UVLO)

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typ. 2.1V.

POWER GOOD

The device has a built in power good function to indicate whether the output voltage has reached the programmed value and therefore the capacitor is fully charged. The power good output (PG) is set high if the feedback voltage reaches 95% of its nominal value. The power good comparator operates even in shut down mode when EN is set to low and/or V_{IN} is turned off. This guaranties power good functionality until the capacitor is discharged. The PG output goes low when V_{OUT} drops below 2.3 V and indicates the discharge of the capacitor. If the output voltage decreases further and goes below 2.0 V the converter disables all internal circuitry. Therefore the PG open drain output becomes high resistive and follows the voltage the pull-up resistor is connected to.

Since power good functionality is active as long as the output capacitors are charged the converter can be disconnected from its supply but is still supplying the following circuitry with energy. A connected buck converter or buck-boost converter can use this energy to support a follow-on circuit that needs additional energy for a secured shut down.

INPUT OVER VOLTAGE PROTECTION

This converter has a input over voltage protection that protects the device from damage due to a voltage higher than the absolute maximum rating of the input allows. If 6.5 V (typ.) at the input is exceeded the converter completely shuts down to protect its inner circuitry as well as the circuit connected to V_{OUT} . If the input voltage drops below 6.4 V (typ.) it turns on the device again and enters normal start up again.

LOAD DISCONNECT AND REVERSE CURRENT PROTECTION

The TPS61251 has an intelligent load disconnect circuit that prevents current flow in any direction during shutdown. In case of a connected battery and $V_{IN} > V_{OUT}$ the converter will not discharge the battery during shutdown of the converter. In the opposite case when a bulk capacitor is connected to VOUT and charged to a higher voltage than V_{IN} the converter prevents the capacitor from being discharged through the input load (battery).

THERMAL REGULATION

The TPS61251 contains a thermal regulation loop that monitors the die temperature. If the die temperature rises to values above 110 °C, the device automatically reduces the current to prevent the die temperature from further increasing. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit-condition.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device enters thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. When the junction temperature falls about 20 °C below the thermal shutdown, the device continues the operation.

APPLICATION INFORMATION

EXAMPLE

During the following Application Information section one specific example will be used to define and work with the different equations.

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	3.6	V
Minimum Input Voltage	$V_{IN(min)}$	2.9	V
Output Voltage	V_{OUT}	5.5	V
Input Current Limit set by R_{ILIM}	I_{LIM}	500	mA
Feedback Voltage	V_{FB}	1.2	V
Switching Frequency	f	3.5	MHz
Estimated Efficiency	η	90	%
Inductor Value of Choice	L1	1.0	µH

OUTPUT VOLTAGE SETTING

The output voltage can be calculated by Equation 4:

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (4)$$

To minimize the current through the feedback divider network and therefore increase efficiency during snooze mode operation, R2 should be >240k. To keep the network robust against noise the resistor divider can also be in the lower 100k values. Regarding the example, R1 is 1000 kΩ and R2 is 280 kΩ.

An external feed forward capacitor C1 is required for optimum load transient response. The value of C1 should be 1000pF. The connection from FB pin to the resistor divider should be kept short and away from noise sources, such as the inductor or the SW line.

AVERAGE INPUT CURRENT LIMIT

The average input current is set by selecting the correct external resistor value correlating to the required current limit. Equation 5 is a guideline for selecting the correct resistor value:

$$R_{ILIM} = \frac{1.0V}{I_{LIM}} \cdot 10{,}000 \quad (5)$$

For a current limit of 500 mA the resistor value will be 20 kΩ

MAXIMUM OUTPUT CURRENT

The maximum output current is set by R_{ILIM} and the input to output voltage ratio and can be calculated by Equation 6:

$$I_{OUT(max)} \approx I_{LIM} \cdot \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (6)$$

Following the example $I_{OUT(max)}$ will be 295 mA at 3.6 V input voltage and will decrease with lower input voltage values due to the energy conservation.

INDUCTOR SELECTION

As for all switching power supplies two main passive components are required for storing the energy during operation. This is done by an inductor and an output capacitor. The inductor must be connected between VIN pin and SW pin to make sure that the TPS61251 device operates. To select the right inductor current rating the programmed input current limit as well as the current ripple through the inductor is necessary. Estimation of the maximum peak inductor current can be done using Equation 7.

$$I_{L(max)} = I_{LIM} + \Delta I_L = I_{LIM} + \frac{V_{IN(min)} \cdot D}{L \cdot f} \quad \text{with} \quad D = 1 - \frac{V_{IN(min)} \cdot \eta}{V_{OUT}} \tag{7}$$

Regarding the example from above the current ripple (ΔI_L) will be 290 mA and therefore an inductor with a rated current of about 800 mA should be used.

The TPS61251 is designed to work with inductor values between 1.0 µH and 2.2 µH. For typical applications a 1.5 µH inductor is recommended. Regarding the conversion factor and the need of a sufficient output current the rated current for the inductor drives into lower inductance values. Therefore the inductor value can be reduced down to 1.0 µH without degrading the stability. Reduced inductance values increase the current ripple that needs to be included in the peak current calculation for the inductor (Equation 7). Using standard boost converters the current through the inductor is defined by the switch current limit of the converters switches and therefore bigger inductors have to be chosen. TPS61251 allows the design engineer to reduce the current limit to the needs of the application regardless the maximum switch current limit of the converter. Programming a lower current value allows the use of smaller inductors without the danger to get into saturation.

OUTPUT CAPACITOR

The second energy storing device is the output capacitor. When selecting output capacitors for large pulsed loads, the magnitude and duration of the pulsing current, together with the ripple voltage specification, determine the choice of the output capacitor. Both the ESR of the capacitor and the charge stored in the capacitor each cycle contribute to the output voltage ripple. The ripple due to the charge is approximately what results from Equation 8

$$V_{RIPPLE(mV)} = \frac{I_{PULSE} - I_{STANDBY} \cdot t_{on}}{C_{OUT}} \tag{8}$$

where I_{PULSE} and t_{ON} are the peak current and on time during transmission burst and $I_{STANDBY}$ is the current in standby mode. The above is a worst-case approximation assuming all the pulsing energy comes from the output capacitor.

The ripple due to the capacitor ESR is defined by Equation 9

$$\Delta V_{ESR} = \left(I_{PULSE} - I_{STANDBY}\right) \cdot ESR \tag{9}$$

High capacitance values and low ESR can lead to instability in some internally compensated boost converters. The internal loop compensation of the TPS61251 is optimized to be stable with output capacitor values greater than 150µF with very low ESR.

Since big bulk capacitors can not be placed very close to the IC it is required to put a small ceramic capacitor of about 4.7 µF as close as possible to the output terminals. This will reduce parasitic effects that can influence the functionality of the converter.

Table 2. List of Bulk Capacitors

VENDOR (alphabetical order)	CAPACITANCE	PART NUMBER
Kemet	470 µF, 6.3 V, 55 mΩ	T520W477M006ATE055
Sanyo	470 µF, 6.3 V, 35 mΩ	6TPE470MAZU

INPUT CAPACITOR

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small form factors. Input capacitors should be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple on the supply rail without limitations. Although low ESR tantalum capacitors may be used.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance. A 10 V rated 0805 capacitor with 10 µF can have an effective capacitance of less 5 µF at an output voltage of 5 V.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the load transient takes place and the turn on of the PMOS switch, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed close to the IC to keep the feedback connection short. To lay out the ground, short traces and wide are recommended. This avoids ground shift problems, which can occur due to superimposition of power ground current and the feedback divider.

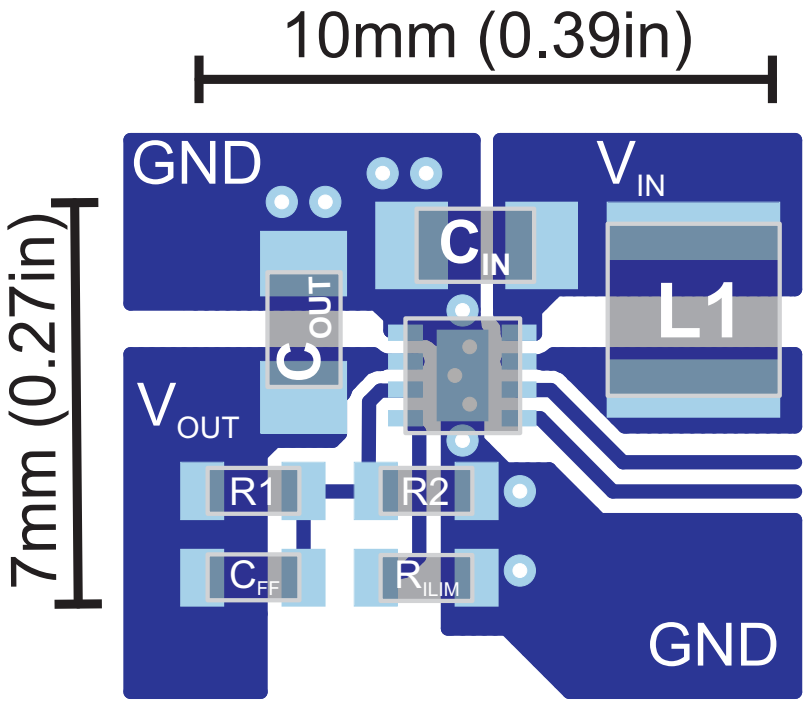


Figure 10. Suggested Layout without bulk capacitors (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - E.g. increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker cupper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS61251 is 150°C.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
TPS61251DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
TPS61251DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

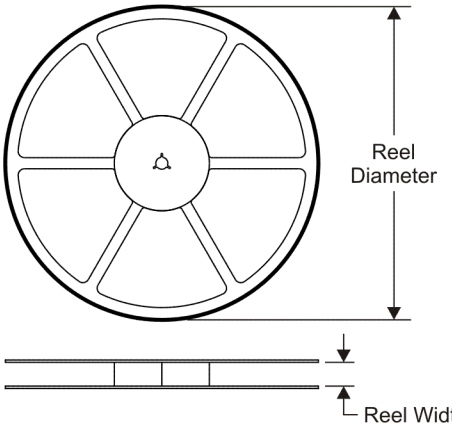
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

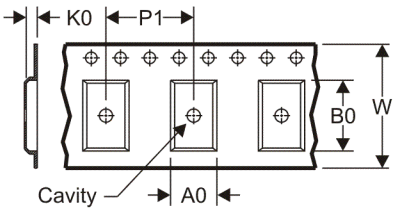
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

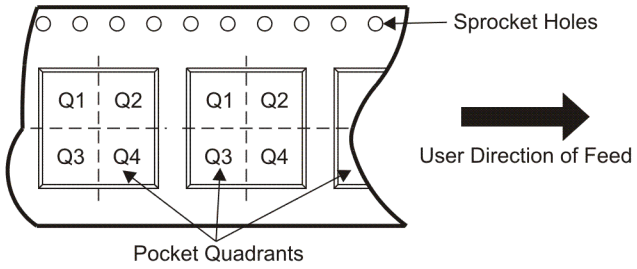


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



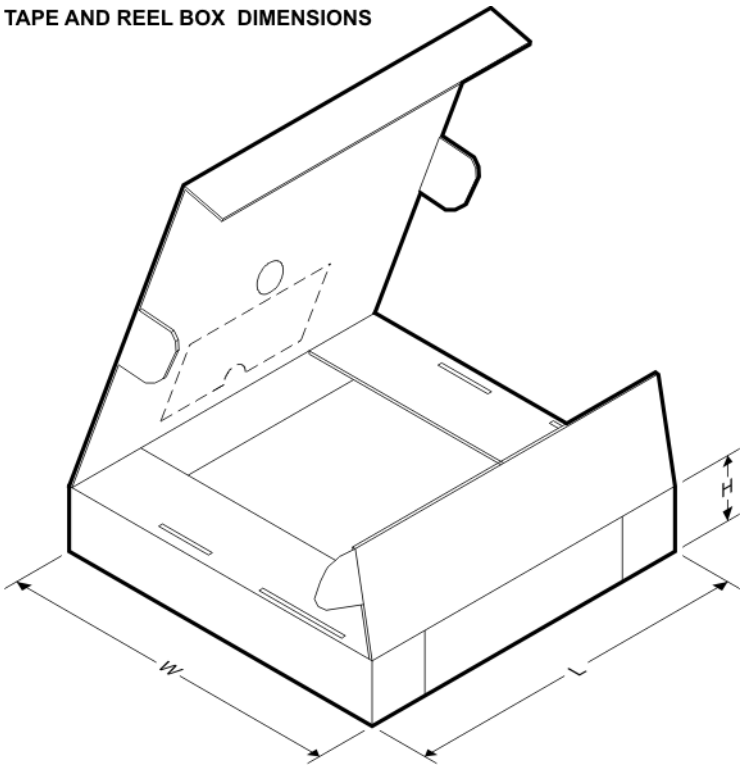
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61251DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61251DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

15-Oct-2010

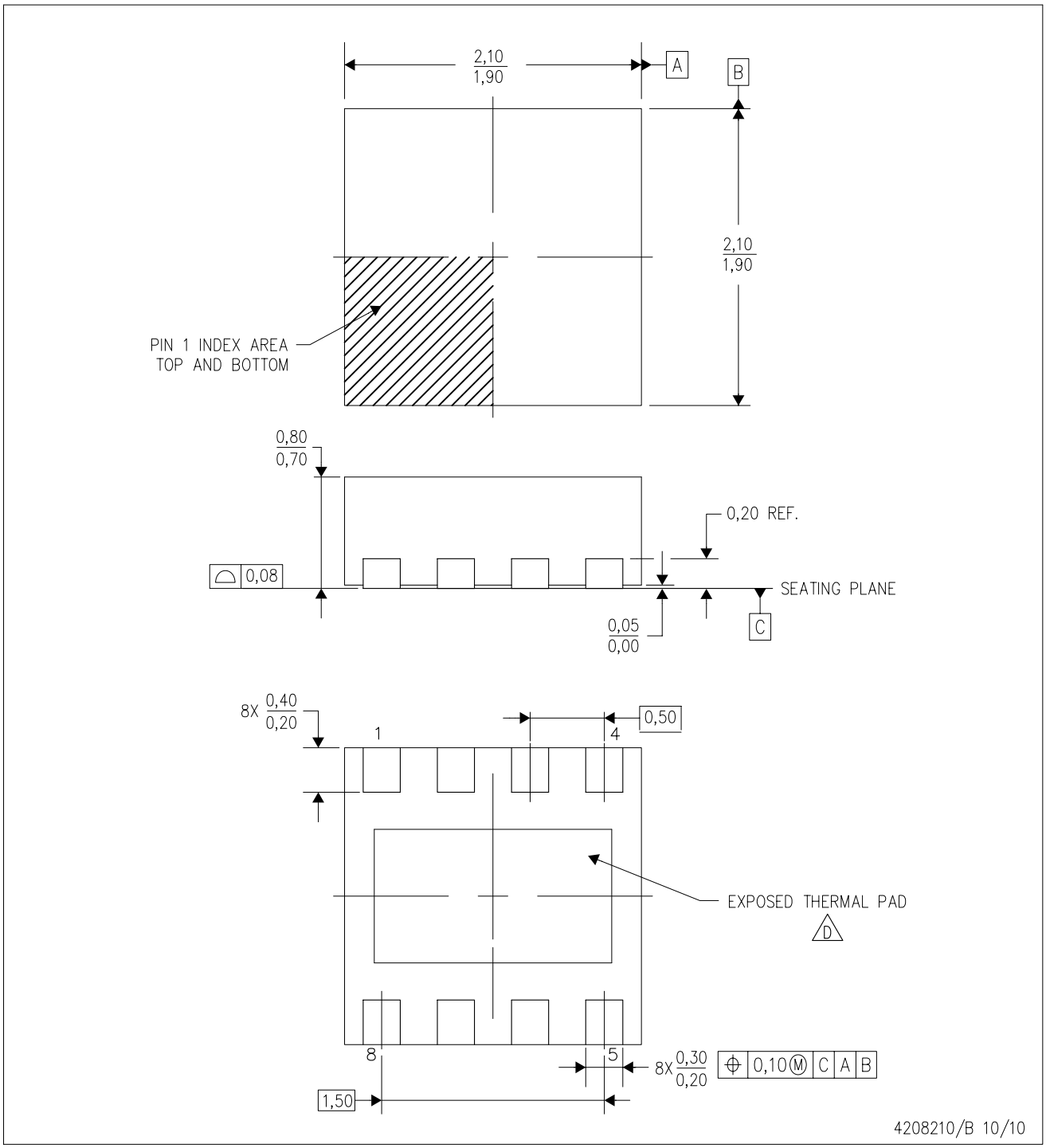
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61251DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
TPS61251DSGT	WSON	DSG	8	250	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

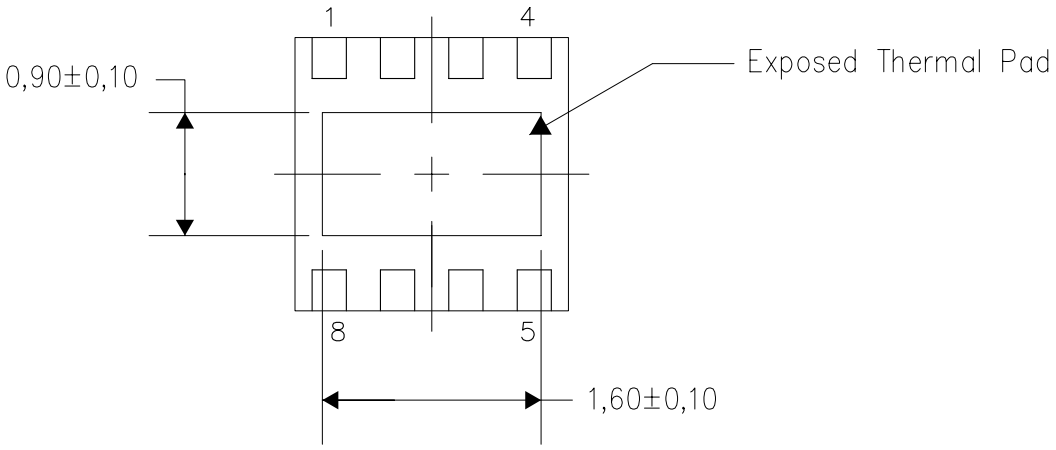
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



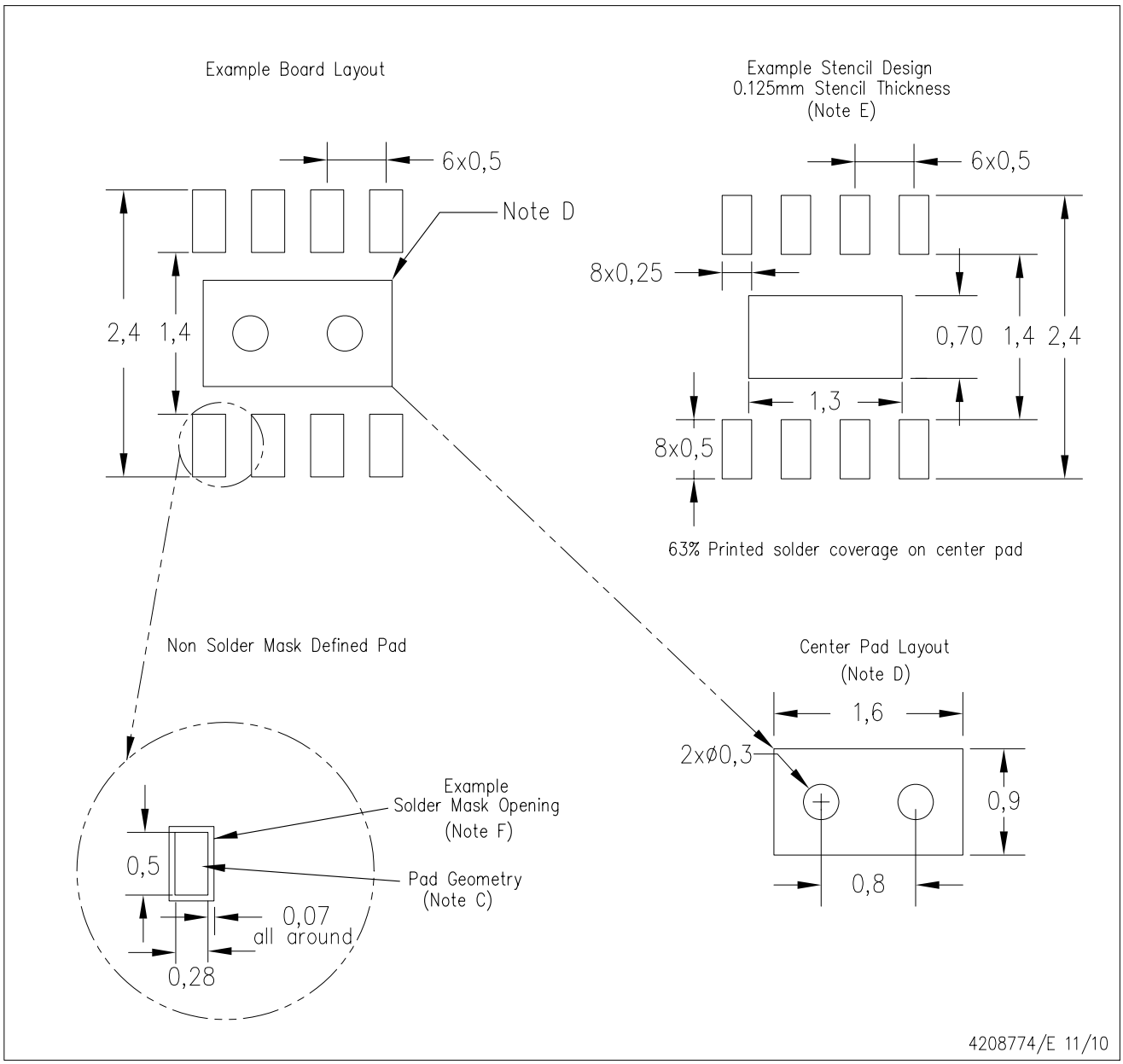
Bottom View

Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A. All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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