REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rajesh Pithadia

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COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
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Raymond Monnin

MICROCIRCUIT, DIGITAL-LINEAR, CMOS, LOW-VOLTAGE 10 -BIT ANALOG TO DIGITAL CONVERTER WITH SERIAL CONTROL AND 8 ANALOG INPUTS, MONOLITHIC SILICON

DRAWING APPROVAL DATE
98-06-24

REVISION LEVEL	SIZE	CAGE CODE	
	A	**67268**	**5962-98538**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E430-98

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	98538	01	Q	R	X
* * *	* * *		* * *	* * *	* * *	* * *
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
\		/				
	V					
	Drawing number					

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLV1548	Low -Voltage 10-Bit Analog to Digital Converters with Serial control and 8 Analog Inputs.

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.5 V dc 2/
Input voltage range (V_I) (any input)	-0.3 V to V_{CC}+0.3 V
Output voltage (V_O)	-0.3 V to V_{CC}+0.3 V
Positive reference voltage, V_{REF+}	V_{CC}+ 0.1 V
Negative reference voltage, V_{REF-}	-0.1 V
Peak input current I_I (any input)	± 20 mA
Peak total input current (all inputs)	-30 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds	+260°C
Maximum power dissipation, $T_A \leq 25°C$: 3/	
Case R	1894 mW
Case 2	1375 mW
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	28°C/W
Case 2	20°C/W
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case R	66°C/W
Case 2	65°C/W
Junction temperature (T_J)	150 °C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+2.7 V dc to +5.5 V dc
Positive reference Voltage, (V_{REF+})	V_{CC} 4/
Negative reference Voltage, (V_{REF-})	0 V 4/
Differential reference Voltage, V_{REF+} - V_{REF-}	+2.5 V dc to V_{cc} + 0.2 V dc 4/
Analog input voltage range (V_I)	0 to V_{CC} 4/
High level input voltage, (V_{IH})	2.1 V dc
Low level input voltage, (V_{IL})	0.6 V dc
Setup time, input data bits valid before I/O CLK↑↓, t_{su} (A)	100 ns
Hold time, input data bits valid after I/O CLK↑↓, t_h(A)	5 ns
Setup time, $\overline{CS}$ ↓to I/O CLK↑, t_{su}(CS)	5 ns
Hold time, I/O CLK↓ to $\overline{CS}$ ↓, t_h(CS)	65 ns
Pulse duration, FS high, t_{wH}(FS)	1 I/O CLK periods

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to GND with REF- and GND wired together. (unless otherwise noted).
3/ Derate factor at $T_A > 25°C$ for case R is 15.1 mW/°C, and for case 2 is 11.0 mW/°C.
4/ Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltage less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.

1.4 Recommended operating conditions - Continued.

Pulse duration, $\overline{CS}$ ↑ to $\overline{CSTART}$, t_w(CSTART) ..... 0.84 µs
Setup time, $\overline{CS}$ ↑ to $\overline{CSTART}$ ↓, t_{su}(CSTART) ..... 10 ns
Clock frequency at I/O CLK , f_{CLK}; V_{CC} = 5.5 V ..... 0.1 to 10 MHz
V_{CC} = 2.7 V ..... 0.1 to 2.81 MHz
Pulse duration, I/O CLK high, t_{wH}(I/O); V_{CC} = 5.5 V ..... 50 ns
V_{CC} = 2.7 V ..... 100 ns
Pulse duration, I/O CLK low, t_{wL}(I/O); V_{CC} = 5.5 V ..... 50 ns
V_{CC} = 2.7 V ..... 100 ns
Transition time, I/O CLK t_t(I/O) ..... 1 µs 5/
Transition time, DATA IN, t_t(DATA IN) ..... 10 µs
Transition time, $\overline{CS}$, t_t(CS) ..... 10 µs
Transition time, FS, t_t(FS) ..... 10 µs
Transition time, $\overline{CSTART}$, t_t(CSTART) ..... 10 µs
Operating free-air temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

5/ This is the time required for the I/O CLK signal to fall from V_{IH} max to V_{IL} min or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with an input clock transition time as slow as 1µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block or logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_{OH} = -0.2 mA V_{CC} = 5.5 V	01	1, 2, 3	2.4		V
		I_{OH} = -20 µA V_{CC} = 2.7 V			V_{CC} - 0.1		
Low level output voltage	V_{OL}	I_{OL} = 0.8 mA V_{CC} = 5.5 V	01	1, 2, 3		0.4	V
		I_{OL} = 20 µA V_{CC} = 2.7 V				0.1	
High impedance output current	I_{OZ}	$V_{OUT} = V_{CC}$, $\overline{CS} = V_{CC}$	01	1, 2, 3		2.5	µA
		V_{OUT} = 0 V, $\overline{CS} = V_{CC}$				-2.5	
High level input current	I_{IH}	$V_{IN} = V_{CC}$	01	1, 2, 3		2.5	µA
Low level input current	I_{IL}	V_{IN} = 0 V	01	1, 2, 3		2.5	
Operating supply current	I_{CC}	I/O CLK = GND, V_{CC} = 3.3 V to 5.5 V, Conversion speed = fast, For all digital inputs, $0 \le V_{IN} \le 0.3$ V or $V_{IN} \ge V_{CC}$ - 0.3 V	01	1,2,3		1.5	mA
		I/O CLK = GND, V_{CC} = 3.3 V to 5.5 V, Conversion speed=slow, For all digital inputs, $0 \le V_{IN} \le 0.3$ V or $V_{IN} \ge V_{CC}$ - 0.3 V				1.0	
		I/O CLK = GND, V_{CC} = 2.7 V to 3.3 V, Conversion speed = slow For all digital inputs, $0 \le V_{IN} \le 0.3$ V or $V_{IN} \ge V_{CC}$ - 0.3 V				0.75	
Power down supply current	$I_{CC(PD)}$	For all digital inputs, $0 \le V_{IN} \le 0.3$ V or $V_{IN} \ge V_{CC}$ - 0.3 V	01	1,2,3		25	µA
Selected channel leakage current	I_{lkg}	Selected channel at V_{CC} Unselected channel at 0 V	01	1,2,3		1.0	µA
		Selected channel at 0 V Unselected channel at V_{CC}				-1.0	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_A ≤+125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Maximum static analog reference current into REF+	----	V_{ref+} = V_{CC} = 5.5V V_{ref-} = GND	01	1,2,3		1	µA
Input capacitance, analog inputs	C_{IN}	2/	01	1,2,3		55	pF
Input capacitance, control inputs	C_{IN}	2/	01	1,2,3		15	pF
Input multiplexer resistance	Z_{IN}	V_{CC} = 4.5 V 2/	01	1,2,3		1	kΩ
		V_{CC} = 2.7 V 2/				5	
Linearity Error	E_L	3/	01	1,2,3		±1	LSB
Differential linearity error	E_D	4/	01	1,2,3		±1	LSB
Offset error	E_O	4/ 5/	01	1,2,3		±1.5	LSB
Gain error	E_G	4/ 5/	01	1,2,3		±1	LSB
Total unadjusted error	E_T	6/	01	1,2,3		±1.75	LSB
Functional tests		See 4.4.1C	01	7,8A,8B	L	H	
Conversion time	t_{CONV}	Fast conversion speed See figure 4	01	9,10,11		10	µs
		Slow conversion speed See figure 4				25	
Total cycle time (access, sample, conversion and EOC↑ to $\overline{CS}$↓ delay)	t_C	Fast conversion speed See figure 4 7/ 8/ 9/	01	9,10,11		10.1 + 10 I/O CLK	µs
		Slow conversion speed See figure 4 7/ 9/				40.1 +10 I/O CLK	
Channel acquisition time (sample)	t_{acq}	See figure 4 7/	01	9,10,11		6	I/O CLK periods
Valid time, DATA OUT remains valid after I/O CLK↓	t_V	See figure 4	01	9,10,11	50		ns
Delay time, I/O CLK high to FS high	$t_{d1(FS)}$	See figure 4	01	9,10,11	5	50	ns
Delay time, I/O CLK high to FS low	$t_{d2(FS)}$	See figure 4	01	9,10,11	10	60	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ -55°C ≤ T_A ≤+125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Delay time, EOC↑ to $\overline{CS}$ low	$t_{d(EOC\uparrow - CS\downarrow)}$	See figure 4 10/	01	9,10,11	100		ns
Delay time $\overline{CS}$↓ to FS↑	$t_{d(CS\downarrow - FS\uparrow)}$	See figure 4	01	9,10,11	1	7	I/O CLK periods
Delay time, 10th I/O CLK low to $\overline{CS}$ low to abort conversion.	$t_{d\ (I/O - CS)}$	See figure 4 11/	01	9,10,11		1.1	µs
Delay time, I/O CLK low to DATA OUT valid	$t_{d\ (I/O - DATA)}$	See figure 4	01	9,10,11		50	ns
Delay time, 10th I/O CLK ↓ to EOC low	$t_{d\ (I/O - EOC)}$	See figure 4	01	9,10,11		240	ns
Enable time, $\overline{CS}$ low to DATA OUT valid (MSB driven)	t_{PZH}, t_{PZL}	See figure 4	01	9,10,11		1.3	µs
Disable time, $\overline{CS}$ high to DATA OUT invalid (high impedance)	t_{PHZ}, t_{PLZ}	See figure 4	01	9,10,11		150	ns
Fall time, EOC	$t_{f\ (EOC)}$	See figure 4	01	9,10,11		50	ns
Rise time, output data bus at 2.2 MHz I/O CLK	$t_{r\ (bus)}$	See figure 4	01	9,10,11		250	ns
Fall time, output data bus at 2.2 MHz I/O CLK	$t_{f\ (bus)}$	See figure 4	01	9,10,11		250	ns

1/ VCC = V_{ref+} = 2.7 V to 5.5 V, I/O frequency = 2.2 MHz.
2/ Tested initially and after any design or process changes which affect this parameter.
3/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
4/ Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltage less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to 1 V (V_{ref+} - V_{ref-}); however, the electrical specifications are no longer applicable.
5/ Zero error is the difference between 0000000000 and the converted output for zero input voltage. Full-scale error is the difference between 1111111111 and the converted output for full-scale input voltage.
6/ Total unadjusted error comprises linearity, zero-scale and full-scale errors.
7/ I/O CLK period = 1/ (I/O CLK frequency).
8/ For 3.3 V to 5.5 V only.
9/ For microprocessor mode.
10/ For all operating modes.
11/ Any transactions of $\overline{CS}$ are recognized as valid only when the level is maintained for a setup time after the transition.

Device type	01
Case outlines	R and 2
Terminal number	Terminal symbol
1	A0
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	$\overline{\text{CSTART}}$
10	GND
11	$\overline{\text{INV CLK}}$
12	FS
13	REF-
14	REF+
15	$\overline{\text{CS}}$
16	DATA OUT
17	DATA IN
18	I/O CLK
19	EOC
20	V_{CC}

Pin description	
Terminal	Description
An (n =0 to 7)	Analog signal inputs
$\overline{\text{CSTART}}$	Sampling/conversion start control
$\overline{\text{INV CLK}}$	Inverted clock input
FS	DSP frame synchronization input
REF-	Lower reference voltage
REF+	Upper reference voltage
$\overline{\text{CS}}$	Chip select
DATA OUT	Serial data output
DATA IN	Serial data input
I/O CLK	Input-output clock
EOC	End of conversion

FIGURE 1. Terminal connections.

Condition Clock		I/O CLK Active Edge	
$\overline{\text{INV CLK}}$	FS at $\overline{\text{CS}}\downarrow$	Output data changes on	Input data sampled on
High	High (MP mode)	↓	↑
High	Low (DSP mode)	↑	↓
Low	High (MP mode)	↓	↓
Low	Low (DSP mode)	↑	↑

FIGURE 2. Truth table.

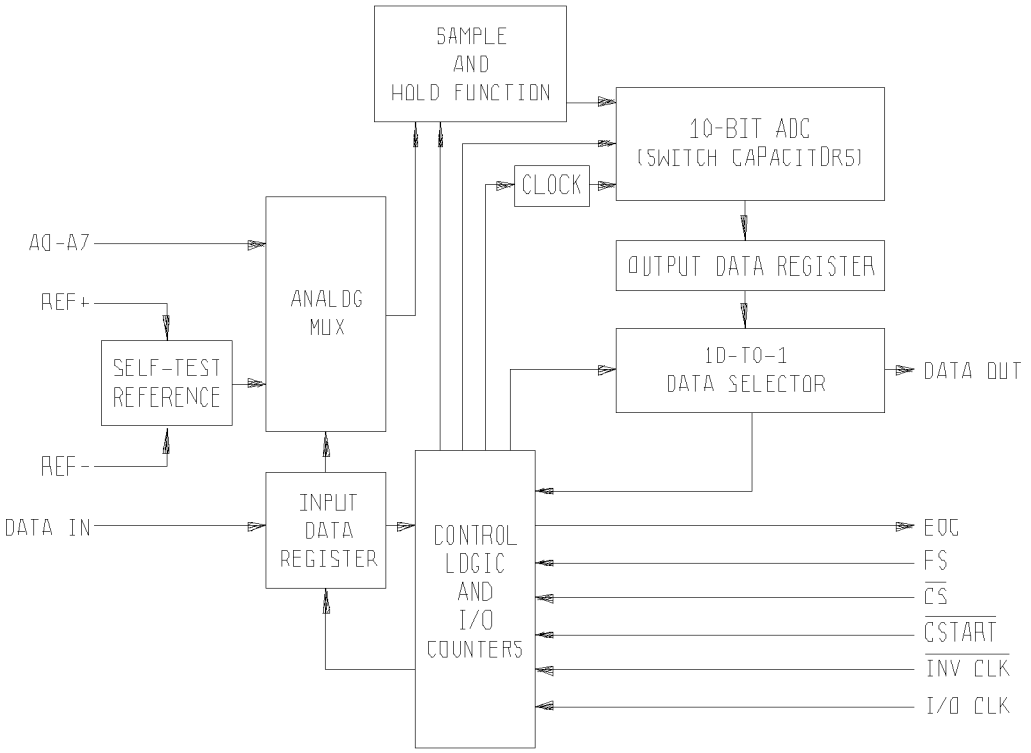
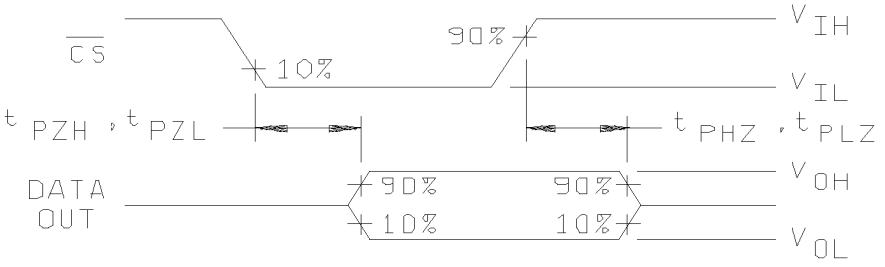


FIGURE 3. Block diagram.

DATA OUT to HI-Z voltage



$\overline{CS}$ and I/O CLK voltage

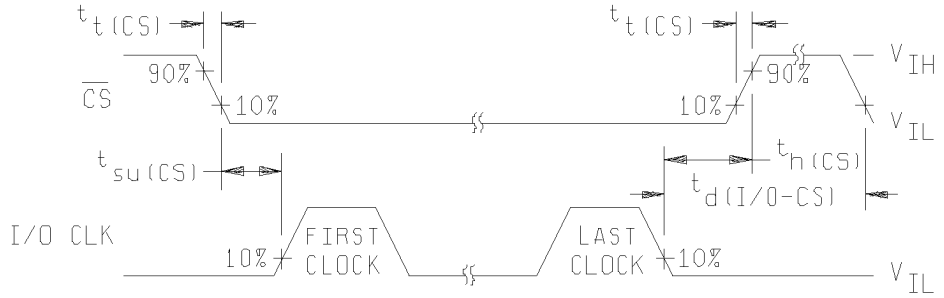
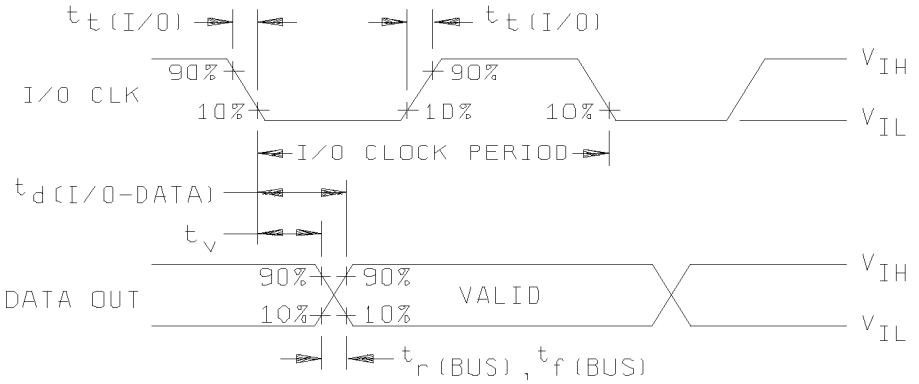


FIGURE 4. Switching waveforms and test circuit.

DATA OUT and I/O CLK voltage



CS low to FS low

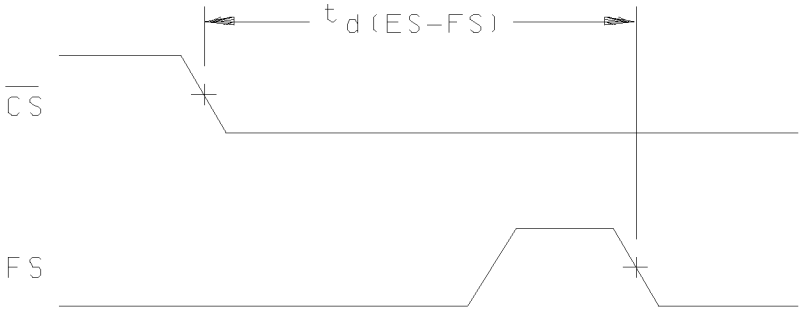
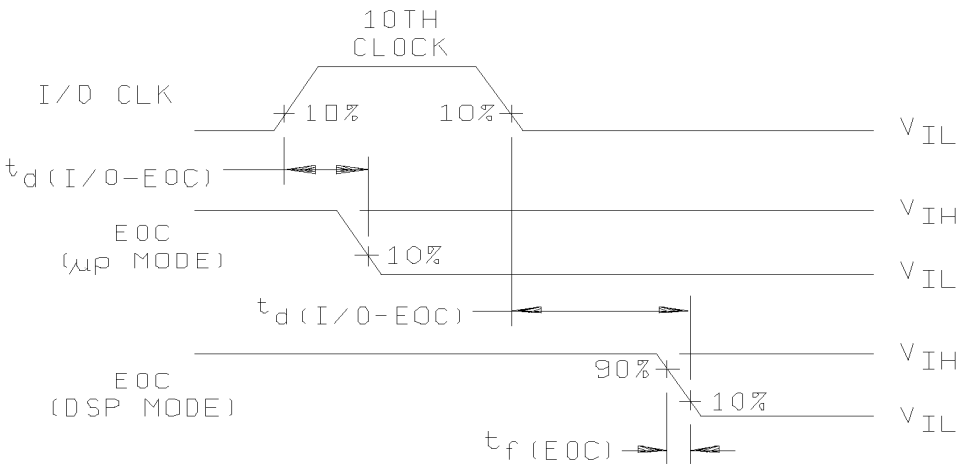


FIGURE 4. Switching waveforms and test circuit - Continued.

I/O CLK and EOC voltage



FS and I/O CLK voltage

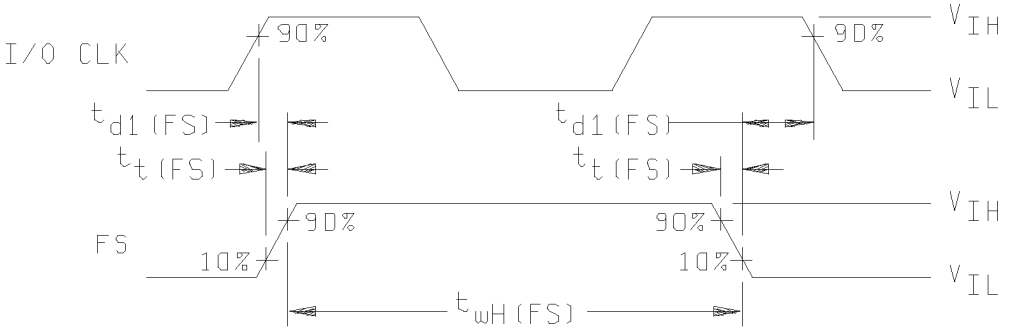


FIGURE 4. Switching waveforms and test circuit - Continued.

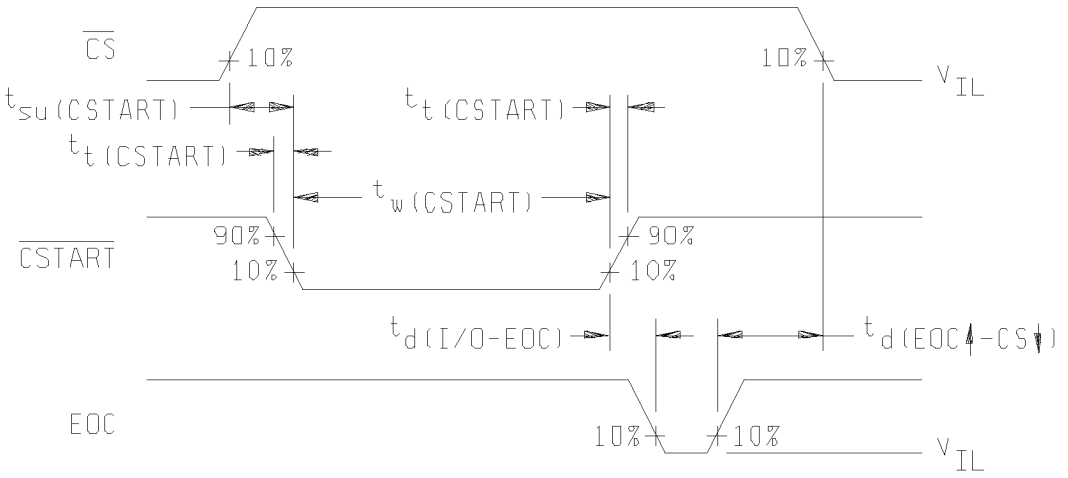
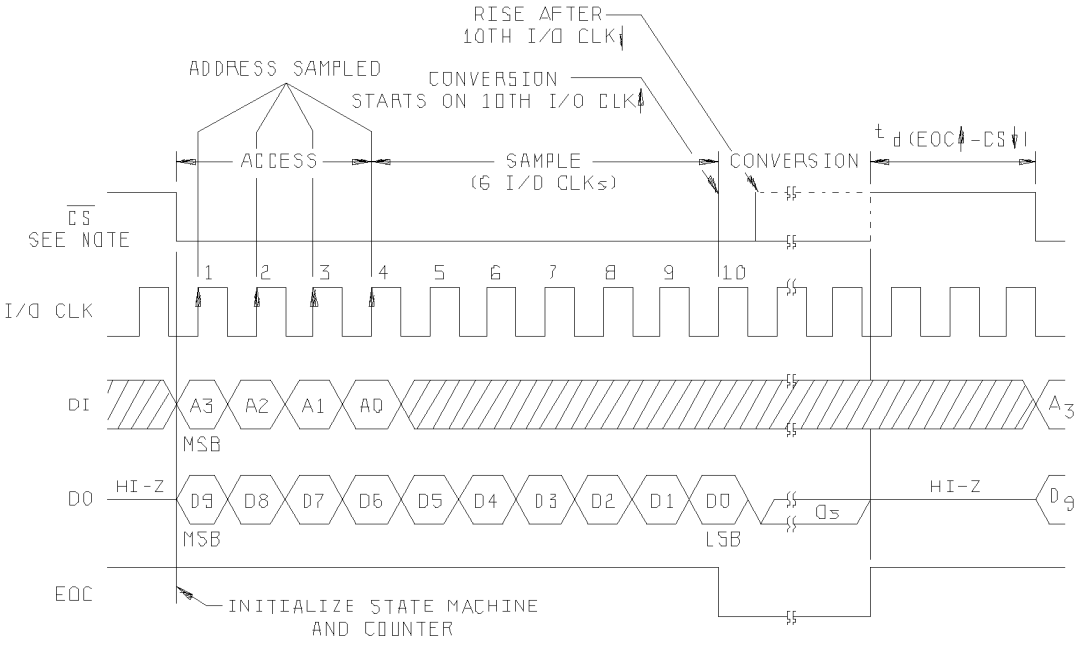


FIGURE 4. Switching waveforms and test circuit - Continued.

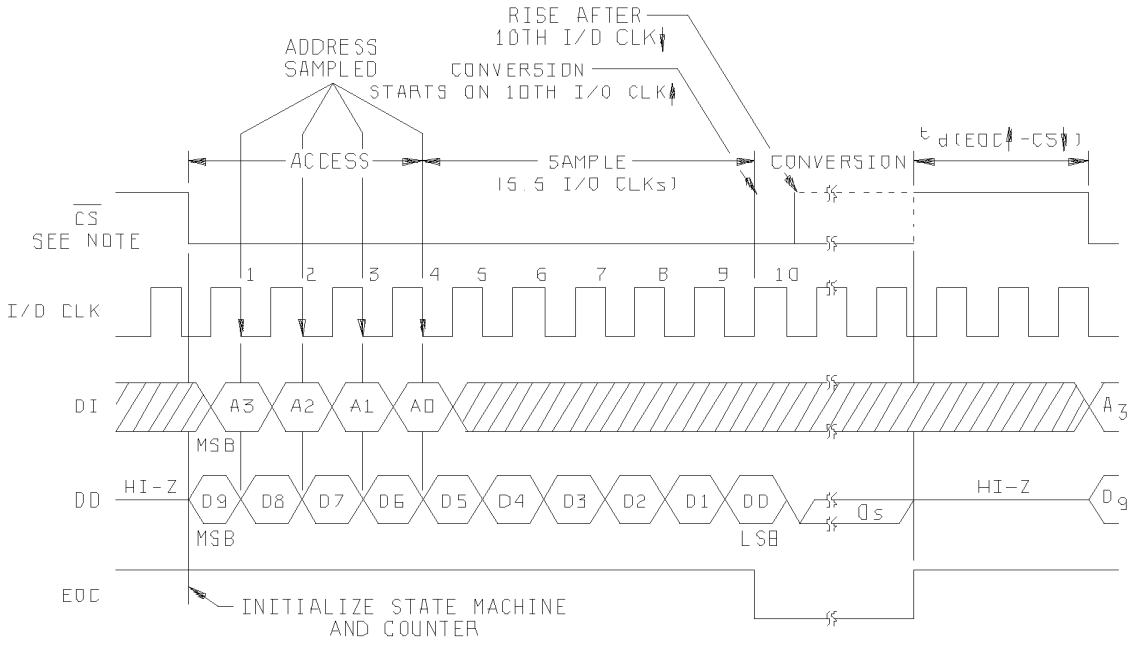
Microprocessor interface timing (normal sample mode, $\overline{\text{INV CLK}}$ = High)



NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - Continued.

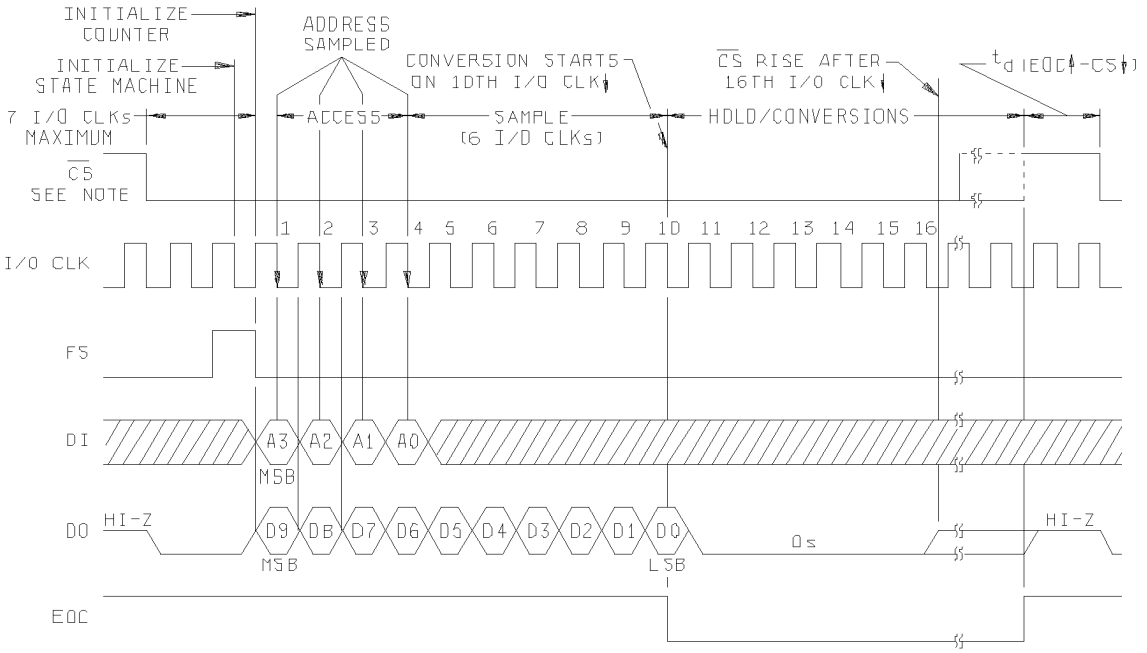
Microprocessor interface timing (normal sample mode, $\overline{\text{INV CLK}}$ = Low)



NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - Continued.

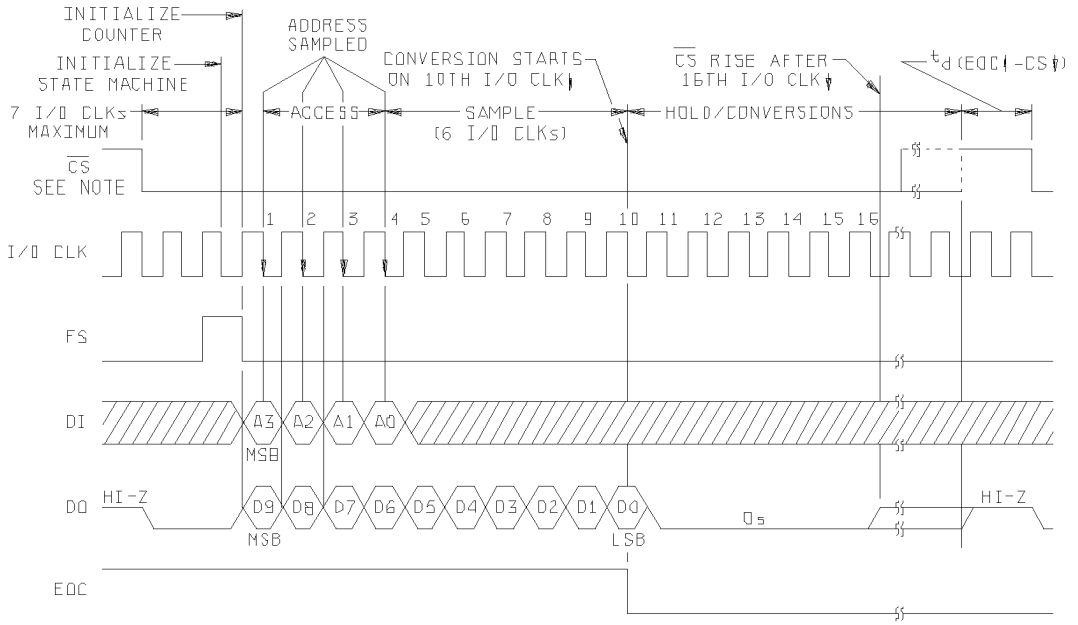
DSP interface timing (16-clock transfer, normal sample mode, $\overline{\text{INV CLK}}$ = High)



NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

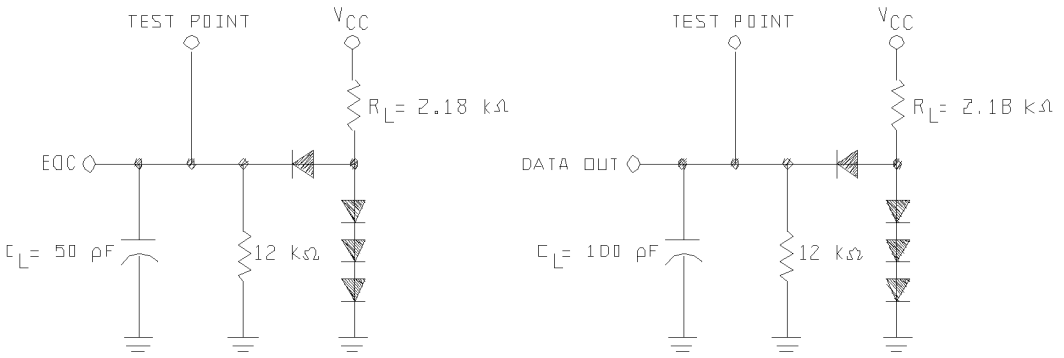
FIGURE 4. Switching waveforms and test circuit - Continued.

DSP interface timing (16-clock transfer, normal sample mode, $\overline{\text{INV CLK}}$ = Low)



NOTE: To minimize errors caused by noise at $\overline{\text{CS}}$, the internal circuitry waits for a setup time after $\overline{\text{CS}}\downarrow$ before responding to control input signals. No attempt should be made to clock in input data until the minimum $\overline{\text{CS}}$ setup time elapses.

FIGURE 4. Switching waveforms and test circuit - Continued.



NOTE: C_L includes probe and jig capacitance.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125EC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----	----	1
Final electrical parameters (see 4.2)	1,2,3,7,8A,8B,9, 10,11 1/	1,2,3,7,8A,8B, 9,10,11 1/	1,2,3,7,8A, 8B,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,7,8A,8B,9, 10,11	1,2,3,7,8A,8B, 9,10,11	1,2,3,7,8A, 8B,9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device .

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125EC, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25EC " 5EC, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-06-24

Approved sources of supply for SMD 5962-98538 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9853801QRA	01295	TLV1548MJB
5962-9853801Q2A	01295	TLV1548MFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.