

## SPICE Device Model Si8435DB

## **Vishay Siliconix**

## **Dual P-Channel 20-V (D-S) MOSFET**

### **CHARACTERISTICS**

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

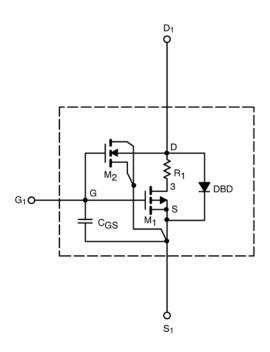
- Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

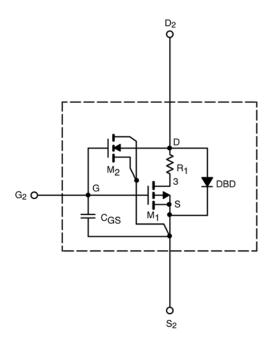
### **DESCRIPTION**

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to  $125^{\circ}$ C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			-		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	0.80		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS}$ = $-4.5 \text{ V}$	60		Α
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -3.3 \text{ A}$	0.063	0.060	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -2.8 \text{ A}$	0.082	0.083	
		$V_{GS} = -1.8 \text{ V}, I_D = -0.76 \text{ A}$	0.107	0.108	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = -10 \text{ V}, I_{D} = -3.3 \text{ A}$	11	9	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_{S} = -1 \text{ A}, V_{GS} = 0 \text{ V}$	-0.78	-0.80	V
Dynamic <sup>b</sup>	-		<del>-</del>	-	
Total Gate Charge	Q <sub>g</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -4.6 \text{ A}$	5	5.5	nC
Gate-Source Charge	$Q_{gs}$		0.75	0.75	
Gate-Drain Charge	$Q_{gd}$		1.5	1.5	

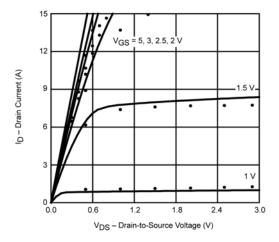
### Notes

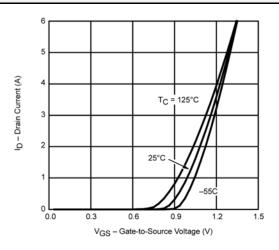
a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%. b. Guaranteed by design, not subject to production testing.

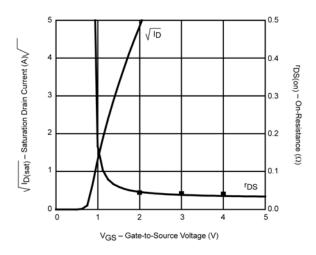


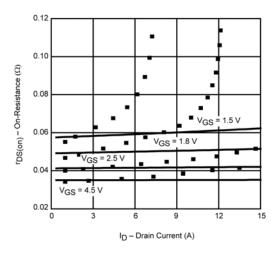
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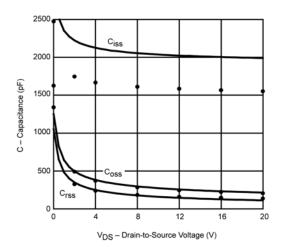
### COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

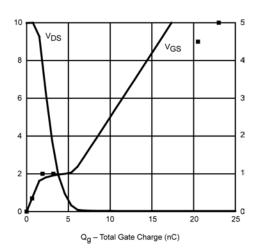












Note: Dots and squares represent measured data