CLASS V, 14-BIT, 400-MSPS DIGITAL-TO-ANALOG CONVERTER

Check for Samples: DAC5675A-SP

FEATURES

- 400-MSPS Update Rate
- LVDS-Compatible Input Interface
- Spurious-Free Dynamic Range (SFDR) to Nyquist
  - 69 dBc at 70 MHz IF, 400 MSPS
- W-CDMA Adjacent Channel Power Ratio (ACPR)
  - 73 dBc at 30.72 MHz IF, 122.88 MSPS
  - 71 dBc at 61.44 MHz IF, 245.76 MSPS
- Differential Scalable Current Outputs: 2 mA to 20 mA
- On-Chip 1.2-V Reference
- Single 3.3-V Supply Operation
- Power Dissipation: 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 20 MHz
- High-Performance 52-Pin Ceramic Quad Flat Pack (HFG)
- QML-V Qualified, SMD 5962-07204
- Military Temperature Range (–55°C to 125°C)

APPLICATIONS

- Cellular Base Transceiver Station Transmit Channel:
  - CDMA: WCDMA, CDMA2000, IS-95
  - TDMA: GSM, IS-136, EDGE/GPRS
  - Supports Single-Carrier and Multicarrier Applications
- Test and Measurement: Arbitrary Waveform Generation

DESCRIPTION/ORDERING INFORMATION

The DAC5675A is a 14-bit resolution high-speed digital-to-analog converter (DAC). The DAC5675A is designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct digital synthesis (DDS), and waveform reconstruction in test and measurement applications. The DAC5675A has excellent spurious-free dynamic range (SFDR) at high intermediate frequencies, which makes it well suited for multicarrier transmission in TDMA and CDMA based cellular base transceiver stations (BTSs).

The DAC5675A operates from a single supply voltage of 3.3 V. Power dissipation is 660 mW at f_{CLK} = 400 MSPS, f_{OUT} = 70 MHz. The DAC5675A provides a nominal full-scale differential current output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The output is referred to the analog supply voltage AV_{DD}.

The DAC5675A includes a low-voltage differential signaling (LVDS) interface for high-speed digital data input. LVDS features a low differential voltage swing with a low constant power consumption across frequency, allowing for high-speed data transmission with low noise levels; that is, with low electromagnetic interference (EMI). LVDS is typically implemented in low-voltage digital CMOS processes, making it the ideal technology for high-speed interfacing between the DAC5675A and high-speed low-voltage CMOS ASICs or FPGAs. The DAC5675A current-source-array architecture supports update rates of up to 400 MSPS. On-chip edge-triggered input latches provide for minimum setup and hold times, thereby relaxing interface timing.

The DAC5675A is specifically designed for a differential transformer-coupled output with a 50-Ω doubly-terminated load. With the 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2 dBm) is supported. The last configuration is preferred for optimum performance at high output frequencies and update rates. The outputs are terminated to AVDD and have voltage compliance ranges from AV_{DD} – 1 to AV_{DD} + 0.3 V.

An accurate on-chip 1.2-V temperature-compensated bandgap reference and control amplifier allows the user to adjust this output current from 20 mA down to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage may be applied. The DAC5675A features a SLEEP mode, which reduces the standby power to approximately 18 mW.

The DAC5675A is available in a 52-pin ceramic nonconductive tie-bar package (HFG). The device is specified for operation over the military temperature range of –55°C to 125°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

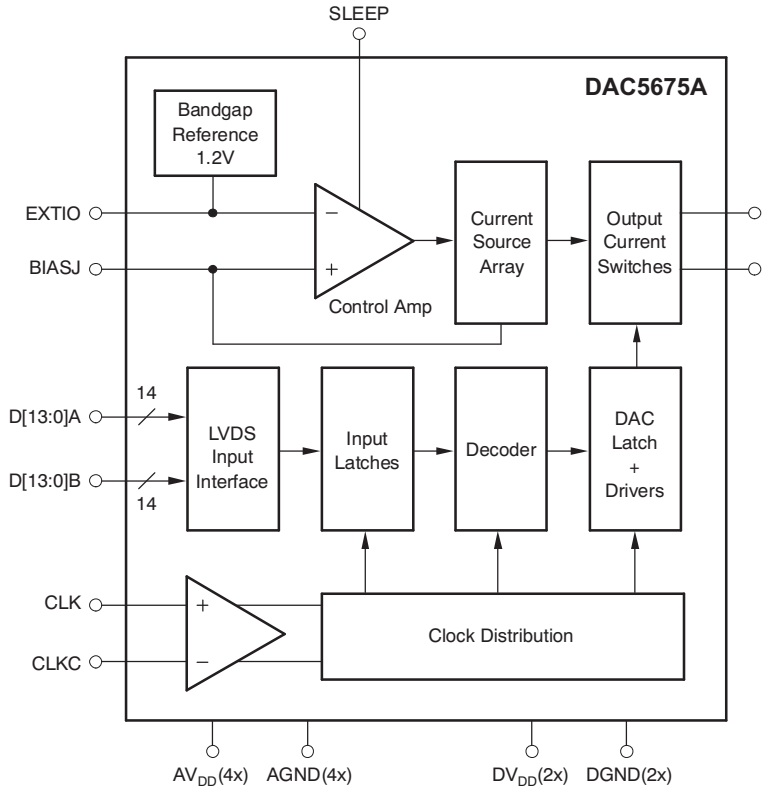
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE (2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	52 / HFG	5962-0720401VXC	5962-0720401VXC DAC5675AMHFG-V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Supply voltage range	AV_{DD} (2)	–0.3 to 3.6	V
	DV_{DD} (3)	–0.3 to 3.6	
	AV_{DD} to DV_{DD}	–3.6 to 3.6	
Voltage between AGND and DGND		–0.3 to 0.5	V
CLK, CLKC(2)		–0.3 to AV_{DD} + 0.3	V
Digital input D[13:0]A, D[13:0]B(3), SLEEP, DLLOFF		–0.3 to DV_{DD} + 0.3	V
IOUT1, IOUT2(2)		–1 to AV_{DD} + 0.3	V
EXTIO, BIASJ(2)		–1 to AV_{DD} + 0.3	V
Peak input current (any input)		20	mA
Peak total input current (all inputs)		–30	mA
Operating free-air temperature range, T_A		–55 to 125	°C
Storage temperature range		–65 to 150	°C
Lead temperature 1,6 mm (1/16 in) from the case for 10 s		260	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND
(3) Measured with respect to DGND

DC Electrical Characteristics (Unchanged after 100 kRad)

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			14			Bit
DC Accuracy(1)						
INL	Integral nonlinearity	T_{MIN} to T_{MAX}	–4	±1.5	4.6	LSB
DNL	Differential nonlinearity	T_{25C} to T_{MAX}	–2	±0.6	2.2	LSB
		T_{MIN}	–2	±0.6	2.5	
Monotonicity			Monotonic 12b Level			
Analog Output						
$I_{O(FS)}$	Full-scale output current		2		20	mA
	Output compliance range	AV_{DD} = 3.15 V to 3.45 V, $I_{O(FS)}$ = 20 mA	AV_{DD} – 1		AV_{DD} + 0.3	V
	Offset error			0.01		%FSR
	Gain error	Without internal reference	–10	5	10	%FSR
		With internal reference	–10	2.5	10	
	Output resistance			300		kΩ
	Output capacitance			5		pF
Reference Output						
$V_{(EXTIO)}$	Reference voltage		1.17	1.23	1.30	V
	Reference output current(2)			100		nA
Reference Input						
$V_{(EXTIO)}$	Input reference voltage		0.6	1.2	1.25	V
	Input resistance			1		MΩ
	Small-signal bandwidth			1.4		MHz
	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			12		ppm of FSR/°C
$\Delta V_{(EXTIO)}$	Reference voltage drift			±50		ppm/°C
Power Supply						
AV_{DD}	Analog supply voltage		3.15	3.3	3.6	V
DV_{DD}	Digital supply voltage		3.15	3.3	3.6	V
$I_{(AVDD)}$	Analog supply current(3)			115	148	mA
$I_{(DVDD)}$	Digital supply current(3)			85	130	mA
P_D	Power dissipation	Sleep mode		18		mW
		AV_{DD} = 3.3 V, DV_{DD} = 3.3 V		660	900	
APSRR	Analog and digital power-supply rejection ratio	AV_{DD} = 3.15 V to 3.45 V	–0.9	±0.1	0.9	%FSR/V
DPSRR			–0.9	±0.1	0.9	

(1) Measured differential at I_{OUT1} and I_{OUT2}: 25 Ω to AV_{DD}
(2) Use an external buffer amplifier with high impedance input to drive any external load.
(3) Measured at f_{CLK} = 400 MSPS and f_{OUT} = 70 MHz

AC Electrical Characteristics (Unchanged after 100 kRad)

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA, differential transformer-coupled output, 50-Ω doubly-terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog Output							
f_{CLK}	Output update rate					400	MSPS
$t_{s(DAC)}$	Output setting time to 0.1%	Transition: code x2000 to $x23_{FF}$			12		ns
t_{PD}	Output propagation delay				1		ns
$t_{r(IOUT)}$	Output rise time, 10% to 90%				300		ps
$t_{f(IOUT)}$	Output fall time, 90% to 10%				300		ps
	Output noise	$IOUT_{FS}$ = 20 mA			55		pA/√Hz
		$IOUT_{FS}$ = 2 mA			30		
AC Linearity							
THD	Total harmonic distortion	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		70		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		72		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		68		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz	60	68		
			f_{OUT} = 20.0 MHz, for T_{MIN}	57			
			f_{OUT} = 70 MHz		67		
			f_{OUT} = 140 MHz		55		
SFDR	Spurious-free dynamic range to Nyquist	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		70		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		73		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		70		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz	62	68		
			f_{OUT} = 20.0 MHz, for T_{MIN}	61			
			f_{OUT} = 70 MHz		69		
			f_{OUT} = 140 MHz		56		
SFDR	Spurious-free dynamic range within a window, 5 MHz span	f_{CLK} = 100 MSPS,	f_{OUT} = 19.9 MHz		82		dBc
		f_{CLK} = 160 MSPS,	f_{OUT} = 41 MHz		77		
		f_{CLK} = 200 MSPS,	f_{OUT} = 70 MHz		82		
		f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz		82		
			f_{OUT} = 70 MHz		82		
			f_{OUT} = 140 MHz		75		
SNR	Signal-to-noise ratio	f_{CLK} = 400 MSPS	f_{OUT} = 20.0 MHz	60	67		dBc
ACPR	Adjacent channel power ratio WCDM A with 3.84 MHz BW, 5 MHz channel spacing	f_{CLK} = 122.88 MSPS, IF = 30.72 MHz, See Figure 11			73		dB
		f_{CLK} = 245.76 MSPS, IF = 61.44 MHz,			71		
		f_{CLK} = 399.36 MSPS, IF = 153.36 MHz, See Figure 13			65		
IMD	Two-tone intermodulation to Nyquist (each tone at –6 dBfs)	f_{CLK} = 400 MSPS, f_{OUT1} = 70 MHz, f_{OUT2} = 71 MHz			73		dBc
		f_{CLK} = 400 MSPS, f_{OUT1} = 140 MHz, f_{OUT2} = 141 MHz			62		
	Four-tone intermodulation, 15-MHz span, missing center tone (each tone at –16 dBfs)	f_{CLK} = 156 MSPS, f_{OUT} = 15.6, 15.8, 16.2, 16.4 MHz			82		
		f_{CLK} = 400 MSPS, f_{OUT} = 68.1, 69.3, 71.2, 72 MHz			74		

Digital Specifications (Unchanged after 100 kRad)

over operating free-air temperature range, typical values at 25°C, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Interface: Nodes D[13:0]A, D[13:0]B						
V_{ITH+}	Positive-going differential input voltage threshold			100		mV
$V_{ITH–}$	Negative-going differential input voltage threshold			–100		mV
Z_T	Internal termination impedance		90	110	132	Ω
C_I	Input capacitance			2		pF
CMOS Interface (SLEEP)						
V_{IH}	High-level input voltage		2	3.3		V
V_{IL}	Low-level input voltage			0	0.8	V
I_{IH}	High-level input current		–100		100	µA
I_{IL}	Low-level input current		–10		10	µA
	Input capacitance			2		pF
Clock Interface (CLK, CLKC)						
|CLK-CLKC|	Clock differential input voltage		0.4		0.8	V_{PP}
$t_{w(H)}$	Clock pulse width high			1.25		ns
$t_{w(L)}$	Clock pulse width low			1.25		ns
	Clock duty cycle		40		60	%
V_{CM}	Common-mode voltage range		1.6	2	2.4	V
	Input resistance	Node CLK, CLKC		670		Ω
	Input capacitance	Node CLK, CLKC		2		pF
	Input resistance	Differential		1.3		kΩ
	Input capacitance	Differential		1		pF
Timing						
t_{SU}	Input setup time		1.5			ns
t_H	Input hold time		0.0			ns
t_{DD}	Digital delay time (DAC latency)			3		clk

Timing Information

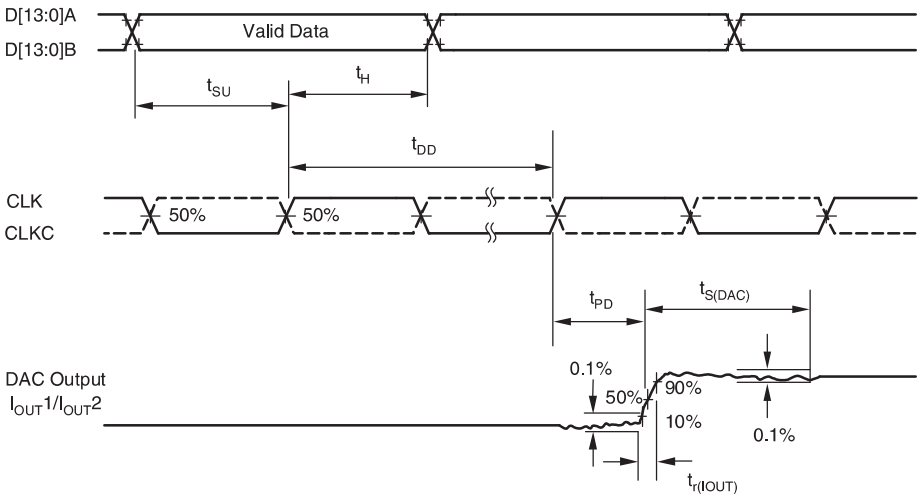


Figure 1. Timing Diagram

Electrical Characteristics(1)

over operating free-air temperature range, AV_{DD} = 3.3 V, DV_{DD} = 3.3 V, $I_{O(FS)}$ = 20 mA (unless otherwise noted)

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	LOGICAL BIT BINARY EQUIVALENT	COMMENT
V_A (V)	V_B (V)	$V_{A,B}$ (mV)	V_{COM} (V)		
1.25	1.15	100	1.2	1	Operation with minimum differential voltage (±100 mV) applied to the complementary inputs versus common-mode range
1.15	1.25	–100	1.2	0	
2.4	2.3	100	2.35	1	
2.3	2.4	–100	2.35	0	
0.1	0	100	0.05	1	
0	0.1	–100	0.05	0	
1.5	0.9	600	1.2	1	Operation with maximum differential voltage (±600 mV) applied to the complementary inputs versus common-mode range
0.9	1.5	–600	1.2	0	
2.4	1.8	600	2.1	1	
1.8	2.4	–600	2.1	0	
0.6	0	600	0.3	1	
0	0.6	–600	0.3	0	

(1) Specifications subject to change.

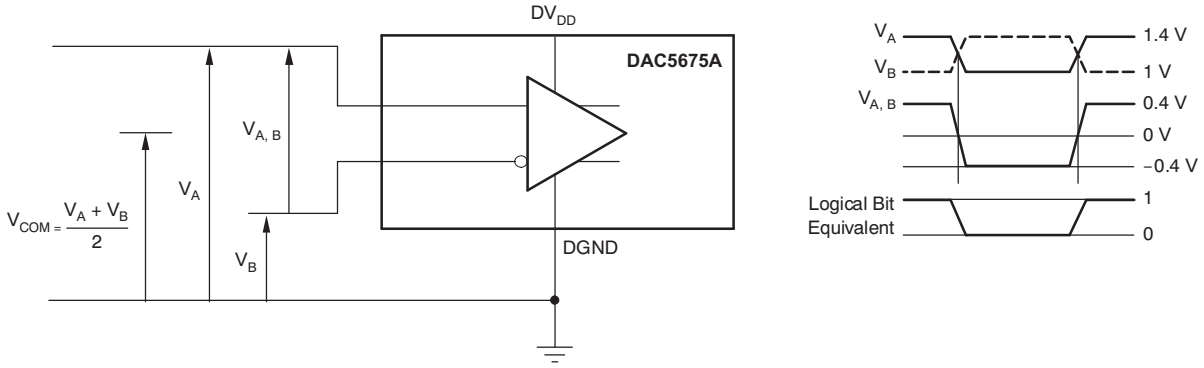
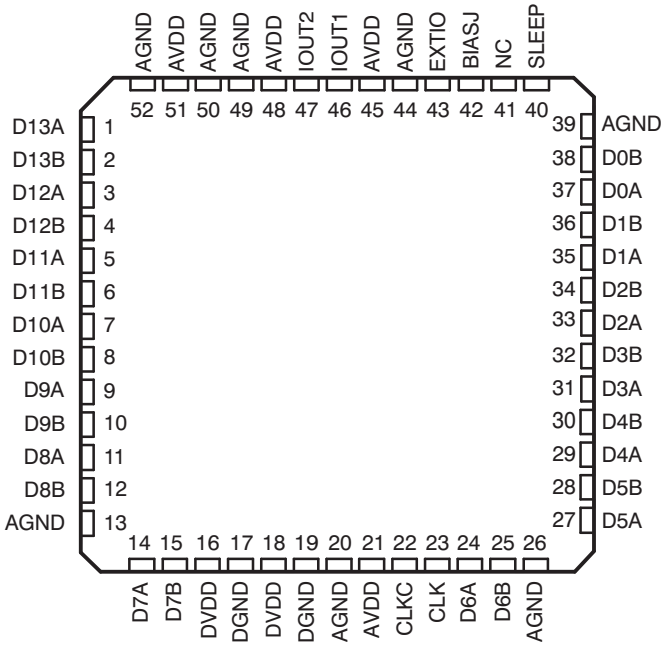


Figure 2. LVDS Timing Test Circuit and Input Test Levels

HFG PACKAGE
(TOP VIEW)



DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	13, 20, 26, 39, 44, 49, 50, 52	I	Analog negative supply voltage (ground). Pin 13 is internally connected to the heat slug and lid (lid is also grounded internally).
AV_{DD}	21, 45, 48, 51	I	Analog positive supply voltage
BIASJ	42	O	Full-scale output current bias
CLK	23	I	External clock input
CLKC	22	I	Complementary external clock
D[13:0]A	1, 3, 5, 7, 9, 11, 14, 24, 27, 29, 31, 33, 35, 37	I	LVDS positive input, data bits 13–0. D13A is the most significant data bit (MSB). D0A is the least significant data bit (LSB).
D[13:0]B	2, 4, 6, 8, 10, 12, 15, 25, 28, 30, 32, 34, 36, 38	I	LVDS negative input, data bits 13–0. D13B is the most significant data bit (MSB). D0B is the least significant data bit (LSB).
DGND	17, 19	I	Digital negative supply voltage (ground)
DV_{DD}	16, 18	I	Digital positive supply voltage
EXTIO	43	I/O	Internal reference output or external reference input. Requires a 0.1-µF decoupling capacitor to AGND when used as reference output.
IOUT1	46	O	DAC current output. Full-scale when all input bits are set '0'. Connect the reference side of the DAC load resistors to AV_{DD}.
IOUT2	47	O	DAC complementary current output. Full-scale when all input bits are '1'. Connect the reference side of the DAC load resistors to AV_{DD}.
NC	41		Not connected in chip. Can be high or low.
SLEEP	40	I	Asynchronous hardware power-down input. Active high. Internal pulldown.

Table 2. THERMAL INFORMATION

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, per JESD 51-5 methodology	21.813	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 test method 1012	0.849	°C/W

THERMAL NOTES

This CQFP package has built-in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly under the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11, 9 mm 2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically ground potential.

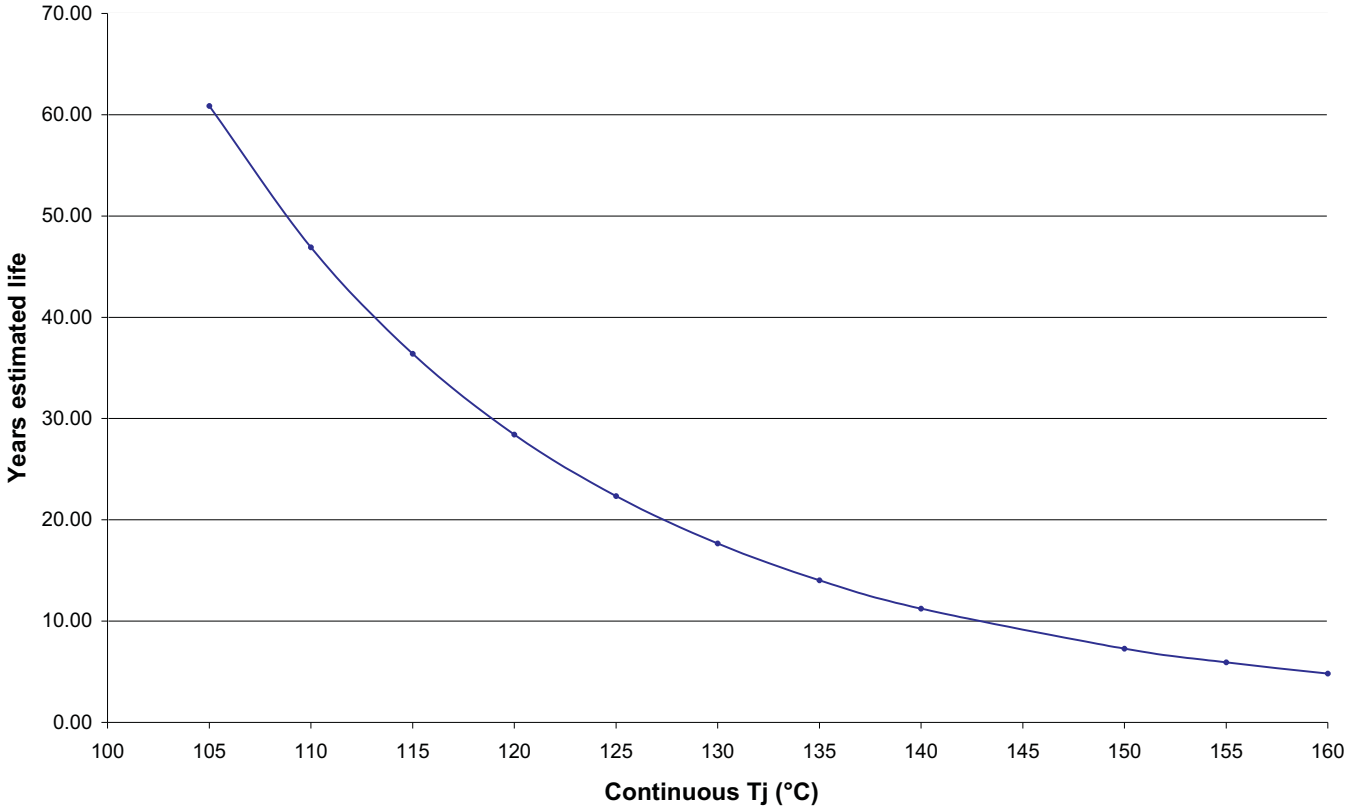


Figure 3. Estimated Device Life at Elevated Temperatures Electromigration Fail Modes

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY (DNL) vs INPUT CODE

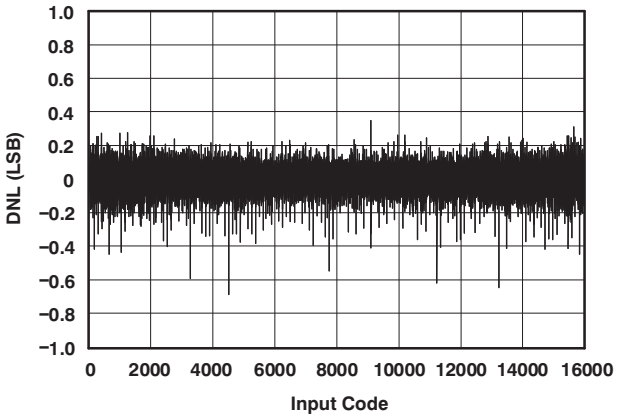


Figure 4.

INTEGRAL NONLINEARITY (INL) vs INPUT CODE

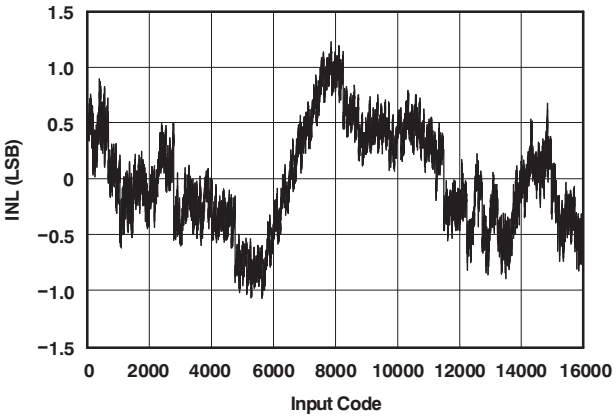


Figure 5.

TWO-TONE IMD (POWER) vs FREQUENCY

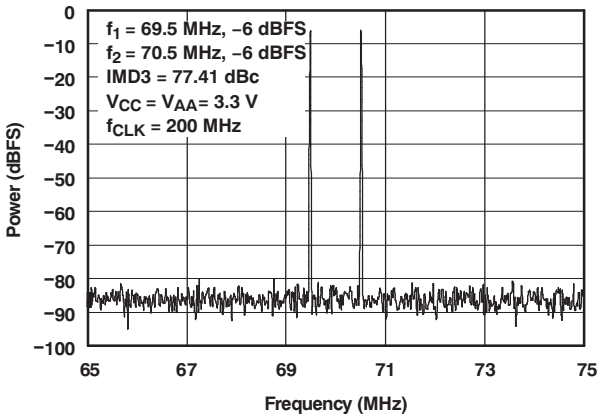


Figure 6.

TWO-TONE IMD3 vs FREQUENCY

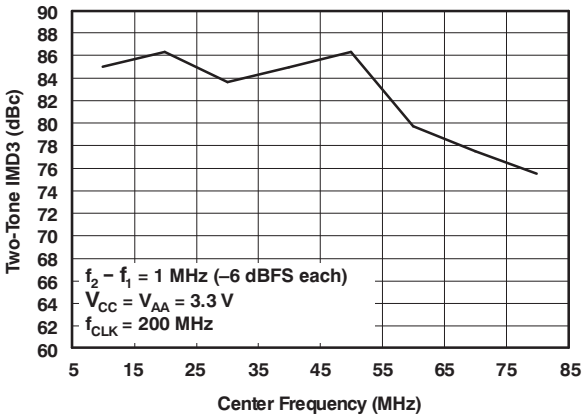


Figure 7.

TYPICAL CHARACTERISTICS (continued)

SINGLE-TONE SPECTRUM POWER VS FREQUENCY

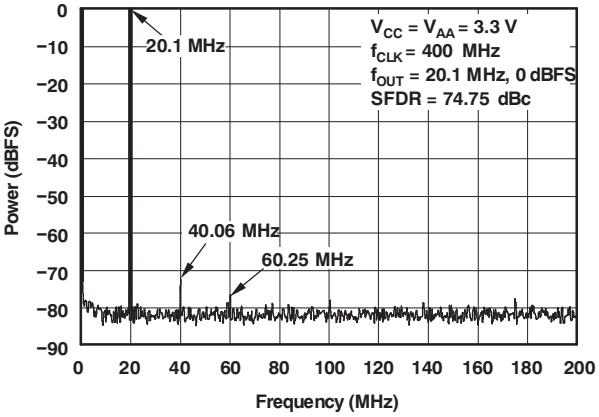


Figure 8.

SPURIOUS-FREE DYNAMIC RANGE VS FREQUENCY

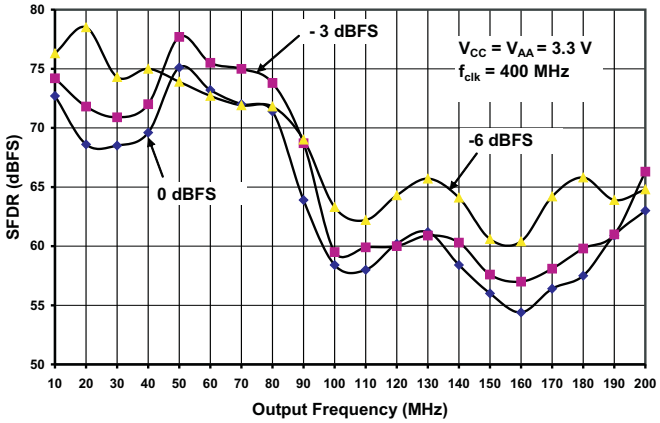


Figure 9.

SPURIOUS-FREE DYNAMIC RANGE VS FREQUENCY

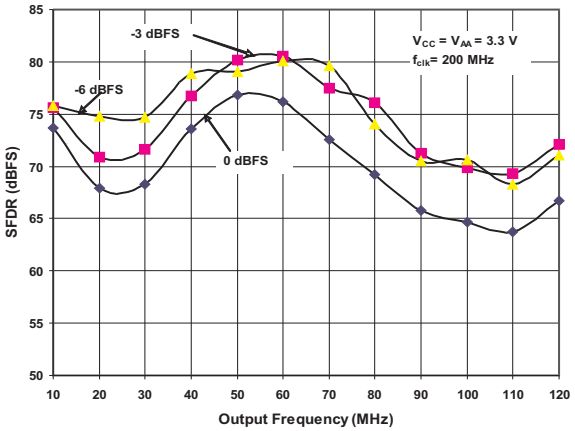


Figure 10.

W-CDMA TM1 SINGLE CARRIER POWER VS FREQUENCY

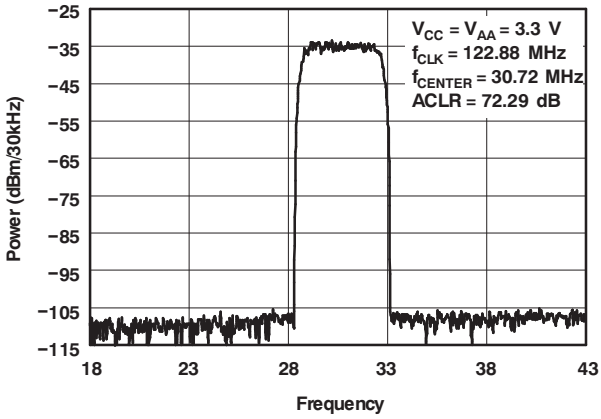


Figure 11.

TYPICAL CHARACTERISTICS (continued)

W-CDMA TM1 DUAL CARRIER POWER vs FREQUENCY

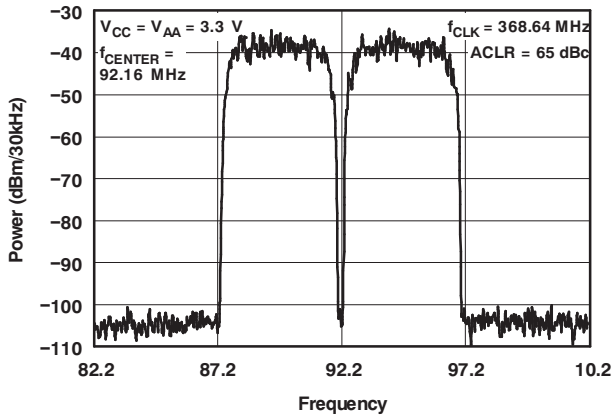


Figure 12.

W-CDMA TM1 SINGLE CARRIER ACLR vs OUTPUT FREQUENCY

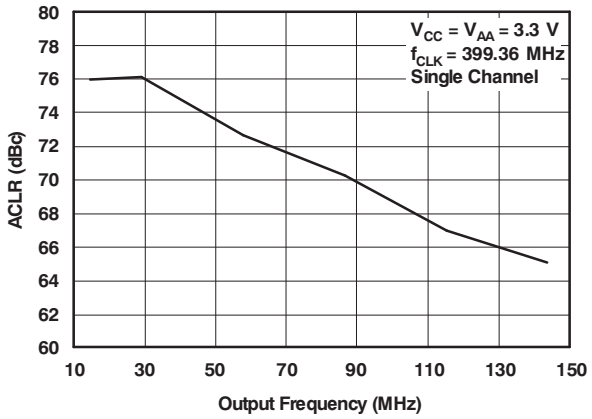


Figure 13.

APPLICATION INFORMATION

Detailed Description

Figure 14 shows a simplified block diagram of the current steering DAC5675A. The DAC5675A consists of a segmented array of NPN-transistor current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feedthrough, on-chip, and PCB noise), dc offsets, and even-order distortion components, and doubling signal output power.

The full-scale output current is set using an external resistor (R_{BIAS}) with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current (I_{BIAS}) through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 times I_{BIAS}. The full-scale current is adjustable from 20 mA down to 2 mA by using the appropriate bias resistor value.

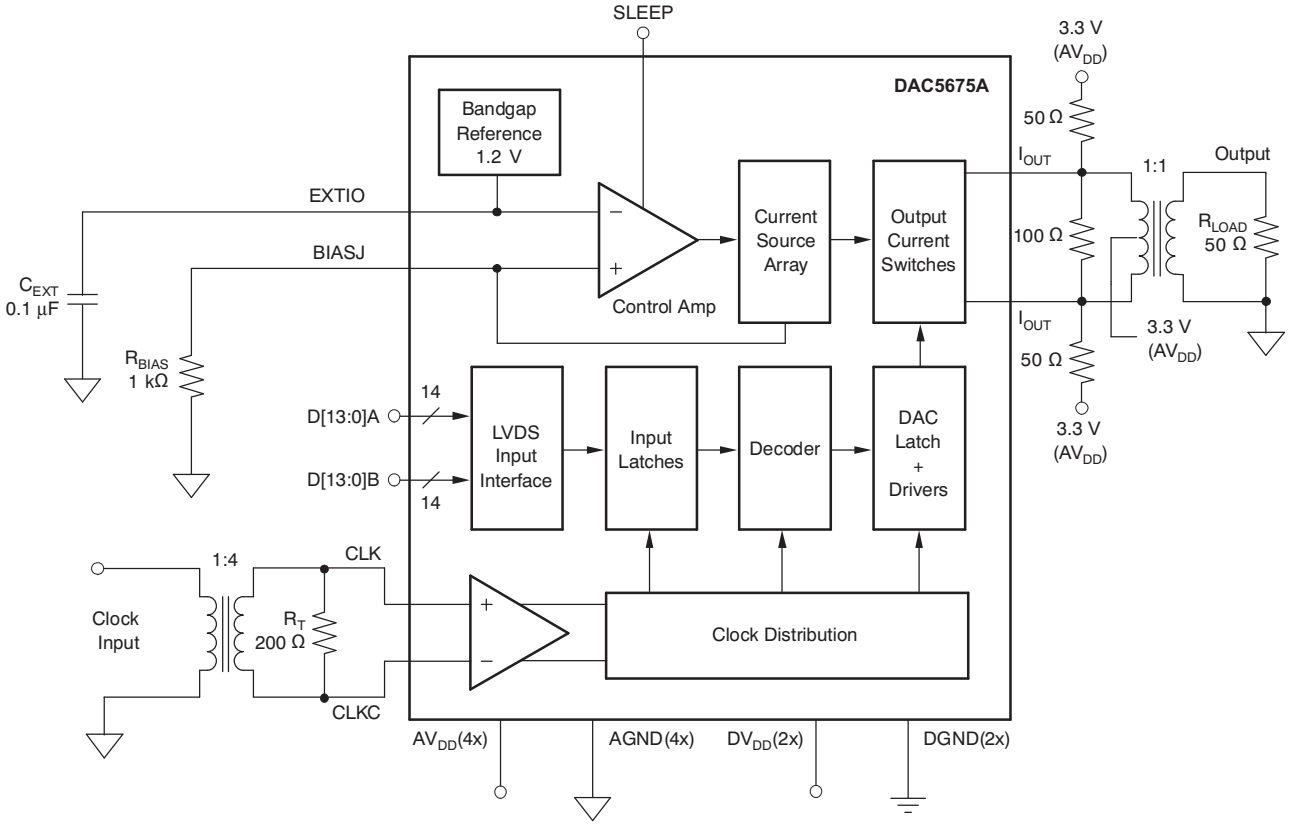


Figure 14. Application Simplified Block Diagram

Digital Inputs

The DAC5675A uses a low-voltage differential signaling (LVDS) bus input interface. The LVDS features a low differential voltage swing with low constant power consumption (4 mA per complementary data input) across frequency. The differential characteristic of LVDS allows for high-speed data transmission with low electromagnetic interference (EMI) levels. Figure 15 shows the equivalent complementary digital input interface for the DAC5675A, valid for pins D[13:0]A and D[13:0]B. Note that the LVDS interface features internal 110-Ω resistors for proper termination. Figure 2 shows the LVDS input timing measurement circuit and waveforms. A common-mode level of 1.2 V and a differential input swing of 0.8 V_{PP} is applied to the inputs.

Figure 16 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5675A, valid for the SLEEP pin.

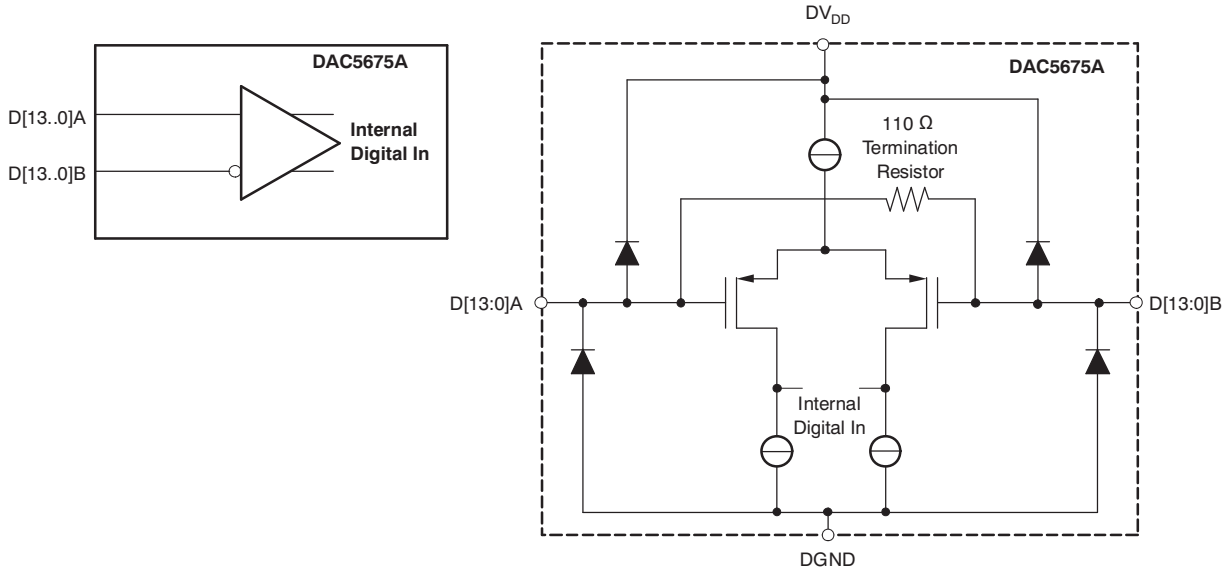


Figure 15. LVDS Digital Equivalent Input

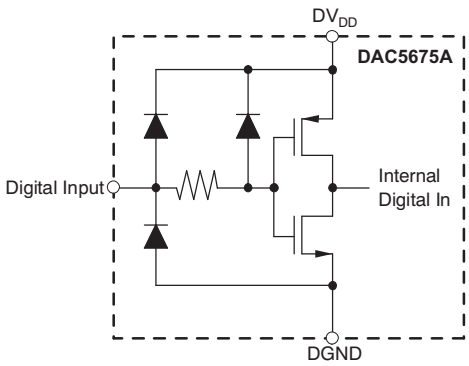


Figure 16. CMOS/TTL Digital Equivalent Input

Clock Input

The DAC5675A features differential LVPECL-compatible clock inputs (CLK, CLKC). Figure 17 shows the equivalent schematic of the clock input buffer. The internal biasing resistors set the input common-mode voltage to approximately 2 V, while the input resistance is typically 670 Ω. A variety of clock sources can be ac-coupled to the device, including a sine-wave source (see Figure 18).

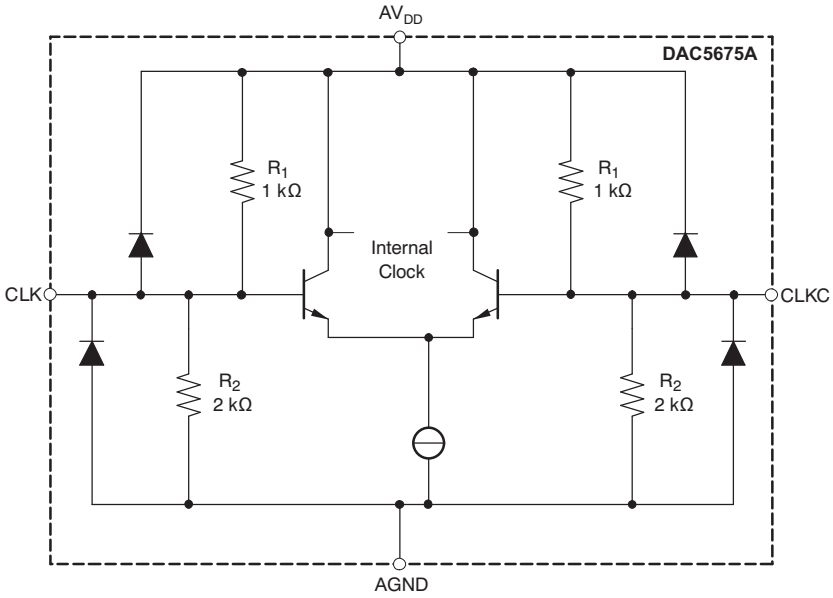


Figure 17. Clock Equivalent Input

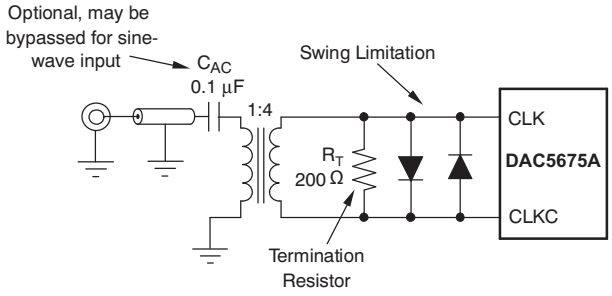


Figure 18. Driving the DAC5675A With a Single-Ended Clock Source Using a Transformer

To obtain best ac performance, the DAC5675A clock input should be driven with a differential LVPECL or sine-wave source as shown in Figure 19 and Figure 20. Here, the potential of V_{TT} should be set to the termination voltage required by the driver along with the proper termination resistors (R_T). The DAC5675A clock input can also be driven single ended; this is shown in Figure 21.

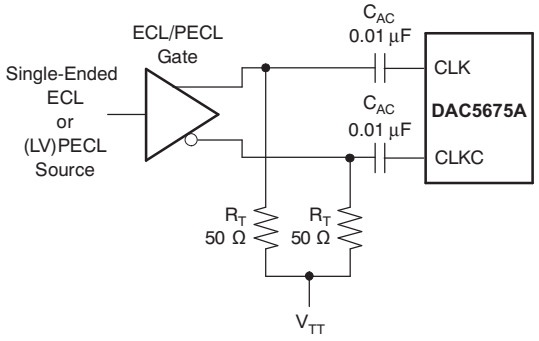


Figure 19. Driving the DAC5675A With a Single-Ended ECL/PECL Clock Source

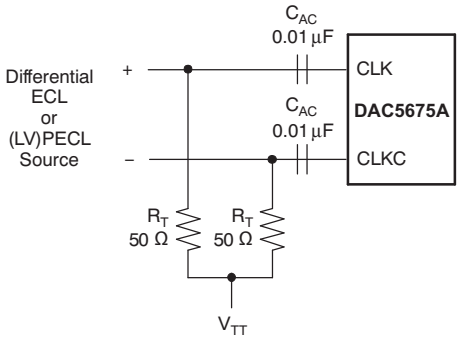


Figure 20. Driving the DAC5675A With a Differential ECL/PECL Clock Source

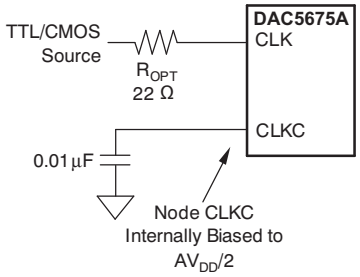


Figure 21. Driving the DAC5675A With a Single-Ended TTL/CMOS Clock Source

Supply Inputs

The DAC5675A comprises separate analog and digital supplies, (AV_{DD} and DV_{DD}) respectively. These supply inputs can be set independently from 3.6 V down to 3.15 V.

DAC Transfer Function

The DAC5675A has a current sink output. The current flow through IOUT1 and IOUT2 is controlled by D[13:0]A and D[13:0]B. For ease of use, D[13:0] is denoted as the logical bit equivalent of D[13:0]A and its complement D[13:0]B. The DAC5675A supports straight binary coding with D13 being the MSB and D0 the LSB. Full-scale current flows through IOUT2 when all D[13:0] inputs are set high and through IOUT1 when all D[13:0] inputs are set low. The relationship between IOUT1 and IOUT2 can be expressed as Equation 1:

$$IOUT1 = IO_{(FS)} - IOUT2 \quad (1)$$

$IO_{(FS)}$ is the full-scale output current sink (2 mA to 20 mA). Because the output stage is a current sink, the current can only flow from AV_{DD} through the load resistors R_L into the IOUT1 and IOUT2 pins.

The output current flow in each pin driving a resistive load can be expressed as shown in Figure 22, as well as in Equation 2 and Equation 3.

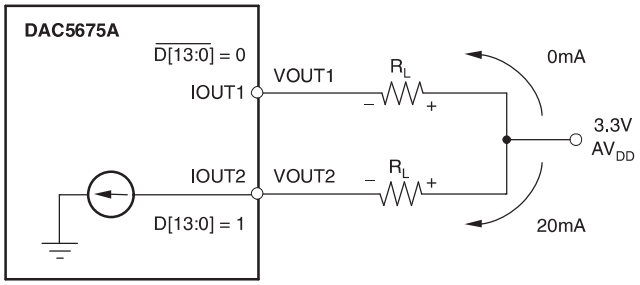


Figure 22. Relationship Between D[13:0], IOUT1 and IOUT2

$$IOUT1 = \frac{IO_{(FS)} \times (16383 - CODE)}{16384} \quad (2)$$

$$IOUT2 = \frac{IO_{(FS)} \times CODE}{16384} \quad (3)$$

where CODE is the decimal representation of the DAC input word. This would translate into single-ended voltages at IOUT1 and IOUT2, as shown in Equation 4 and Equation 5:

$$VOUT1 = AVDD - IOUT1 \times R_L \quad (4)$$

$$VOUT2 = AVDD - IOUT2 \times R_L \quad (5)$$

Assuming that D[13:0] = 1 and the R_L is 50Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as shown in Equation 6 through Equation 8:

$$VOUT1 = 3.3V - 0mA \times 50 = 3.3V \quad (6)$$

$$VOUT2 = AVDD - 20mA \times 50 = 2.3V \quad (7)$$

$$VDIFF = VOUT1 - VOUT2 = 1V \quad (8)$$

If D[13:0] = 0, then IOUT2 = 0mA and IOUT1 = 20mA and the differential voltage VDIFF = –1V.

The output currents and voltages in IOUT1 and IOUT2 are complementary. The voltage, when measured differentially, is doubled compared to measuring each output individually. Care must be taken not to exceed the compliance voltages at the IOUT1 and IOUT2 pins to keep signal distortion low.

Reference Operation

The DAC5675A has a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IO_{(FS)}$ is thus expressed as Equation 9:

$$I_{O(FS)} = 16 \times I_{BIAS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}} \quad (9)$$

where V_{EXTIO} is the voltage at terminal EXTIO. The bandgap reference voltage delivers a stable voltage of 1.2 V. This reference can be overridden by applying an external voltage to terminal EXTIO. The bandgap reference can additionally be used for external reference operation. In such a case, an external buffer amplifier with high impedance input should be selected to limit the bandgap load current to less than 100 nA. The capacitor C_{EXT} may be omitted. Terminal EXTIO serves as either an input or output node. The full-scale output current is adjustable from 20 mA down to 2 mA by varying resistor R_{BIAS}.

Analog Current Outputs

Figure 23 shows a simplified schematic of the current source array output with corresponding switches. Differential NPN switches direct the current of each individual NPN current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches and is >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to the positive supply AV_{DD}.

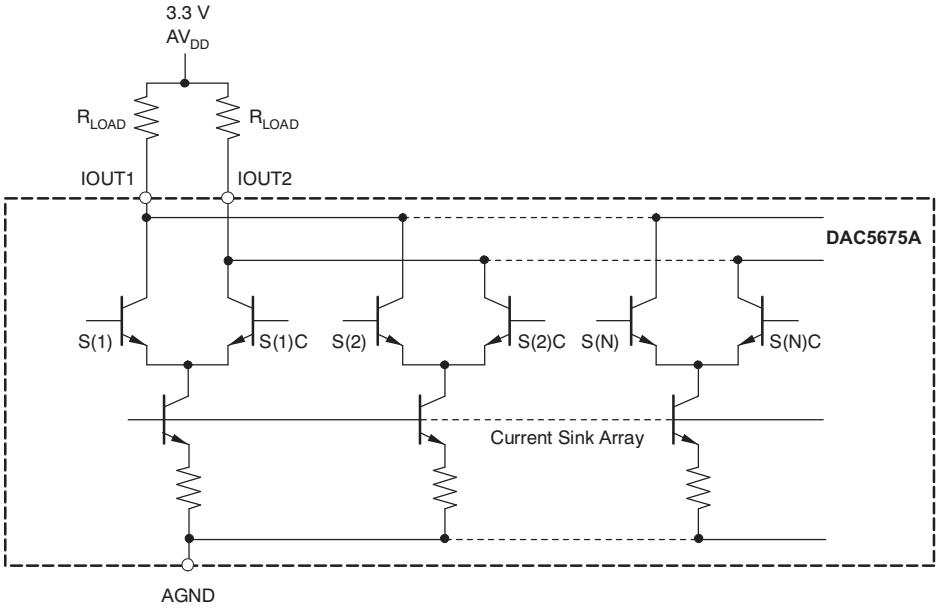


Figure 23. Equivalent Analog Current Output

The DAC5675A easily can be configured to drive a doubly-terminated 50-Ω cable using a properly selected transformer. Figure 24 and Figure 25 show the 1:1 and 4:1 impedance ratio configuration, respectively. These configurations provide maximum rejection of common-mode noise sources and even-order distortion components, thereby doubling the power of the DAC to the output. The center tap on the primary side of the transformer is terminated to AV_{DD}, enabling a dc-current flow for both IOUT1 and IOUT2. Note that the ac performance of the DAC5675A is optimum and specified using a 1:1 differential transformer-coupled output.

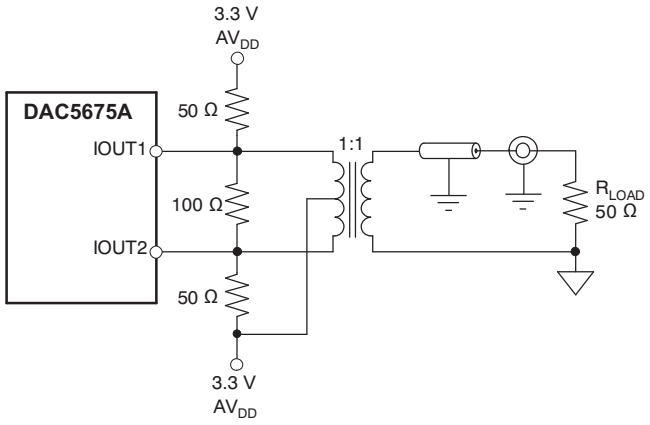


Figure 24. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

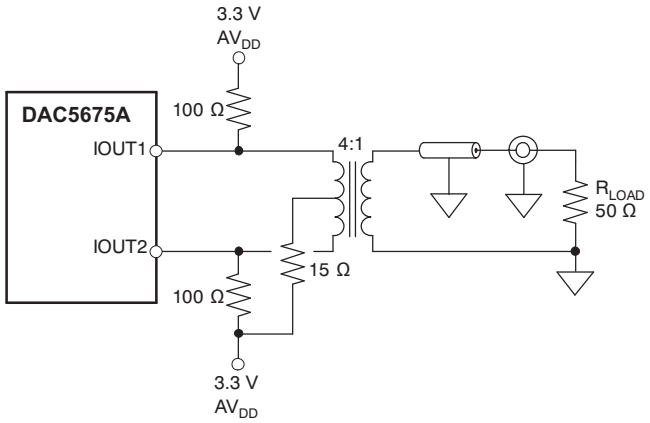


Figure 25. Driving a Doubly Terminated 50 Ω Cable Using a 4:1 Impedance Ratio Transformer

Figure 26(a) shows the typical differential output configuration with two external matched resistor loads. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} (0.5 V_{PP} single ended) when applying a 20-mA full-scale output current. The output impedance of the DAC5675A slightly depends on the output voltage at nodes IOUT1 and IOUT2. Consequently, for optimum dc-integral nonlinearity, the configuration of Figure 26(b) should be chosen. In this current/voltage (I-V) configuration, terminal IOUT1 is kept at AV_{DD} by the inverting operational amplifier. The complementary output should be connected to AV_{DD} to provide a dc-current path for the current sources switched to IOUT1. The amplifier maximum output swing and the full-scale output current of the DAC determine the value of the feedback resistor R_{FB}. The capacitor C_{FB} filters the steep edges of the DAC5675A current output, thereby reducing the operational amplifier slew-rate requirements. In this configuration, the operational amplifier should operate at a supply voltage higher than the resistor output reference voltage AV_{DD} as a result of its positive and negative output swing around AV_{DD}. Node IOUT1 should be selected if a single-ended unipolar output is desired.

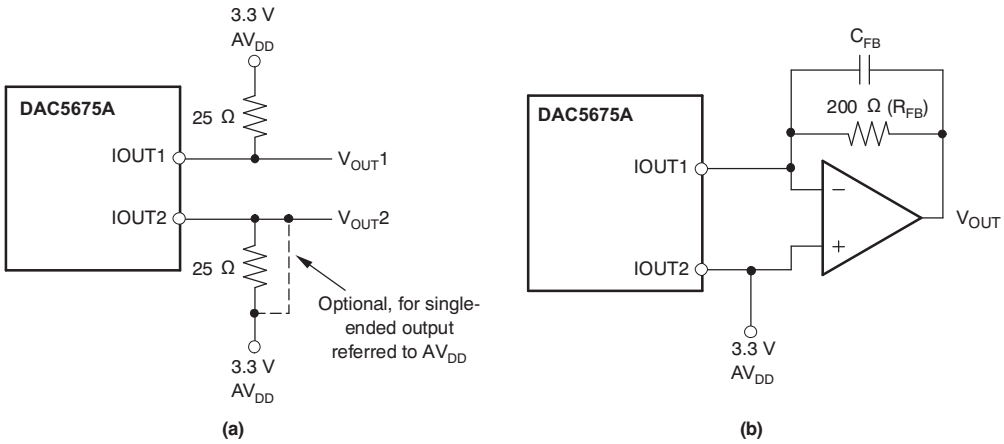


Figure 26. Output Configurations

Sleep Mode

The DAC5675A features a power-down mode that turns off the output current and reduces the supply current to approximately 6 mA. The power-down mode is activated by applying a logic level one to the SLEEP pin, pulled down internally.

DEFINITIONS

Definitions of Specifications and Terminology

Gain error is as the percentage error in the ratio between the measured full-scale output current and the value of 16 × $V_{(EXTIO)}/R_{BIAS}$. A $V_{(EXTIO)}$ of 1.25 V is used to measure the gain error with an external reference voltage applied. With an internal reference, this error includes the deviation of $V_{(EXTIO)}$ (internal bandgap reference voltage) from the typical value of 1.25 V.

Offset error is as the percentage error in the ratio of the differential output current (IOUT1-IOUT2) and the half of the full-scale output current for input code 8192.

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental output signal.

SNR is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

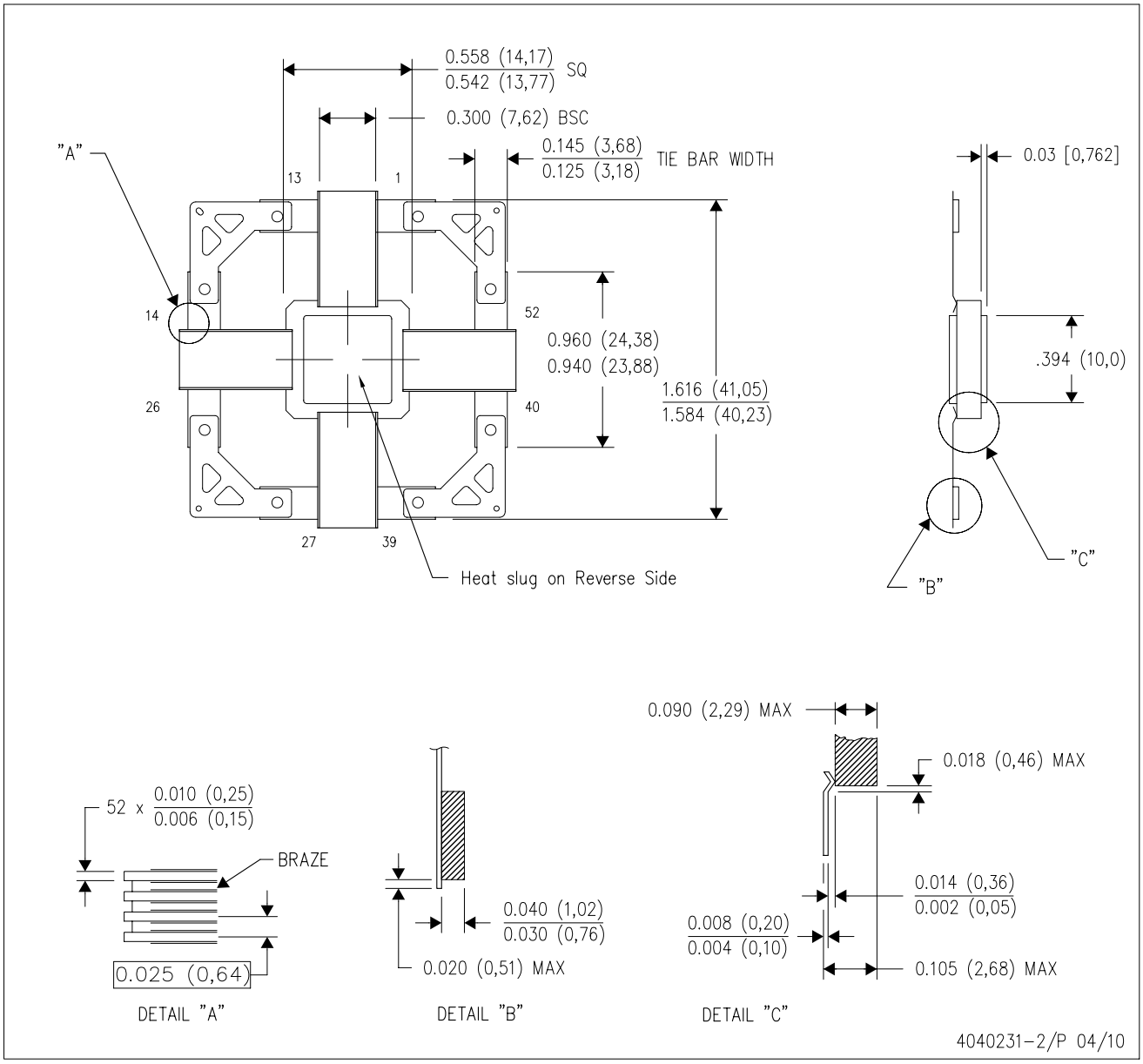
SINAD is the ratio of the rms value of the fundamental output signal to the rms sum of all other spectral components below the Nyquist frequency, including noise and harmonics, but excluding dc.

ACPR or adjacent channel power ratio is defined for a 3.84-Mcps 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

APSSR or analog power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the analog power supply AV_{DD} from the nominal. This is a dc measurement.

DPSSR or digital power supply ratio is the percentage variation of full-scale output current versus a 5% variation of the digital power supply DV_{DD} from the nominal. This is a dc measurement.

HFG (S–CQFP–F52) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

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