

Am29BL802C

[查询"AM29BL802CB-80RDGE"供应商](#)
Known Good Die

Data Sheet



July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **23694** Revision **A** Amendment **+2** Issue Date **September 13, 2002**





Am29BL802C Known Good Die

8 Megabit (512 K x 16-Bit)

CMOS 3.0 Volt-only, Burst-mode, Boot Sector Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **32 words sequential with wrap around (linear 32), bottom boot**
- **One 8 Kword, two 4 Kword, one 48 Kword, three 64 Kword, and two 128 Kword sectors**
- **Single power supply operation**
 - Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Read access times**
 - 22 ns burst access at extended temperature range
 - 80 ns initial/random access
- **Alterable burst length via BAA# pin**
- **Power dissipation (typical)**
 - Burst Mode Read: 15 mA @ 25 MHz, 20 mA @ 33 MHz, 25 mA @ 40 MHz
 - Program/Erase: 20 mA
 - Standby mode, CMOS: 22 μ A
- **5 V-tolerant data, address, and control signals**
- **Sector Protection**
 - Implemented using in-system or via programming equipment
 - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
 - Reduces overall programming time when issuing multiple program command sequences
- **Embedded Algorithms**
 - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
 - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**
- **Compatibility with JEDEC standards**
 - Pinout and software compatible with single-power supply Flash
 - Superior inadvertent write protection
 - Backward-compatible with AMD Am29LV and Am29F flash memories: powers up in asynchronous mode for system boot, but can immediately be placed into burst mode
- **Data# Polling and toggle bits**
 - Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
 - Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
 - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
 - Hardware method to reset the device for reading array data
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

GENERAL DESCRIPTION

查询 "AM29BL802CD-80RDGE1" 供应商

The Am29BL802C in Known Good Die (KGD) form is an 8 Mbit, 3.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29BL802C Features

The Am29BL802C is an 8 Mbit, 3.0 Volt-only burst mode Flash memory devices organized as 524, 288 words. These devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply. A 12.0-volt V_{PP} or 5.0 V_{CC} is not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers an access time of 80 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Burst Mode Features

The Am29BL802C offers a Linear Burst mode—a 32 word sequential burst with wrap around—in a bottom boot configuration only. This devices require additional control pins for **burst operations**: Load Burst Address (LBA#), Burst Address Advance (BAA#), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

AMD Flash Memory Features

Each device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. The I/O and control signals are 5V tolerant.

The Am29BL802C is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically pre-

programs the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Electrical Specifications

Refer to the Am29BL802C data sheet, publication number 22371, for full electrical specifications on the Am29BL802C in KGD form.

PRODUCT SELECTOR GUIDE

[查询 AM29BL802C 80RDCEP 供应商](#)

Family Part Number		Am29BL802C
Speed (ns)	Regulated Voltage Range: $V_{CC} = 3.0\text{--}3.6\text{ V}$	80R
Max access time, ns (t_{ACC} , t_{IACC})		80
Max CE# access time, ns (t_{CE})		80
Max OE# access time, ns (t_{OE})		22 (at 30 pF loading)

AC CHARACTERISTICS

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Burst Mode Read

Parameter		Description		Speed Options and Temperature Ranges	Unit
JEDEC	Std.			80R	
	t_{IACC}	Initial Access Time LBA# Valid Clock to Output Delay (See Note)	Max	80	ns
	t_{BACC}	Burst Access Time BAA# Valid Clock to Output Delay	Max	24	ns
	t_{LBAS}	LBA# Setup Time	Min	6	ns
	t_{LBAH}	LBA# Hold Time	Min	2	ns
	t_{BAAS}	BAA# Setup Time	Min	6	ns
	t_{BAAH}	BAA# Hold Time	Min	2	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4	ns
	t_{ACS}	Address Setup Time to CLK (See Note)	Min	6	ns
	t_{ACH}	Address Hold Time from CLK (See Note)	Min	2	ns
	t_{OE}	Output Enable to Output Valid	Max	24	ns
	t_{OEZ}	Output Enable to Output High Z	Max	25	ns
	t_{CEZ}	Chip Enable to Output High Z	Min	25	ns
	t_{CES}	CE# Setup Time to Clock	Min	6	ns

Note: Initial valid data will be output after second clock rising edge of LBA# assertion.

AC CHARACTERISTICS

[查询"Am29BL802CB-80R"供应商](#)

Erase/Program Operations

Parameter		Description		Speed Options	Unit
JEDEC	Std			80R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	80	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min		ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	35	ns
t_{WHDx}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3	sec
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50	μ s
	t_{RB}	Recovery Time from RY/BY#	Min	0	ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay	Min	90	ns

Notes:

1. Not 100% tested.

AC CHARACTERISTICS

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Alternate CE# Controlled Erase/Program Operations

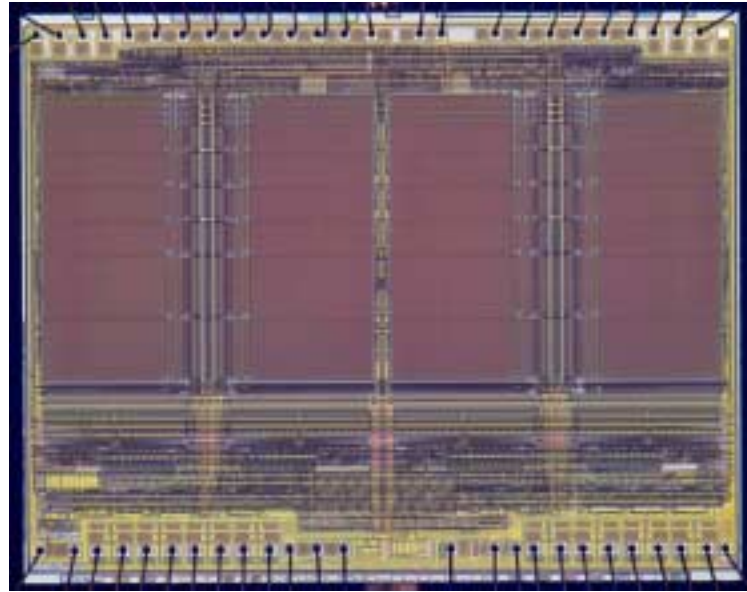
Parameter		Description		Speed Options	Unit
JEDEC	Std			80R	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	80	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min		ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30	ns
t_{WHWSH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	μ s
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	3	sec

Notes:

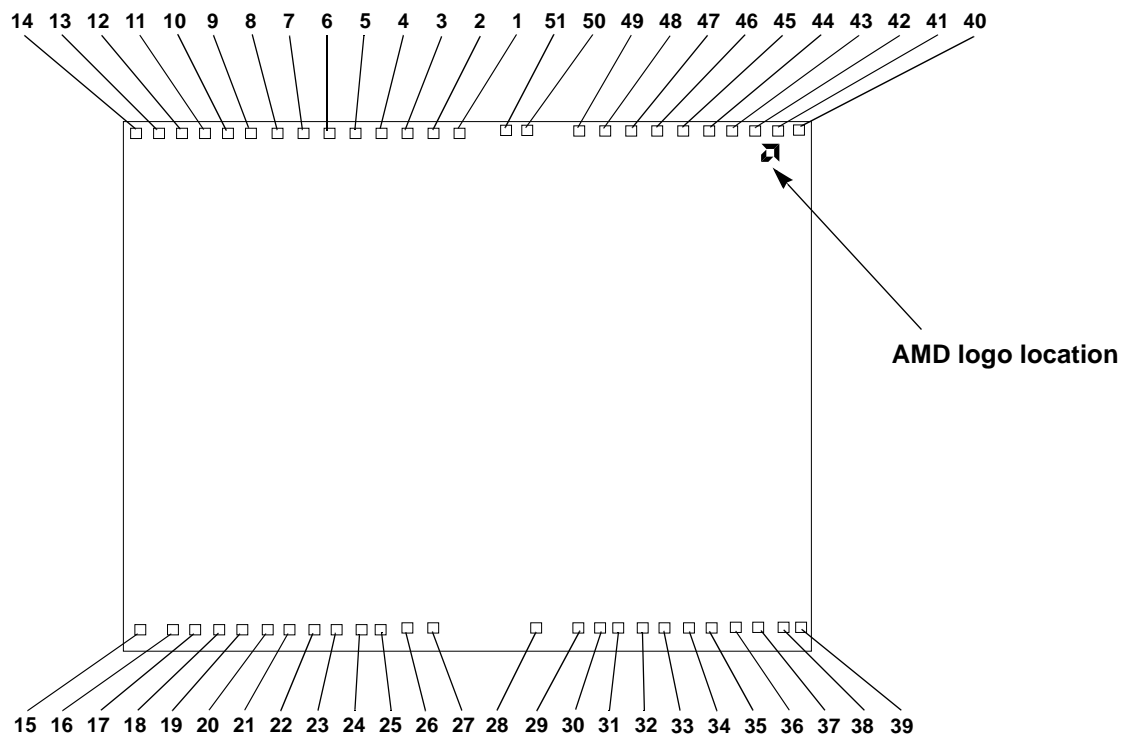
1. Not 100% tested.
2. See the “Erase and Programming Performance” section for more information.

DIE PHOTOGRAPH

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DIE PAD LOCATIONS



PAD DESCRIPTION
[查询"AM29BL802CB-80RDGE1"供应商](#)

Pads relative to die center.

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	WE#	-3.11	98.18	-0.0790	2.4938
2	RESET#	-13.41	98.18	-0.3406	2.4938
3	RY/BY#	-23.34	98.18	-0.5929	2.4938
4	A18	-33.39	98.18	-0.8482	2.4938
5	A17	-43.44	98.18	-1.1034	2.4938
6	A7	-53.49	98.18	-1.3587	2.4938
7	A6	-63.54	98.18	-1.6140	2.4938
8	A5	-73.59	98.18	-1.8692	2.4938
9	A4	-83.64	98.18	-2.1245	2.4938
10	A3	-93.69	98.18	-2.3798	2.4938
11	A2	-102.32	98.18	-2.5988	2.4938
12	A1	-110.94	98.18	-2.8179	2.4938
13	A0	-119.57	98.18	-3.0370	2.4938
14	CE#	-128.19	98.18	-3.2560	2.4938
15	V _{SS}	-128.19	-94.14	-3.2560	-2.3912
16	OE#	-114.94	-94.14	-2.9194	-2.3912
17	DQ0	-106.36	-94.14	-2.7015	-2.3912
18	DQ8	-96.72	-94.14	-2.4566	-2.3912
19	DQ1	-88.15	-94.14	-2.2391	-2.3912
20	DQ9	-78.51	-94.14	-1.9941	-2.3912
21	DQ2	-69.94	-94.14	-1.7766	-2.3912
22	DQ10	-60.30	-94.14	-1.5317	-2.3912
23	DQ3	-51.74	-94.14	-1.3141	-2.3912
24	DQ11	-42.10	-94.14	-1.0692	-2.3912
25	V _{SS}	-34.48	-94.14	-0.8758	-2.3912

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
26	CLK	-24.43	-94.14	-0.6205	-2.3912
27	BAA#	-14.38	-94.14	-0.3653	-2.3912
28	IND#	25.76	-94.14	0.6543	-2.3912
29	V _{CC}	42.04	-94.14	1.0678	-2.3912
30	V _{CC}	50.19	-94.14	1.2749	-2.3912
31	DQ4	57.06	-94.14	1.4493	-2.3912
32	DQ12	66.70	-94.14	1.6942	-2.3912
33	DQ5	75.27	-94.14	1.9118	-2.3912
34	DQ13	84.91	-94.14	2.1567	-2.3912
35	DQ6	93.47	-94.14	2.3742	-2.3912
36	DQ14	103.12	-94.14	2.6192	-2.3912
37	DQ7	111.68	-94.14	2.8367	-2.3912
38	DQ15	121.32	-94.14	3.0816	-2.3912
39	V _{SS}	128.19	-94.14	3.2560	-2.3912
40	NC	128.19	98.18	3.2560	2.4938
41	A16	119.57	98.18	3.0370	2.4938
42	A15	110.94	98.18	2.8179	2.4938
43	A14	102.32	98.18	2.5988	2.4938
44	A13	93.69	98.18	2.3798	2.4938
45	A12	83.64	98.18	2.1245	2.4938
46	A11	73.59	98.18	1.8692	2.4938
47	A10	63.54	98.18	1.6140	2.4938
48	A9	53.49	98.18	1.3587	2.4938
49	A8	43.20	98.18	1.0972	2.4938
50	V _{CC}	23.10	98.18	0.5866	2.4938
51	LBA#	14.94	98.18	0.3795	2.4938

Note: The coordinates above are relative to the die center and can be used to operate wire bonding equipment.

PAD DESCRIPTION
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Pads relative to V_{CC} .

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	WE#	-26.21	0.00	-0.6656	0.0000
2	RESET#	-36.51	0.00	-0.9272	0.0000
3	RY/BY#	-46.44	0.00	-1.1795	0.0000
4	A18	-56.49	0.00	-1.4348	0.0000
5	A17	-66.54	0.00	-1.6900	0.0000
6	A7	-76.59	0.00	-1.9453	0.0000
7	A6	-86.64	0.00	-2.2006	0.0000
8	A5	-96.69	0.00	-2.4558	0.0000
9	A4	-106.74	0.00	-2.7111	0.0000
10	A3	-116.79	0.00	-2.9664	0.0000
11	A2	-125.42	0.00	-3.1854	0.0000
12	A1	-134.04	0.00	-3.4045	0.0000
13	A0	-142.67	0.00	-3.6236	0.0000
14	CE#	-151.29	0.00	-3.8426	0.0000
15	V_{SS}	-151.29	-192.32	-3.8426	-4.8850
16	OE#	-138.04	-192.32	-3.5060	-4.8850
17	DQ0	-129.46	-192.32	-3.2881	-4.8850
18	DQ8	-119.82	-192.32	-3.0432	-4.8850
19	DQ1	-111.25	-192.32	-2.8257	-4.8850
20	DQ9	-101.61	-192.32	-2.5807	-4.8850
21	DQ2	-93.04	-192.32	-2.3632	-4.8850
22	DQ10	-83.40	-192.32	-2.1183	-4.8850
23	DQ3	-74.84	-192.32	-1.9007	-4.8850
24	DQ11	-65.20	-192.32	-1.6558	-4.8850
25	V_{SS}	-57.58	-192.32	-1.4624	-4.8850

Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
26	CLK	-47.53	-192.32	-1.2071	-4.8850
27	BAA#	-37.48	-192.32	-0.9519	-4.8850
28	IND#	2.66	-192.32	0.0677	-4.8850
29	V_{CC}	18.94	-192.32	0.4812	-4.8850
30	V_{CC}	27.09	-192.32	0.6883	-4.8850
31	DQ4	33.96	-192.32	0.8627	-4.8850
32	DQ12	43.60	-192.32	1.1076	-4.8850
33	DQ5	52.17	-192.32	1.3252	-4.8850
34	DQ13	61.81	-192.32	1.5701	-4.8850
35	DQ6	70.37	-192.32	1.7876	-4.8850
36	DQ14	80.02	-192.32	2.0326	-4.8850
37	DQ7	88.58	-192.32	2.2501	-4.8850
38	DQ15	98.22	-192.32	2.4950	-4.8850
39	V_{SS}	105.09	-192.32	2.6694	-4.8850
40	NC	105.09	0.00	2.6694	0.0000
41	A16	96.47	0.00	2.4504	0.0000
42	A15	87.84	0.00	2.2313	0.0000
43	A14	79.22	0.00	2.0122	0.0000
44	A13	70.59	0.00	1.7932	0.0000
45	A12	60.54	0.00	1.5379	0.0000
46	A11	50.49	0.00	1.2826	0.0000
47	A10	40.44	0.00	1.0274	0.0000
48	A9	30.39	0.00	0.7721	0.0000
49	A8	20.10	0.00	0.5106	0.0000
50	V_{CC}	0.00	0.00	0.0000	0.0000
51	LBA#	-8.16	0.00	-0.2071	0.0000

Note: The coordinates above are relative to the V_{CC} location and can be used to operate wire bonding equipment.

ORDERING INFORMATION

[查询 AM29BL802CB-80RDGE1"供应商"](#)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29BL802C	B	80R	DP	E	1	
						DIE REVISION This number refers to the specific AMD manufacturing process and product technology reflected in this document. It is entered in the revision field of AMD standard product nomenclature.
						TEMPERATURE RANGE I = Industrial (–40°C to +85°C) E = Extended (–55°C to +125°C) H = Super Extended (–55°C to +145°C)
						PACKAGE TYPE AND MINIMUM ORDER QUANTITY DP = Waffle Pack 125 die per 5 tray stack DG = Gel-Pak® Die Tray 336 die per 6 tray stack DT = Surftape™ (Tape and Reel) 1600 per 7-inch reel DW = Gel-Pak® Wafer Tray (sawn wafer on frame) Call AMD sales office for minimum order quantity
						SPEED OPTION See Product Selector Guide and Valid Combinations
						BOOT CODE SECTOR ARCHITECTURE B = Bottom boot sector
						DEVICE NUMBER/DESCRIPTION Am29BL802C Known Good Die 8 Megabit (512 K x 16-Bit) CMOS Flash Memory—Die Revision 1 3.0 Volt-only Program and Erase

Valid Combinations	
AM29BL802CB-80R (30 pF loading)	DPI 1, DPE 1, DPH 1 DGI 1, DGE 1, DGH 1 DTI 1, DTE 1, DTH 1 DWI 1, DWE 1, DWH 1

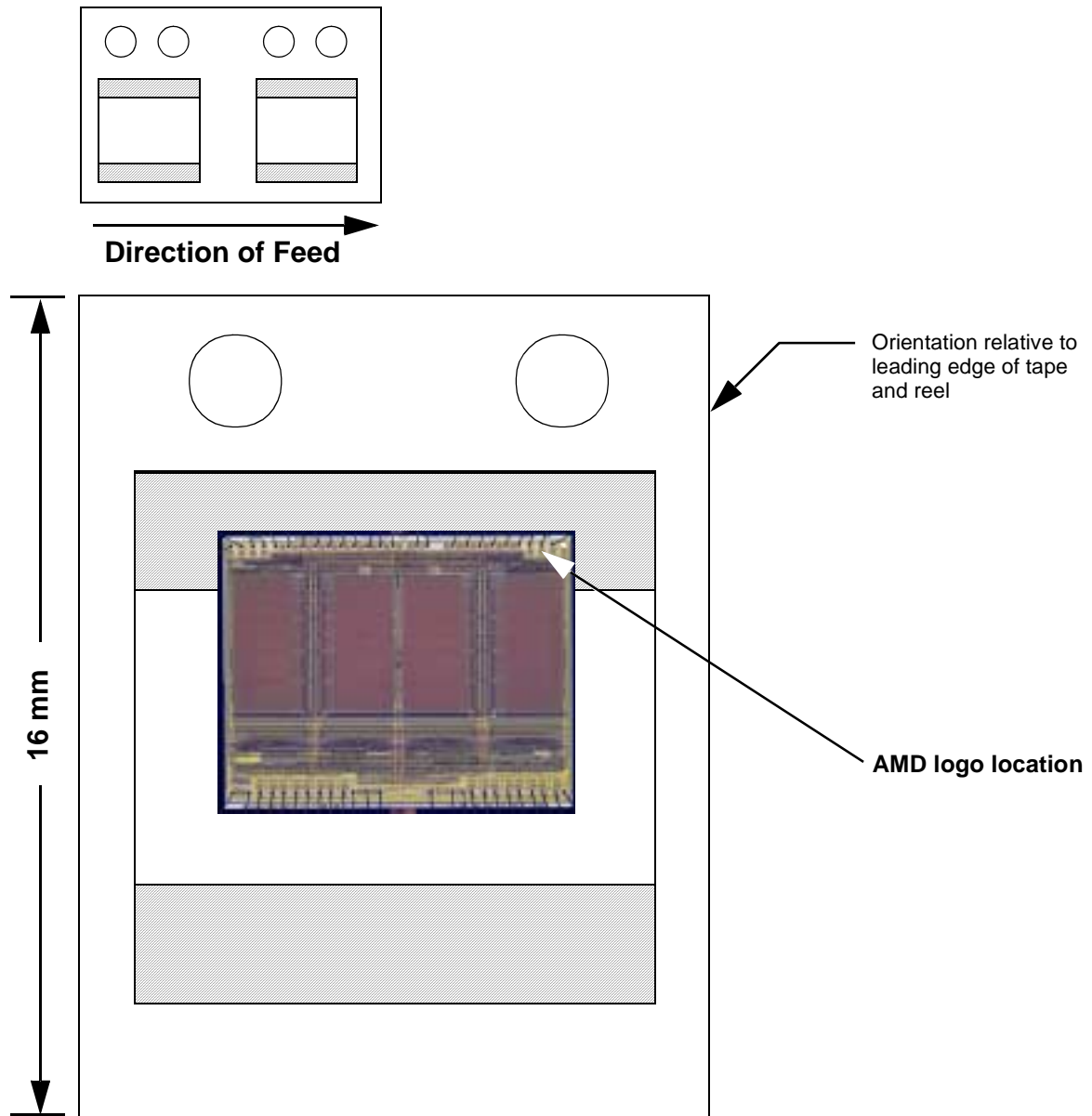
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

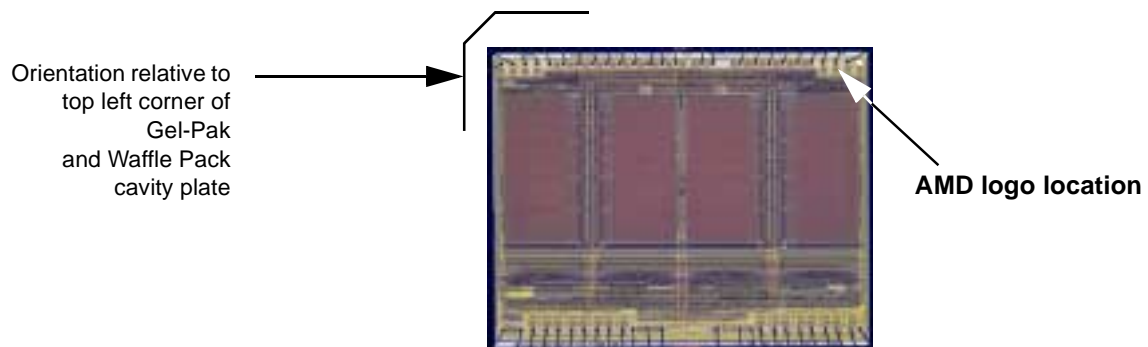
PACKAGING INFORMATION

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Surftape Packaging



Gel-Pak and Waffle Pack Packaging



PRODUCT TEST FLOW

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Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29BL802C product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition,

an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

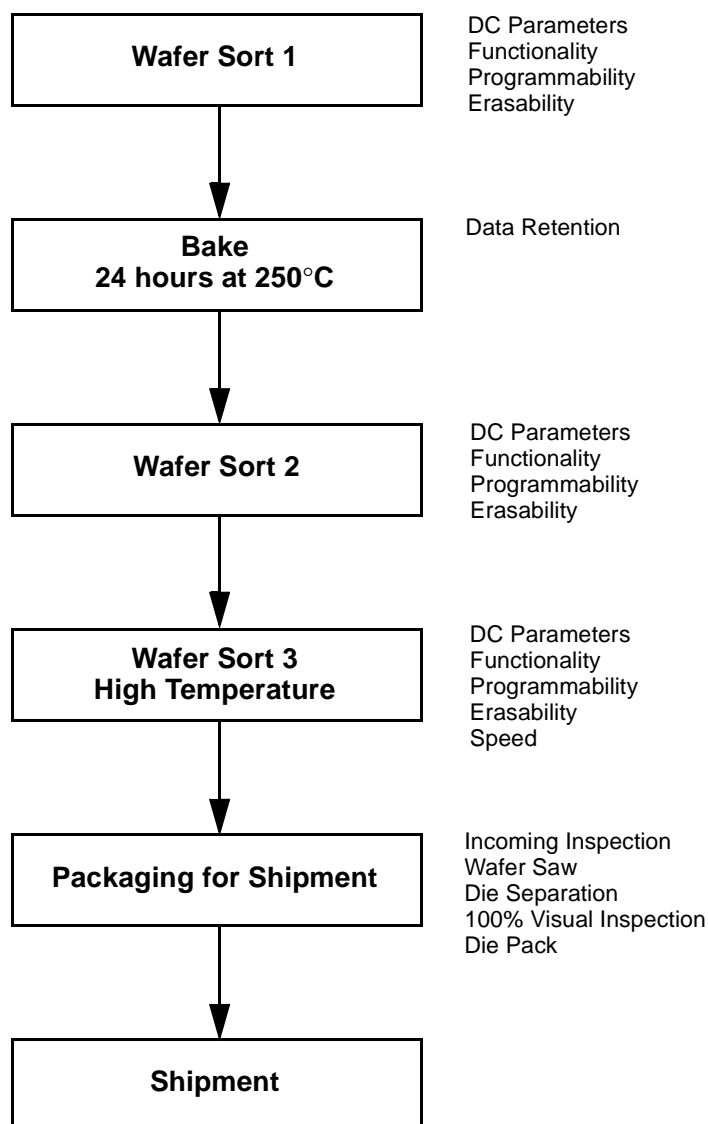


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

查词 AM29BL802CB-60RDCE1 供应商

Die dimensions	269.7 mils x 214.2 mils
	6.85 mm x 5.44 mm
Die Thickness	500 μ m
Bond Pad Size	3.74 mils x 3.74 mils
	95 μ m x 95 μ m
Pad Area Free of Passivation	13.99 mils ²
	9,025 μ m ²
Pads Per Die	51
Bond Pad Metalization	Al/Cu
Die Backside	No metal, may be grounded (optional)
Passivation	Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage)	3.0 V to 3.6 V
Operating Temperature	
Industrial	-40°C to +85°C
Extended	-55°C to +125°C
Super Extended	-55°C to +145°C

MANUFACTURING INFORMATION

Manufacturing	FASL
Wafer Sort Test	Sunnyvale, CA, USA, and Penang, Malaysia
Manufacturing ID (Bottom Boot)	98H11
Preparation for Shipment	Penang, Malaysia
Fabrication Process	CS39LS
Die Revision	1

SPECIAL HANDLING INSTRUCTIONS**Processing**

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

DC PARAMETER EXCEPTIONS

The following specifications replace those given in the Am29BL802 data sheet (publication number 22371):

Parameter	Description	Test Conditions		Typ	Max	Unit
I_{CC3}	V_{CC} Standby Current (Note 3)	$CE\#, RESET\# = V_{CC} \pm 0.3 V$		22	35	μA
I_{CC4}	V_{CC} Standby Current During Reset (Note 3)	$RESET\# = V_{SS} \pm 0.3 V$		22	35	μA
I_{CC5}	Automatic Sleep Mode (Notes 3, 4)	$V_{IH} = V_{CC} \pm 0.3 V$; $V_{IL} = V_{SS} \pm 0.3 V$	$OE\# = V_{IH}$	30	50	μA
			$OE\# = V_{IL}$	30	50	μA

Notes:

- Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.
- Automatic sleep mode enables the low power mode when addresses remain stable for $t_{ACC} + 30 ns$.

AC CHARACTERISTICS

[查询"AM29BL802CB-80RDGE1"供应商](#)

Read Operations

Parameter		Description		Test Setup		Speed Options and Temperature Ranges	Unit
JEDEC	Std.					80R	
t _{AVAV}	t _{RC}	Read Cycle Time (Note)			Min	80	ns
t _{AVQV}	t _{ACC}	Address to Output Delay		CE# = V _{IL} OE# = V _{IL}	Max	80	ns
t _{ELQV}	t _{CE}	Chip Enable to Output Delay		OE# = V _{IL}	Max	80	ns
t _{GLQV}	t _{OE}	Output Enable to Output Delay			Max	24	ns
t _{EHQZ}	t _{DF}	Chip Enable to Output High Z (Note)			Max	24	ns
t _{GHQZ}	t _{DF}	Output Enable to Output High Z (Note)			Max	25	ns
	t _{OEh}	Output Enable Hold Time (Note)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns
t _{AXQX}	t _{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note)			Min	0	ns

Not 100% tested.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to unpackaged die under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

AMD warrants unpackaged die of its manufacture ("Known Good Die" or "Die") against defective materials or workmanship for a period of one (1) year from date of shipment. This warranty does not extend beyond the first purchaser of said Die. Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of Known Good Die (including but not limited to proper Die preparation, Die attach, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in AMD's specifications for Known Good Die, and AMD assumes no responsibility for environmental effects on Known Good Die or for any activity of Buyer or a third party that damages the Die due to improper use, abuse, negligence, improper installation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than AMD ("Warranty Exclusions").

The liability of AMD under this warranty is limited, at AMD's option, solely to repair the Die, to send replacement Die, or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die returned to AMD, provided that: (a) AMD is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Known Good Die; (b) Buyer obtains authorization from AMD to return the defective Die; (c) the defective Die is returned to AMD by Buyer in accordance with AMD's shipping instructions set forth below; and (d) Buyer shows to AMD's satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die to AMD via AMD's carrier, collect. Risk of loss will transfer to AMD when the defective Die is provided to AMD's carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to AMD's specified location. The aforementioned provisions do not extend the original warranty period of any Known Good Die that has either been repaired or replaced by AMD.

WITHOUT LIMITING THE FOREGOING, EXCEPT TO THE EXTENT THAT AMD EXPRESSLY WARRANTS TO BUYER IN A SEPARATE AGREEMENT SIGNED BY AMD, AMD MAKES NO WARRANTY WITH RESPECT TO THE DIE'S PROCESSING OF DATE DATA, AND SHALL HAVE NO LIABILITY FOR DAMAGES OF ANY KIND, UNDER EQUITY, LAW, OR ANY OTHER THEORY, DUE TO THE FAILURE OF SUCH KNOWN GOOD DIE TO PROCESS ANY PARTICULAR DATA CONTAINING DATES, INCLUDING DATES IN AND AFTER THE YEAR 2000, WHETHER OR NOT AMD RECEIVED NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

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Buyer agrees that it will make no warranty representations to its customers which exceed those given by AMD to Buyer unless and until Buyer shall agree to indemnify AMD in writing for any claims which exceed AMD's warranty.

Known Good Die are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the Die can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

REVISION SUMMARY[查询"AM29BL802CB-60RDGE1"供应商](#)**Revision A (December 19, 2000)**

Initial release.

Revision A+1 (June 27, 2001)**Manufacturing Information**

Added Penang, Malaysia as a test facility (ACN2016).

Revision A+2 (September 13, 2002)

Changed title from Boot Sector to Burst Sector.

AC Characteristics

Added Read Options, Burst Mode Read, Erase/Program Operations, and Alternate CE# Controlled Erase/Program Operations Tables.

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