

MC10E160, MC100E160

5V ECL 12-Bit Parity Generator/Checker

The MC10E/100E160 is a 12-bit parity generator/checker. The Q output is HIGH when an odd number of inputs are HIGH. A HIGH on the Enable input (\overline{EN}) forces the Q output LOW.

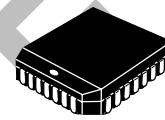
The 100 Series contains temperature compensation.

- Provides Odd-HIGH Parity of 12 Inputs
- Shiftable Output Register with Hold
- 900 ps Max. D to Q/\overline{Q} Output
- Enable
- Asynchronous Register Reset
- Dual Clocks
- PECL Mode Operating Range: $V_{CC} = 4.2\text{ V to }5.7\text{ V}$ with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
- Internal Input to 50 $K\Omega$ Pulldown Resistors
- ESD Protection: Human Body Model; > 1 KV, Machine Model; > 7 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 312 devices



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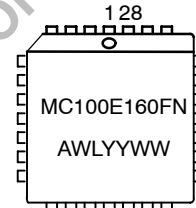
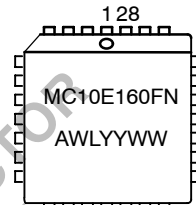
<http://onsemi.com>



PLCC-28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

MARKING DIAGRAMS



ORDERING INFORMATION

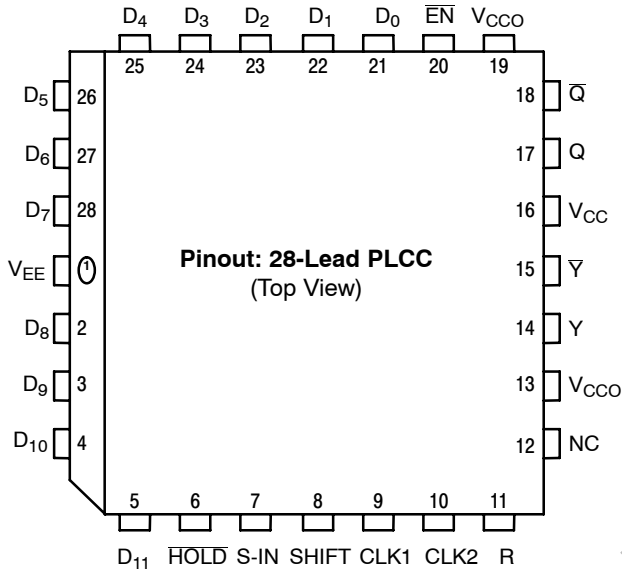
| Device | Package | Shipping [†] |
|---------------|---------|-----------------------|
| MC10E160FN | PLCC-28 | 37 Units/Rail |
| MC10E160FNR2 | PLCC-28 | 500 Units/Reel |
| MC100E160FN | PLCC-28 | 37 Units/Rail |
| MC100E160FNR2 | PLCC-28 | 500 Units/Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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LOGIC DIAGRAM AND PINOUT ASSIGNMENT



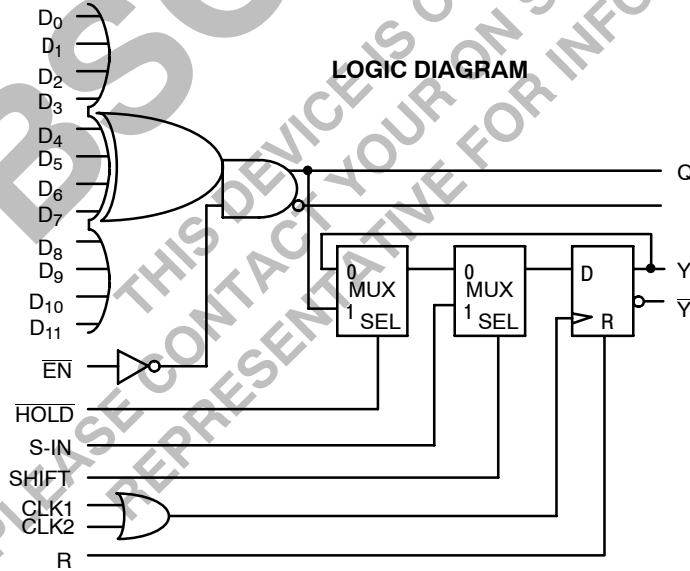
PIN DESCRIPTION

| PIN | FUNCTION |
|------------------------------------|------------------------|
| D ₀ - D ₁₁ | ECL Data Inputs |
| S-IN | ECL Serial Data Input |
| EN | ECL Enable, active LOW |
| HOLD | ECL Hold, active LOW |
| SHIFT | ECL Shift, active HIGH |
| CLK1, CLK2 | ECL Clock Inputs |
| R | ECL Reset Inputs |
| Q, Q̄ | ECL Direct Output |
| Y, Ȳ | ECL Register Output |
| V _{CC} , V _{CCO} | Positive Supply |
| V _{EE} | Negative Supply |
| NC | No Connect |

* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



MC10E160, MC100E160

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MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|--------------|--------------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | 0 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 LFPM 500 LFPM | 28 PLCC 28 PLCC | 63.5 43.5 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 28 PLCC | 22 to 26 | °C/W |
| T _{sol} | Wave Solder | <2 to 3 sec @ 248°C | | 265 | °C |

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 2)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-----------------|---|------|------|-------------------|------|------|-------------------|------|------|-------------------|----------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Power Supply Current | | 82 | 98 | | 82 | 98 | | 82 | 98 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 3980 | 4070 | 4160 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 3050 | 3210 | 3370 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| V _{IH} | Input HIGH Voltage | 3830 | 3995 | 4160 | 3870 | 4030 | 4190 | 3940 | 4110 | 4280 | mV |
| V _{IL} | Input LOW Voltage | 3050 | 3285 | 3520 | 3050 | 3285 | 3520 | 3050 | 3302 | 3555 | mV |
| I _{IH} | Input HIGH Current CLK1, CLK2 R All Other Inputs | | | 200 300 150 | | | 200 300 150 | | | 200 300 150 | μA μA μA |
| I _{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.3 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary -0.46 V / +0.06 V.
3. Outputs are terminated through a 50 ohm resistor to V_{CC} - 2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 8)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|-----------------|---|-------|-------|-------------------|-------|-------|-------------------|-------|-------|-------------------|----------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Power Supply Current | | 82 | 98 | | 82 | 98 | | 82 | 98 | mA |
| V _{OH} | Output HIGH Voltage (Note 5) | -1020 | -930 | -840 | -980 | -895 | -810 | -910 | -815 | -720 | mV |
| V _{OL} | Output LOW Voltage (Note 5) | -1950 | -1790 | -1630 | -1950 | -1790 | -1630 | -1950 | -1773 | -1595 | mV |
| V _{IH} | Input HIGH Voltage | -1170 | -1005 | -840 | -1130 | -970 | -810 | -1060 | -890 | -720 | mV |
| V _{IL} | Input LOW Voltage | -1950 | -1715 | -1480 | -1950 | -1715 | -1480 | -1950 | -1698 | -1445 | mV |
| I _{IH} | Input HIGH Current CLK1, CLK2 R All Other Inputs | | | 200 300 150 | | | 200 300 150 | | | 200 300 150 | μA μA μA |
| I _{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.065 | | 0.3 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary -0.46 V / +0.06 V.
5. Outputs are terminated through a 50 ohm resistor to V_{CC} - 2 volts.

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100E SERIES PECL DC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 6)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|----------|---|------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 82 | 98 | | 82 | 98 | | 94 | 113 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 7) | 3190 | 3295 | 3380 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| V_{IH} | Input HIGH Voltage | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| V_{IL} | Input LOW Voltage | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| I_{IH} | Input HIGH Current CLK1, CLK2 R All Other Inputs | | | 200 | | | 200 | | | 200 | μA |
| | | | | 300 | | | 300 | | | 300 | μA |
| | | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

7. Outputs are terminated through a 50 ohm resistor to $V_{CC} - 2$ volts.

100E SERIES NECL DC CHARACTERISTICS $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 8)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|----------|---|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 82 | 98 | | 82 | 98 | | 94 | 113 | mA |
| V_{OH} | Output HIGH Voltage (Note 9) | -1025 | -950 | -880 | -1025 | -950 | -880 | -1025 | -950 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 9) | -1810 | -1705 | -1620 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV |
| V_{IH} | Input HIGH Voltage | -1165 | -1025 | -880 | -1165 | -1025 | -880 | -1165 | -1025 | -880 | mV |
| V_{IL} | Input LOW Voltage | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV |
| I_{IH} | Input HIGH Current CLK1, CLK2 R All Other Inputs | | | 200 | | | 200 | | | 200 | μA |
| | | | | 300 | | | 300 | | | 300 | μA |
| | | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

8. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

9. Outputs are terminated through a 50 ohm resistor to $V_{CC} - 2$ volts.

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AC CHARACTERISTICS $V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 10)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|--------------|---|------|------|-----|------|------|-----|------|------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Toggle Frequency | 700 | 1100 | | 700 | 1100 | | 700 | 1100 | | MHz |
| t_{PLH} | Propagation Delay to Output D to Q \overline{EN} to Q CLK to Y R to Y | 400 | 650 | 950 | 400 | 650 | 950 | 400 | 650 | 950 | ps |
| t_{PHL} | | 300 | 550 | 750 | 300 | 550 | 750 | 300 | 550 | 750 | |
| | | 275 | 500 | 700 | 275 | 500 | 700 | 275 | 500 | 700 | |
| | | 275 | 500 | 725 | 275 | 500 | 725 | 275 | 500 | 725 | |
| t_s | Setup Time D \overline{HOLD} S-IN SHIFT | 1200 | 900 | | 1200 | 900 | | 1200 | 900 | | ps |
| | | 600 | 300 | | 600 | 300 | | 600 | 300 | | |
| | | 350 | 150 | | 350 | 150 | | 350 | 150 | | |
| | | 500 | 250 | | 500 | 250 | | 500 | 250 | | |
| t_h | Hold Time D \overline{HOLD} S-IN SHIFT | -400 | -900 | | -400 | -900 | | -400 | -900 | | ps |
| | | 100 | -300 | | 100 | -300 | | 100 | -300 | | |
| | | 300 | -150 | | 300 | -150 | | 300 | -150 | | |
| | | 200 | -250 | | 200 | -250 | | 200 | -250 | | |
| t_{JITTER} | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| t_r | Rise/Fall Time (20 - 80%) | | | | | | | | | | ps |
| t_f | | 300 | 450 | 650 | 300 | 450 | 650 | 300 | 450 | 650 | |

NOTE: Devices are designed to meet the AC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 LFPM is maintained.

10, 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.

100 Series: V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

MC10E160, MC100E160

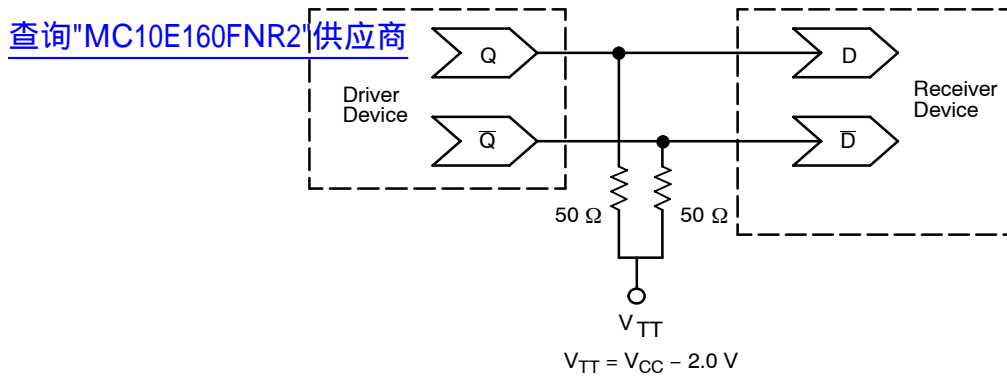


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

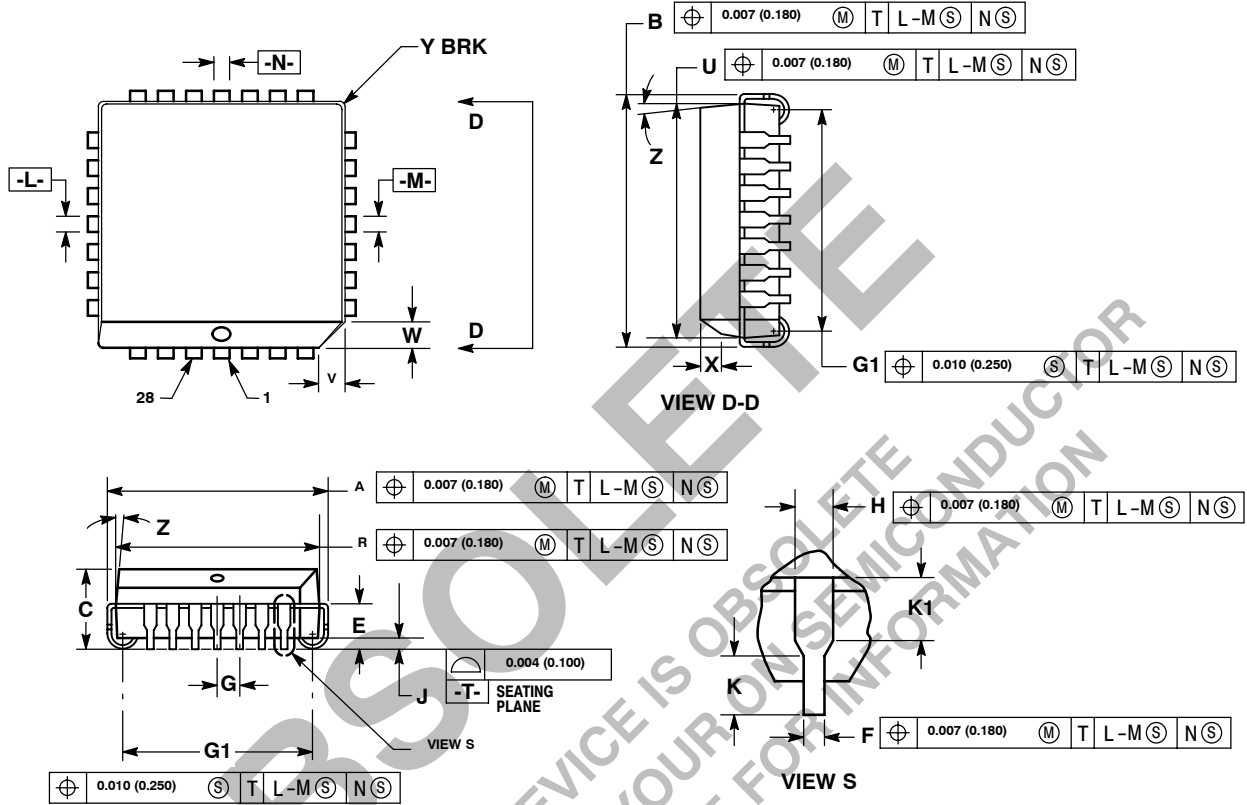
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC10E160, MC100E160

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:


- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

MC10E160, MC100E160

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