# VCXO JITTER ATTENUATOR & FEMTOCLOCK™ MULTIPLIER

ICS813322-02

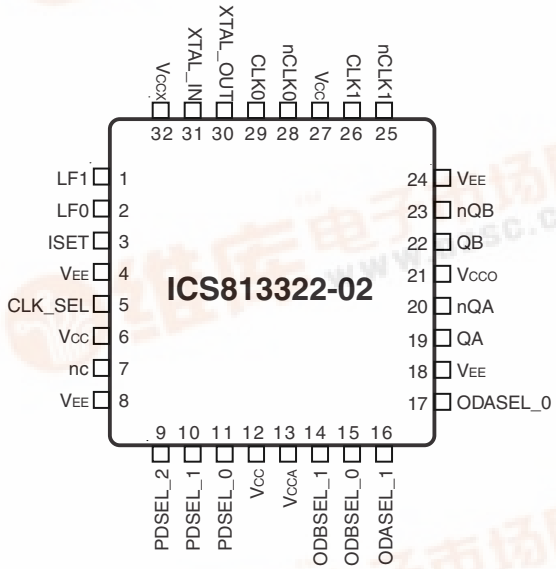
## General Description

The ICS813322-02 is a member of the HiperClockS™family of high performance clock solutions from IDT. The ICS813322-02 is a PLL based synchronous multiplier that is optimized for Ethernet or SONET-to-SONET clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock™ frequency multiplier that provides the low jitter, high frequency SONET output clock that meets up to SONET OC-48 jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in Ethernet and SONET applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-VFQFN package.

## Features

- Two differential LVPECL outputs
  Each output supports independent frequency selection at 19.44MHz, 77.76MHz, 155.52MHz and 622.08MHz
- Two differential inputs support the following input types: LVPECL, LVDS, HCSL
- Accepts input frequencies from 8kHz to 156.25MHz including 8kHz,19.44MHz, 25MHz, 62.5MHZ, 77.76MHz, 125MHz, 155.52MHz and 156.25MHz
- Each output has independently controlled dividers for common SONET clock rates
- Attenuates the phase jitter of the input clock by using a low-cost pullable funamental mode VCXO crystal
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock frequency multiplier provides low jitter, high frequency output
- Absolute pull range: 50ppm
- FemtoClock VCO frequency: 622.08MHz
- RMS phase jitter @ 155.52MHz, using a 19.44MHz crystal (12kHz – 20MHz): 1.16ps (typical)
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Pin Assignment




**32-Lead VFQFN**
5mm x 5mm x 0.925mm package body
**K Package**
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

## BLOCK DIAGRAM

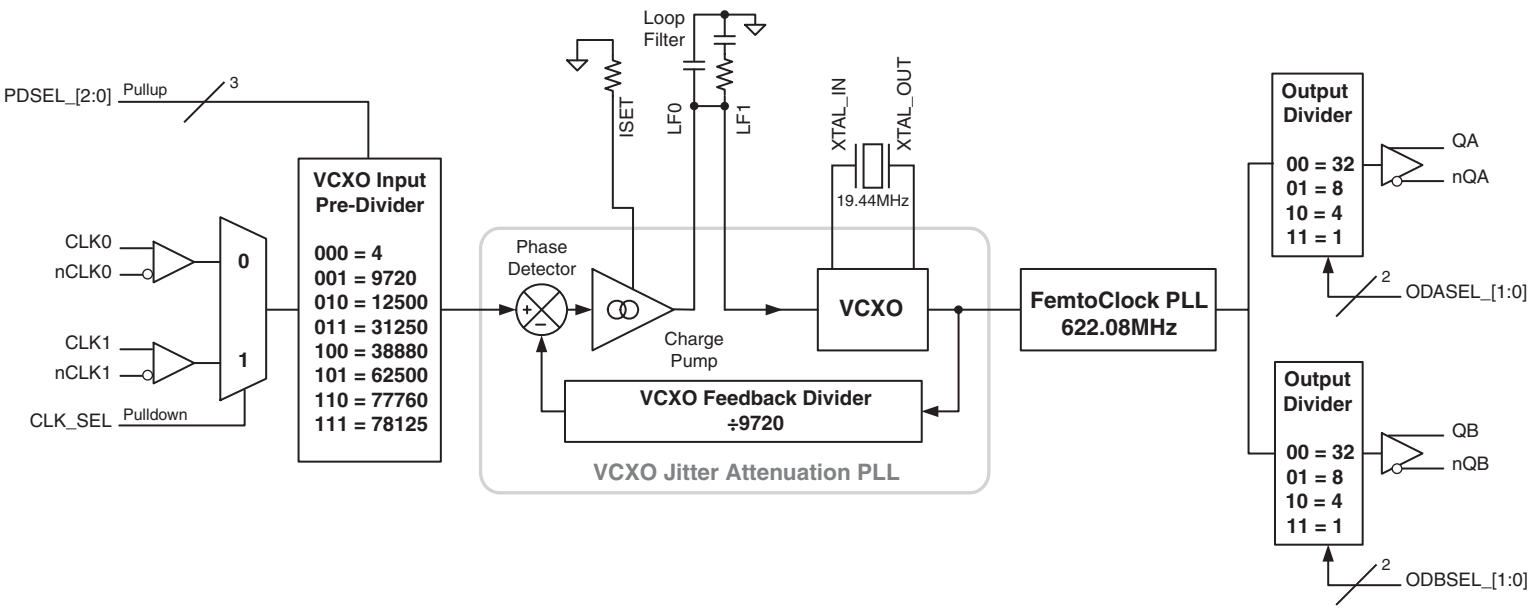


**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 2 | LF1, LF0 | Analog Input/Output | | Loop filter connection node pins. |
| 3 | ISET | Analog Input/Output | | Charge pump current setting pin. |
| 4, 8, 18, 24 | $V_{EE}$ | Power | | Negative supply pins. |
| 5 | CLK_SEL | Input | Pulldown | Input clock select. When HIGH selects CLK1/nCLK1. When LOW, selects CLK0/nCLK0. LVCMOS/LVTTL interface levels. |
| 6, 12, 27 | $V_{CC}$ | Power | | Core power supply pins. |
| 7, 20, 23 | nc | Unused | | No connect. |
| 9, 10, 11 | PDSEL_2, PDSEL_1, PDSEL_0 | Input | Pullup | Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A. |
| 13 | $V_{CCA}$ | Power | | Analog supply pin. |
| 14, 15 | ODBSEL_1, ODBSEL_0 | Input | Pulldown | Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels. |
| 16, 17 | ODASEL_1, ODASEL_0 | Input | Pulldown | Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels. |
| 19, 20 | QA, nQA | Output | | Bank A differential clock outputs. LVPECL interface levels. |
| 21 | $V_{CCO}$ | Power | | Output power supply pin. |
| 22, 23 | QB, nQB | Output | | Bank B differential clock outputs. LVPECL interface levels. |
| 25 | nCLK1 | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating. |
| 26 | CLK1 | Input | Pulldown | Non-inverting differential clock input. |
| 28 | nCLK0 | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{DD}/2$ bias voltage when left floating. |
| 29 | CLK0 | Input | Pulldown | Non-inverting differential clock input. |
| 30, 31 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 32 | $V_{CCX}$ | Power | | Power supply pin for VCXO charge pump. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

**TABLE 3A. PRE-DIVIDER FUNCTION TABLE**

| Inputs | | | Pre-Divider Value |
|---|---|---|---|
| PDSEL_2 | PDSEL_1 | PDSEL_0 | |
| 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 9720 |
| 0 | 1 | 0 | 12500 |
| 0 | 1 | 1 | 31250 |
| 1 | 0 | 0 | 38880 |
| 1 | 0 | 1 | 62500 |
| 1 | 1 | 0 | 77760 |
| 1 | 1 | 1 | 78125 (default) |

**TABLE 3B. OUTPUT DIVIDER FUNCTION TABLE**

| Inputs | | Output Divider Value |
|---|---|---|
| ODxSEL_1 | ODxSEL_0 | |
| 0 | 0 | 32 (default) |
| 0 | 1 | 8 |
| 1 | 0 | 4 |
| 1 | 1 | 1 |

**TABLE 3C. FREQUENCY FUNCTION TABLE**

| Input Frequency (MHz) | Pre-Divider Value | VCXO Frequency (MHz) | FemtoClock Feedback Divider Value | Femtoclock VCO Frequency (MHz) | Output Divider Value | Output Frequency (MHz) |
|---|---|---|---|---|---|---|
| 0.008 | 4 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 0.008 | 4 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 0.008 | 4 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 0.008 | 4 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 19.44 | 9720 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 19.44 | 9720 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 19.44 | 9720 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 19.44 | 9720 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 25 | 12500 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 25 | 12500 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 25 | 12500 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 25 | 12500 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 62.5 | 31250 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 62.5 | 31250 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 62.5 | 31250 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 62.5 | 31250 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 77.76 | 38880 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 77.76 | 38880 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 77.76 | 38880 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 77.76 | 38880 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 125 | 62500 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 125 | 62500 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 125 | 62500 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 125 | 62500 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 155.52 | 77760 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 155.52 | 77760 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 155.52 | 77760 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 155.52 | 77760 | 19.44 | 32 | 622.08 | 1 | 622.08 |
| 156.25 | 78125 | 19.44 | 32 | 622.08 | 32 | 19.44 |
| 156.25 | 78125 | 19.44 | 32 | 622.08 | 8 | 77.76 |
| 156.25 | 78125 | 19.44 | 32 | 622.08 | 4 | 155.52 |
| 156.25 | 78125 | 19.44 | 32 | 622.08 | 1 | 622.08 |

## Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 37°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = $V_{CCO}$ = $V_{CCX}$ = 3.3V±5%, $V_{EE}$ = 0V, TA = 0°C to 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | $V_{CC}$ – 0.15 | 3.3 | $V_{CC}$ | V |
| $V_{CCO}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCX}$ | Charge Pump Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{CCA}$ | Analog Supply Current | | | 15 | | mA |
| $I_{EE}$ | Output Supply Current | | | 250 | | mA |
| $I_{CCX}$ | Charge Pump Supply Current | | | 0.250 | | mA |

**Table 4B. LVCMOS / LVTTL DC Characteristics,** $V_{CC}$ = $V_{CCO}$ = $V_{CCX}$ = 3.3V±5%, $V_{EE}$ = 0V, TA = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1] | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | PDSEL[0:2] | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1] | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | PDSEL[0:2] | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$/2.

**Table 4C. Differential DC Characteristics,** $V_{CC}$ = $V_{CCO}$ = $V_{CCX}$ = 3.3V±5%, $V_{EE}$ = 0V, TA = 0°C to 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High Current | CLK0/nCLK0, CLK1/nCLK1 | $V_{IN}$ = $V_{CC}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK0, CLK1 | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -5 | | | µA |
| | | nCLK0, nCLK1 | $V_{IN}$ = 0V, $V_{CC}$ = 3.465V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | $V_{EE}$ + 0.5 | | $V_{CC}$ – 0.85 | V |

NOTE 1: Common mode voltage is defined as $V_{IH}$.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is $V_{CC}$ + 0.3V.

**TABLE 4D. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO}$ - 1.4 | | $V_{CCO}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO}$ - 2.0 | | $V_{CCO}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

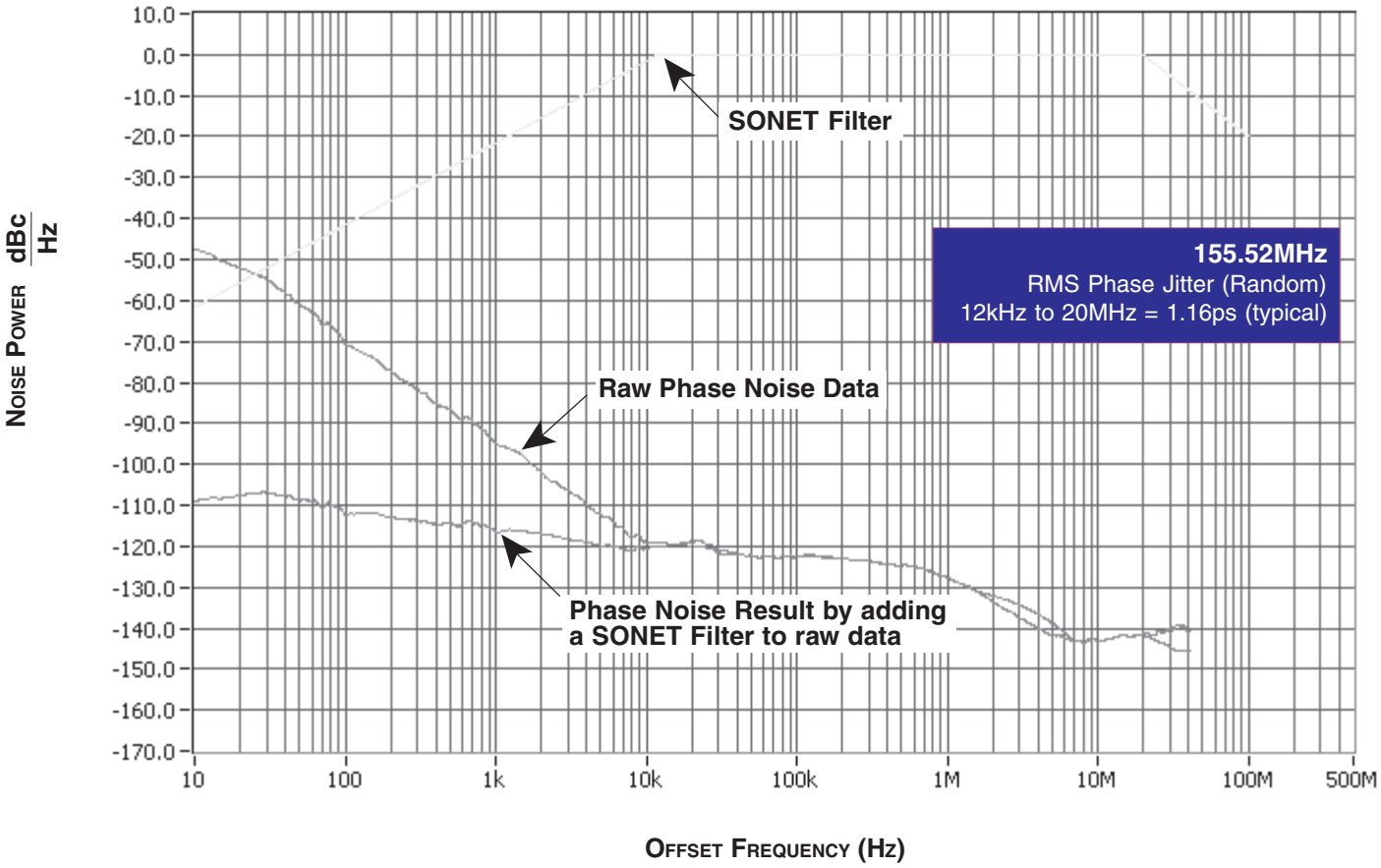
NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$ - 2V.

**TABLE 5. AC CHARACTERISTICS,** $V_{CC} = V_{CCO} = V_{CCX} = 3.3V±5\%$, $V_{EE} = 0V$, $T_A = 0°C$ TO $70°C$

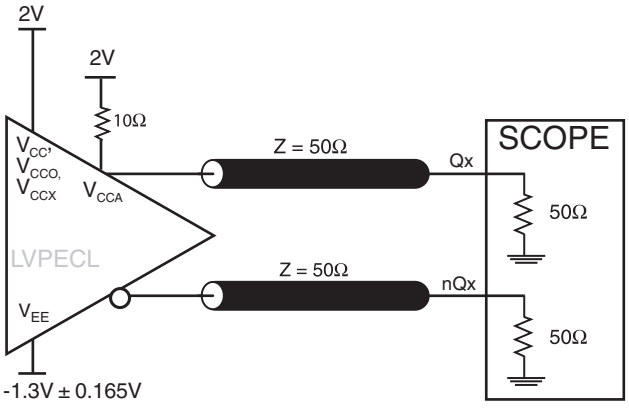
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | | 0.008 | | 156.25 | MHz |
| $f_{OUT}$ | Output Frequency | | 19.44 | | 622.08 | MHz |
| *t*jit(Ø) | RMS Phase Jitter (Random); NOTE 1 | 155.52MHz $f_{OUT}$, 19.44MHz crystal, Integration Range: 12kHz - 20MHz | | 1.16 | | ps |
| *t*jit(cc) | Cycle-to-Cycle Jitter; NOTE 2, 3 | | | 50 | | ps |
| *t*jit(per) | Period Jitter; NOTE 4 | | | 5 | | ps |
| *t*sk(o) | Output Skew; NOTE 3, 5 | | | 50 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | | 600 | | ps |
| $t_{LOCK}$ | PLL Lock Time | | | 100 | | ms |

NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Outputs terminated with 50Ω to $V_{CCO}$ - 2V.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Jitter performance using crystal inputs.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load condtions. Measured at the output differential cross points.

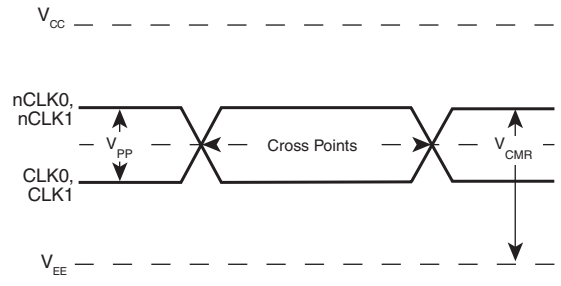
## TYPICAL PHASE NOISE AT 155.52MHZ



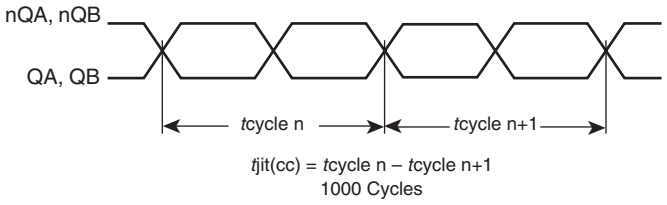
# PARAMETER MEASUREMENT INFORMATION



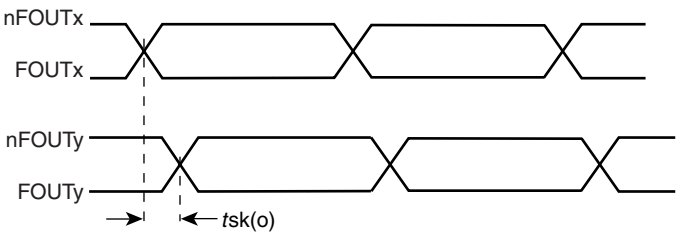

### 3.3V OUTPUT LOAD AC TEST CIRCUIT



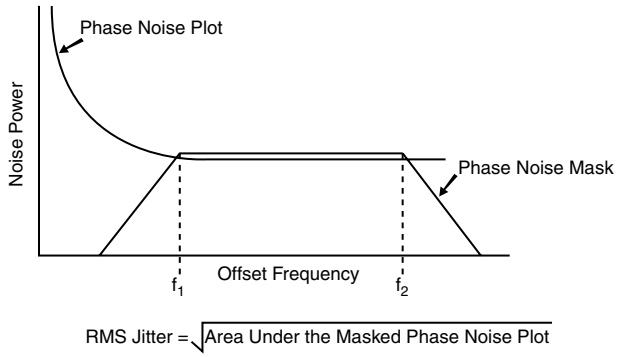

### DIFFERENTIAL INPUT LEVEL



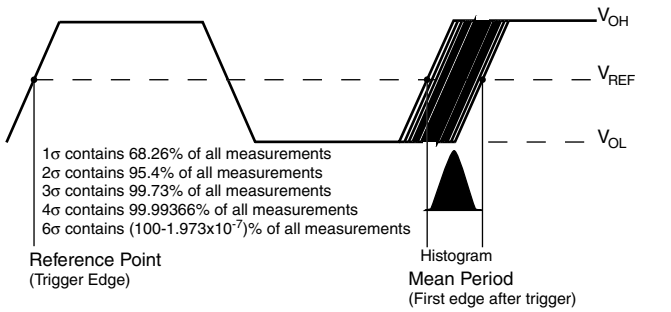

### CYCLE-TO-CYCLE JITTER



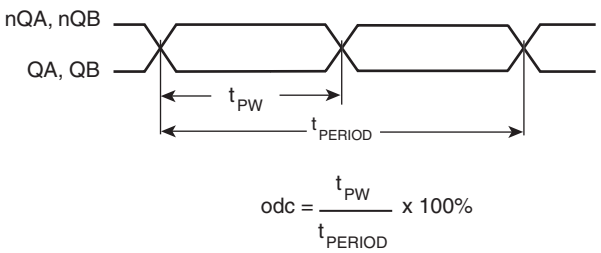

### OUTPUT SKEW



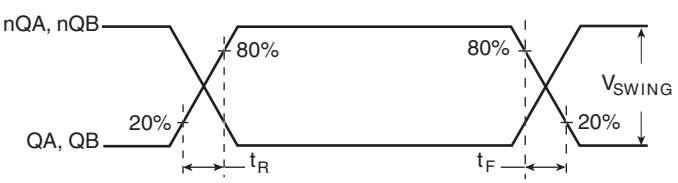

### PHASE JITTER




### PERIOD JITTER




### OUTPUT DUTY CYCLE/PULSE WIDTH/tPERIOD




### OUTPUT RISE/FALL TIME

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS813322-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCX}$, $V_{CCA}$, and $V_{CCO}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{CC}$ pin and also shows that $V_{CCA}$ requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{CCA}$ pin.

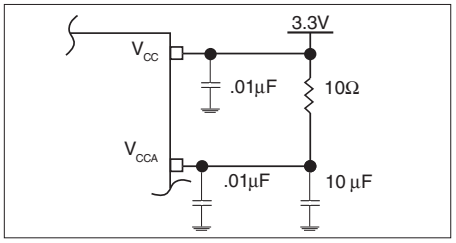



FIGURE 1. POWER SUPPLY FILTERING

## WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ $V_{CC}$/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC}$= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

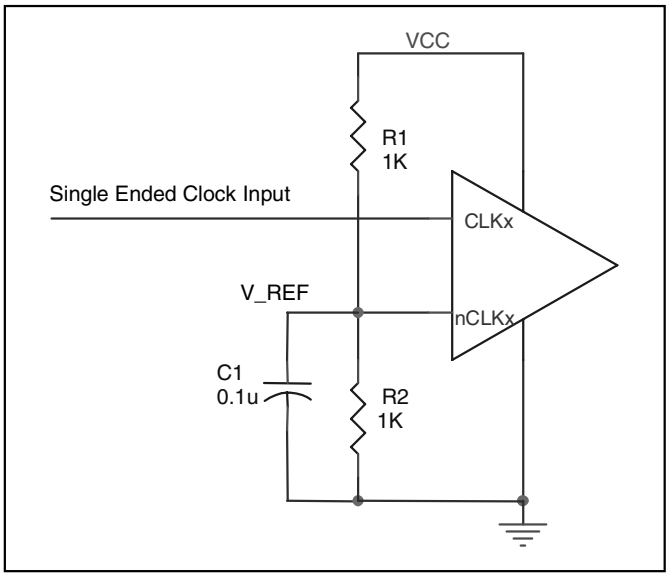



FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

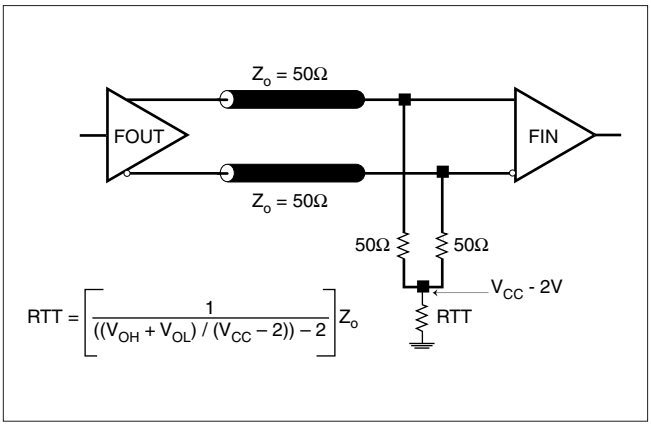



Figure 3A. LVPECL Output Termination

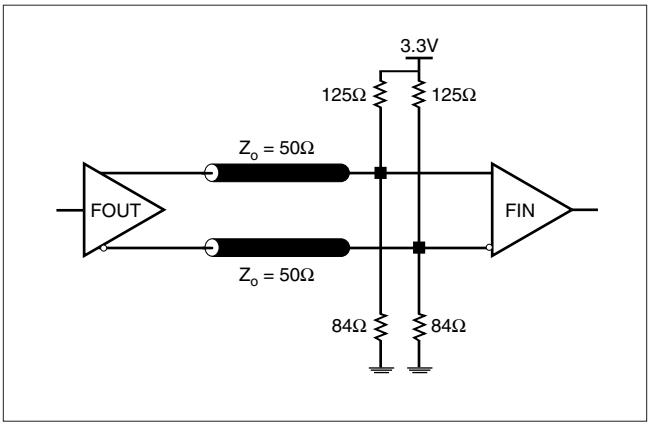



Figure 3B. LVPECL Output Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

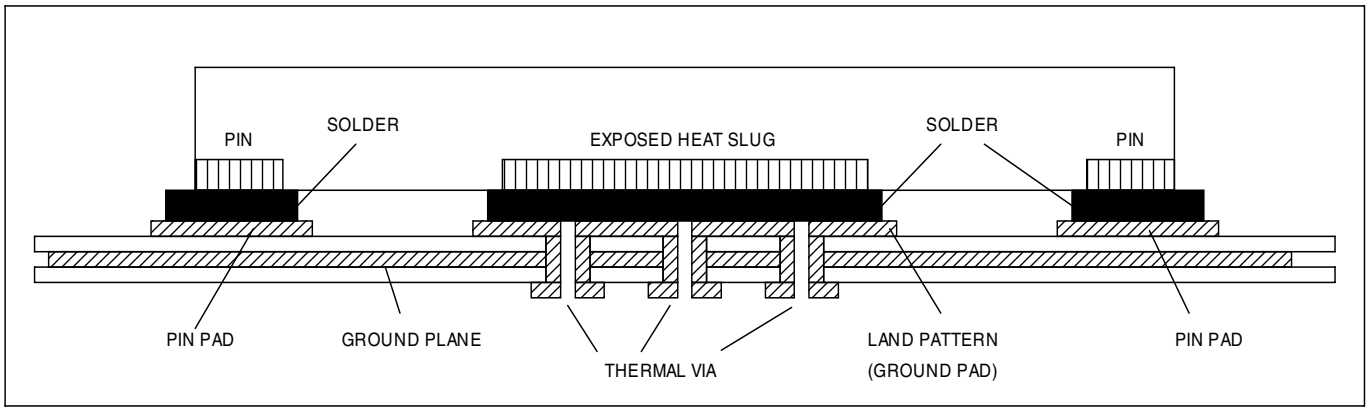



**Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)**

## SCHEMATIC EXAMPLE

*Figure 5* shows an example of the ICS813322-02 application schematic. In this example, the device is operated at $V_{CC}$ = $V_{CCX}$ = $V_{CCO}$ = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

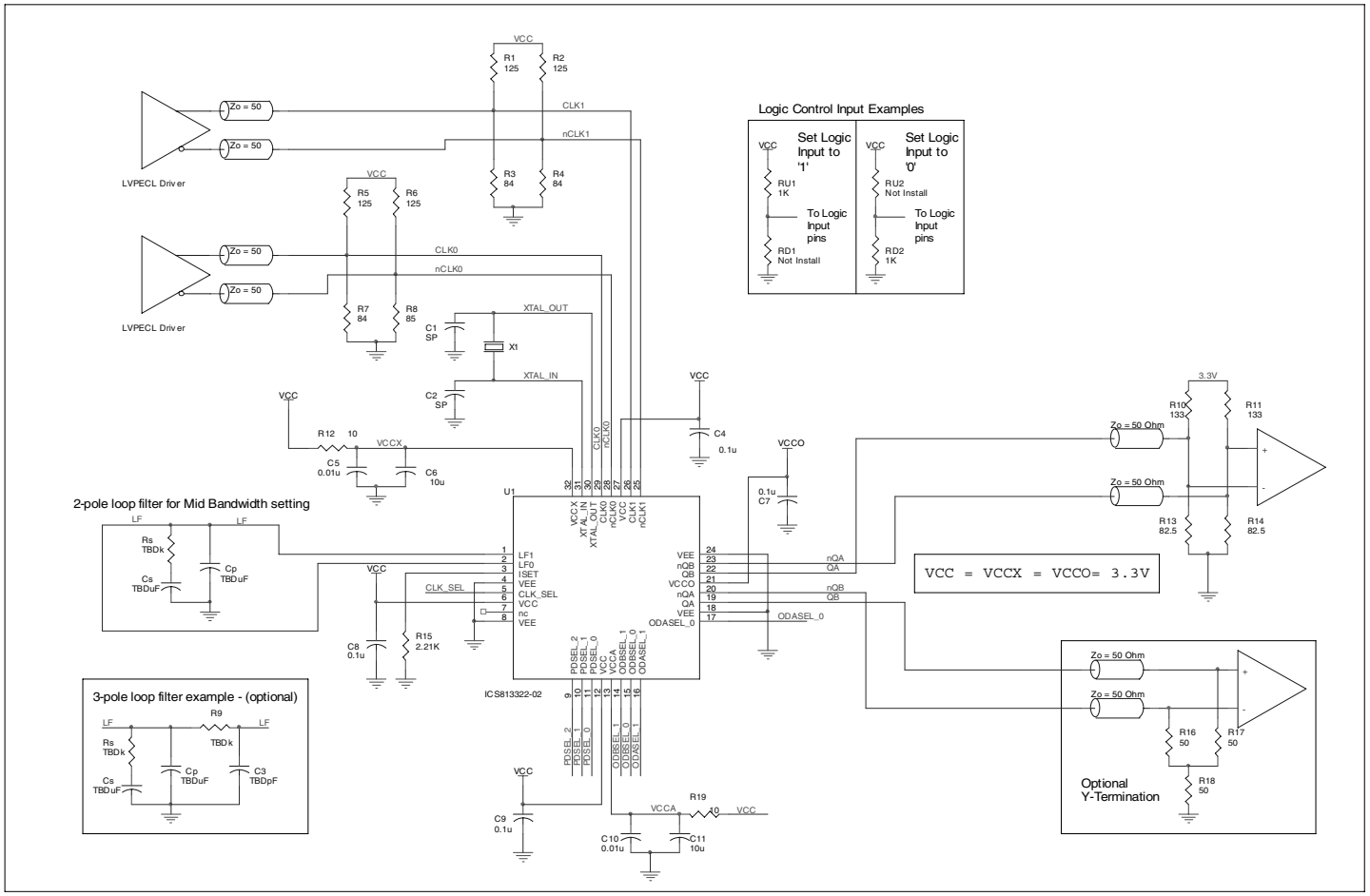



**FIGURE 5. ICS813322-02 SCHEMATIC LAYOUT**

## VCXO-PLL External Components

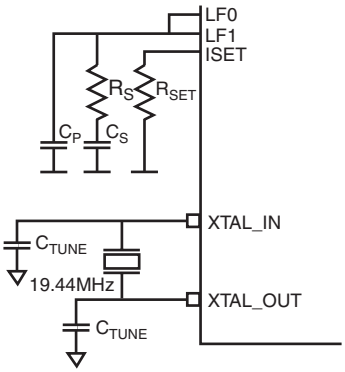
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance ($C_L$). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

*The crystal's load capacitance $C_L$* characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors ($C_{TUNE}$).

If the crystal $C_L$ is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal $C_L$ is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of $C_L$ is dependant on the characteristics of the VCXO. The recommended $C_L$ in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows $R_S$, $C_S$ and $C_P$ values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.




### VCXO Characteristics Table

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $k_{VCXO}$ | VCXO Gain | 6000 | Hz/V |
| $C_{V\_LOW}$ | Low Varactor Capacitance | 15.9 | pF |
| $C_{V\_HIGH}$ | High Varactor Capacitance | 29.8 | pF |

### VCXO-PLL Loop Bandwidth Selection Table

| Bandwidth | Crystal Frequency (MHz) | $R_S$ (kΩ) | $C_S$ (µF) | $C_P$ (µF) | $R_{SET}$ (kΩ) |
|---|---|---|---|---|---|
| 10Hz (Low) | 19.44MHz | 800 | 1.8 | 0.0034 | 8.5 |
| 80Hz (Mid) | 19.44MHz | 540 | 0.15 | 0.0015 | 2.3 |
| 240Hz (High) | 19.44MHz | 1000 | 0.25 | 0.0008 | 2.1 |

### Crystal Characteristics

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| | Mode of Operation | | Fundamental | | |
| $f_N$ | Frequency | | 19.44 | | MHz |
| $f_T$ | Frequency Tolerance | | | ±20 | ppm |
| $f_S$ | Frequency Stability | | | ±20 | ppm |
| | Operating Temperature Range | 0 | | 70 | °C |
| $C_L$ | Load Capacitance | | 10 | | pF |
| $C_O$ | Shunt Capacitance | | 4 | | pF |
| $C_O/C_1$ | Pullability Ratio | | 220 | 240 | |
| ESR | Equivalent Series Resistance | | | 20 | |
| | Drive Level | | | 1 | mW |
| | Aging @ 25°C | | | ±3 per year | ppm |

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS813322-02. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS813322-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 250mA = **866.25mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

**Total Power$_{_MAX}$** (3.465V, with all outputs switching) = 866.25mW + 60mW = **926.25mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.926W * 37°C/W = 104.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE $\theta_{JA}$ FOR 32-LEAD VFQFN, FORCED CONVECTION**

| $\theta_{JA}$ vs. 0 Air Flow (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.0°C/W | 32.4°C/W | 29.0°C/W |

*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

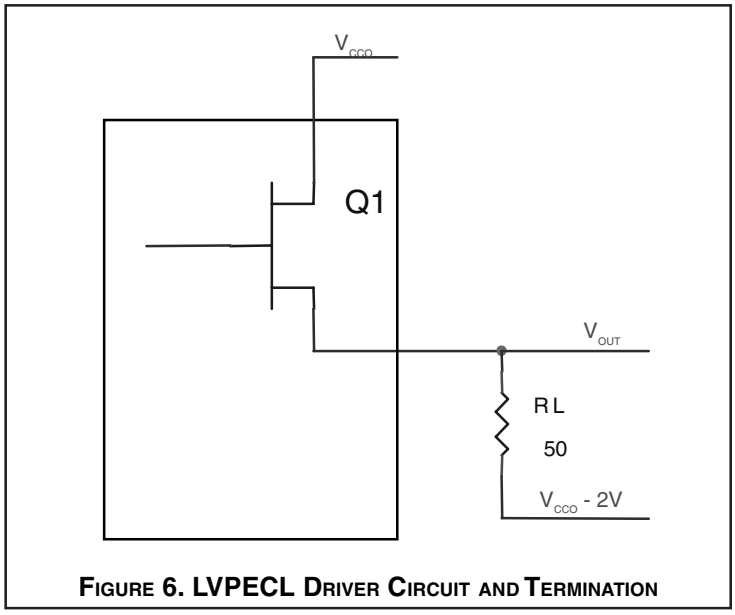



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.9V)/50Ω] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

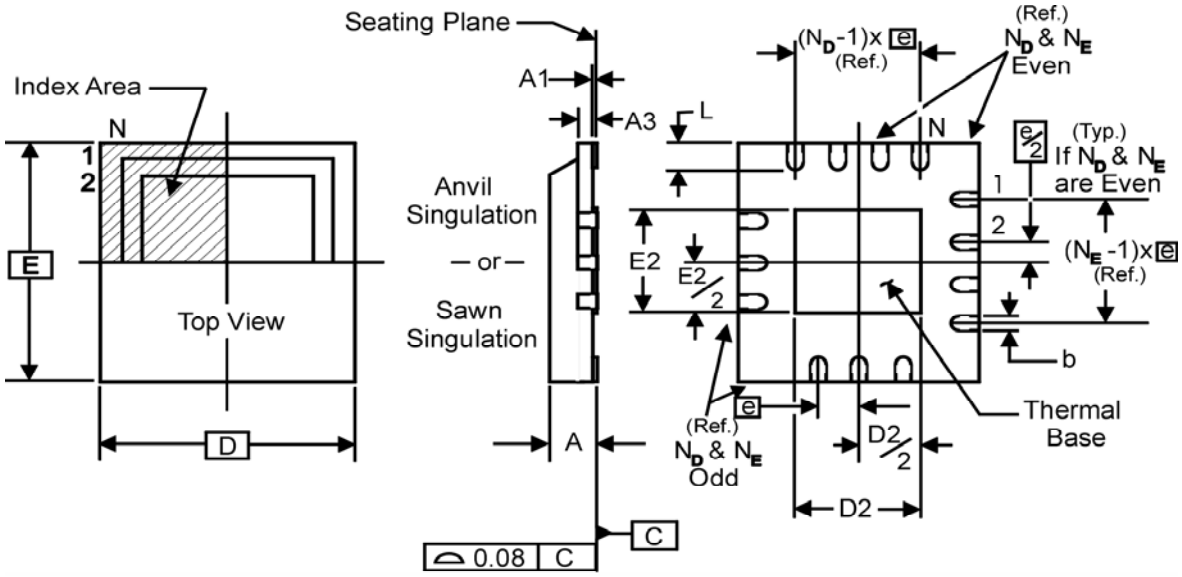
**TABLE 7. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 32 LEAD VFQFN**

| $\theta_{JA}$ vs. 0 Air Flow (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 37.0°C/W | 32.4°C/W | 29.0°C/W |

## TRANSISTOR COUNT

The transistor count for ICS813322-02 is: 6331

## Package Outline and Dimensions - K Suffix for 32 Lead VFQFN




NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

### Table 8. Package Dimensions

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4) | | |
|---|---|---|
| **SYMBOL** | **Minimum** | **Maximum** |
| **N** | 32 | |
| **A** | 0.80 | 1.0 |
| **A1** | 0 | 0.05 |
| **A3** | 0.25 Reference | |
| **b** | 0.18 | 0.30 |
| **e** | 0.50 BASIC | |
| **$N_D$** | 8 | |
| **$N_E$** | 8 | |
| **D, E** | 5.0 | |
| **D2, E2** | 3.0 | 3.3 |
| **L** | 0.30 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 813322BK-02 | ICS13322B02 | 32 Lead VFQFN | tray | 0°C to 70°C |
| 813322BK-02T | ICS13322B02 | 32 Lead VFQFN | 2500 tape & reel | 0°C to 70°C |
| 813322BK-02LF | ICS3322B02L | 32 Lead "Lead-Free" VFQFN | tray | 0°C to 70°C |
| 813322BK-02LFT | ICS3322B02L | 32 Lead "Lead-Free" VFQFN | 2500 tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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