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National Semiconductor

June 2004



# LP2997
# DDR-II Termination Regulator

## General Description

The LP2997 linear regulator is designed to meet the JEDEC SSTL-18 specifications for termination of DDR-II memory. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 500mA continuous current and transient peaks up to 900mA in the application as required for DDR-II SDRAM termination. The LP2997 also incorporates a $V_{SENSE}$ pin to provide superior load regulation and a $V_{REF}$ output as a reference for the chipset and DIMMs.

An additional feature found on the LP2997 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the $V_{TT}$ output will tri-state providing a high impedance output, but, $V_{REF}$ will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

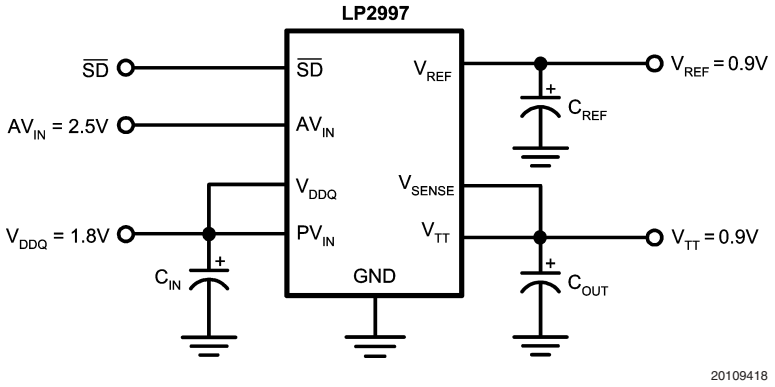
## Features

- Source and sink current
- Low output voltage offset
- No external resistors required
- Linear topology
- Suspend to Ram (STR) functionality
- Low external component count
- Thermal Shutdown
- Available in SO-8, PSOP-8 packages

## Applications

- DDR-II Termination Voltage
- SSTL-18 Termination

## Typical Application Circuit

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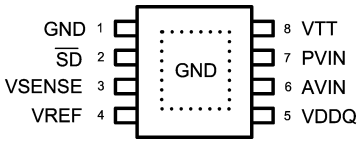
## Connection Diagrams

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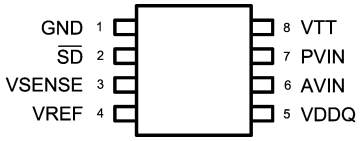
**PSOP-8 Layout**

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**SO-8 Layout**

## Pin Description

| SO-8 Pin or PSOP-8 Pin | Name | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | $\overline{SD}$ | Shutdown |
| 3 | VSENSE | Feedback pin for regulating $V_{TT}$. |
| 4 | VREF | Buffered internal reference voltage of $V_{DDQ}/2$ |
| 5 | VDDQ | Input for internal reference equal to $V_{DDQ}/2$ |
| 6 | AVIN | Analog input pin |
| 7 | PVIN | Power input pin |
| 8 | VTT | Output voltage for connection to termination resistors |

## Ordering Information

| Order Number | Package Type | NSC Package Drawing | Supplied As |
|---|---|---|---|
| LP2997M | SO-8 | M08A | 95 Units per Rail |
| LP2997MX | SO-8 | M08A | 2500 Units Tape and Reel |
| LP2997MR | PSOP-8 | MRA08A | 95 Units Tape and Reel |
| LP2997MRX | PSOP-8 | MRA08A | 2500 Units Tape and Reel |

## Absolute Maximum Ratings (Note 1)

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**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| PVIN, AVIN, VDDQ to GND | |
| No pin should exceed AVIN | −0.3V to +6V |
| Storage Temp. Range | −65˚C to +150˚C |
| Junction Temperature | 150˚C |
| Lead Temperature (Soldering, 10 sec) | 260˚C |
| SO-8 Thermal Resistance ($\theta_{JA}$) | 151˚C/W |
| PSOP-8 Thermal Resistance ($\theta_{JA}$) | 43˚C/W |
| Minimum ESD Rating (Note 2) | 1kV |

## Operating Range

| | |
|---|---|
| Junction Temp. Range (Note 3) | 0˚C to +125˚C |
| AVIN to GND | 2.2V to 5.5V |

## Electrical Characteristics

Specifications with standard typeface are for $T_J$ = 25˚C and limits in **boldface type** apply over the full **Operating Temperature Range** ($T_J$ = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = 2.5V, PVIN = 1.8V, VDDQ = 1.8V.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{REF}$ | $V_{REF}$ Voltage | PVIN = VDDQ = 1.7V | **0.837** | 0.860 | **0.887** | V |
| | | PVIN = VDDQ = 1.8V | **0.887** | 0.910 | **0.937** | |
| | | PVIN = VDDQ = 1.9V | **0.936** | 0.959 | **0.986** | |
| $Z_{VREF}$ | $V_{REF}$ Output Impedance | $I_{REF}$ = -30 to +30 µA | | 2.5 | | kΩ |
| $V_{TT}$ | $V_{TT}$ Output Voltage | $I_{OUT}$ = 0A | | | | V |
| | | PVIN = VDDQ = 1.7V | **0.822** | 0.856 | **0.887** | |
| | | PVIN = VDDQ = 1.8V | **0.874** | 0.908 | **0.939** | |
| | | PVIN = VDDQ = 1.9V | **0.923** | 0.957 | **0.988** | |
| | | $I_{OUT}$ = ±0.5A (Note 7) | | | | |
| | | PVIN = VDDQ = 1.7V | **0.828** | 0.856 | **0.890** | |
| | | PVIN = VDDQ = 1.8V | **0.878** | 0.908 | **0.940** | |
| | | PVIN = VDDQ = 1.9V | **0.928** | 0.957 | **0.990** | |
| $Vos_{TT}/V_{TT}$ | $V_{TT}$ Output Voltage Offset ($V_{REF}$-$V_{TT}$) | $I_{OUT}$ = 0A | **-25** | 0 | **25** | mV |
| | | $I_{OUT}$ = -0.5A | **-25** | 0 | **25** | |
| | | $I_{OUT}$ = +0.5A | **-25** | 0 | **25** | |
| $I_Q$ | Quiescent Current (Note 5) | $I_{OUT}$ = 0A (Note 5) | | 320 | **500** | µA |
| $Z_{VDDQ}$ | VDDQ Input Impedance | | | 100 | | kΩ |
| $I_{SD}$ | Quiescent Current in Shutdown (Note 5) | SD = 0V | | 115 | **150** | µA |
| $I_{Q_SD}$ | Shutdown Leakage Current | SD = 0V | | 2 | **5** | µA |
| $V_{IH}$ | Minimum Shutdown High Level | | **1.9** | | | V |
| $V_{IL}$ | Minimum Shutdown Low Level | | | | **0.8** | V |
| $I_{SENSE}$ | $V_{SENSE}$ Input Current | | | 13 | | nA |
| $T_{SD}$ | Thermal Shutdown | (Note 6) | | 165 | | Celsius |
| $T_{SD}$_HYS | Thermal Shutdown Hysteresis | | | 10 | | Celsius |

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**Electrical Characteristics** Specifications with standard typeface are for $T_J$ = 25˚C and limits in **boldface type** apply over the **Operating Temperature Range** ($T_J$ = 0˚C to +125˚C) (Note 4). Unless otherwise specified, AVIN = 2.5V, PVIN = 1.8V, VDDQ = 1.8V. (Continued)

**Note 1:** Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions see Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

**Note 3:** At elevated temperatures, devices must be derated based on thermal resistance. The device in the SO-8 package must be derated at $\theta_{JA}$ = 151.2˚ C/W junction to ambient with no heat sink.

**Note 4:** Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

**Note 5:** Quiescent current defined as the current flow into AVIN.

**Note 6:** The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

**Note 7:** $V_{TT}$ load regulation is tested by using a 10 ms current pulse and measuring $V_{TT}$.

## Typical Performance Characteristics

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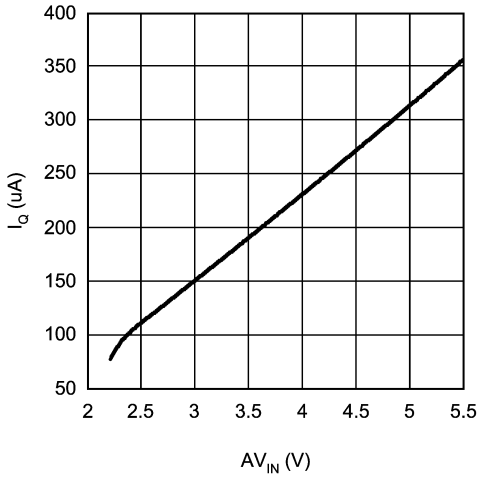
**Iq vs $AV_{IN}$ in SD**

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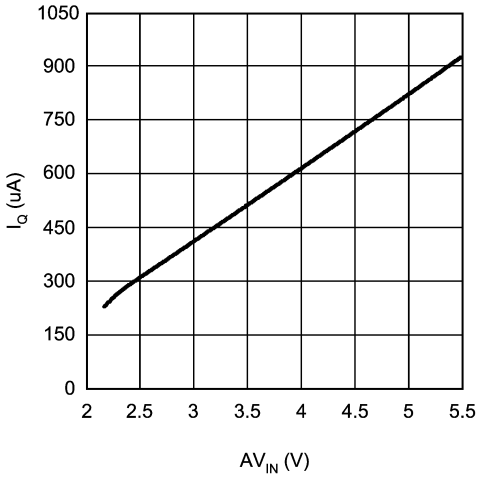
**Iq vs $AV_{IN}$**

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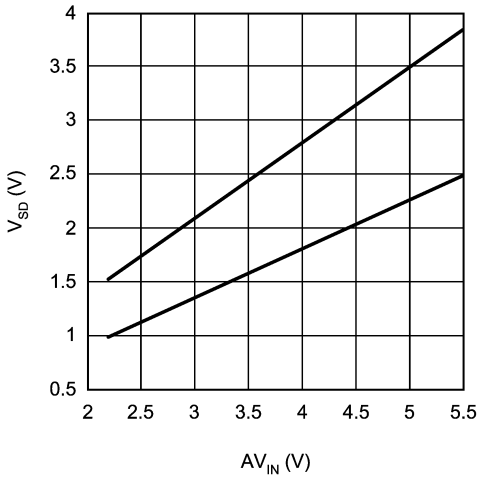
**$V_{IH}$ and $V_{IL}$**

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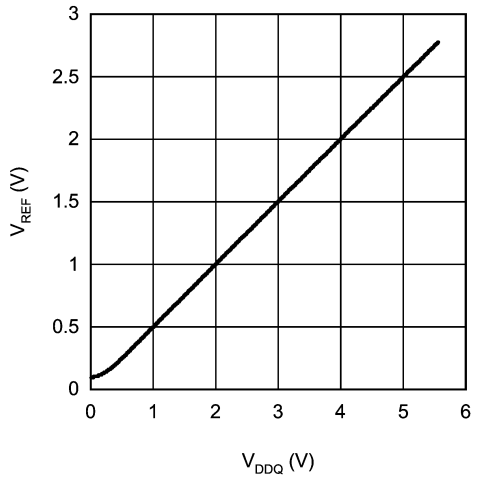
**$V_{REF}$ vs $V_{DDQ}$**

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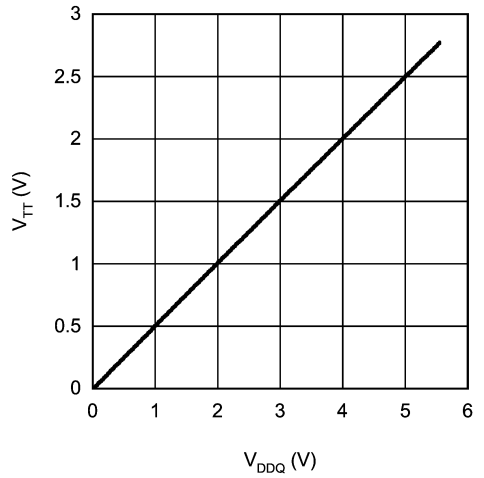
**$V_{TT}$ vs $V_{DDQ}$**

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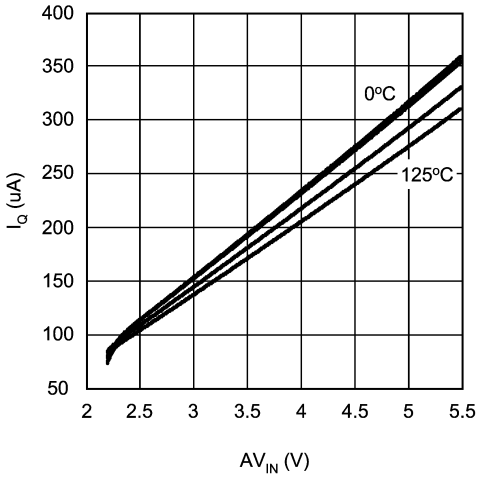
**Iq vs $AV_{IN}$ in SD Temperature**

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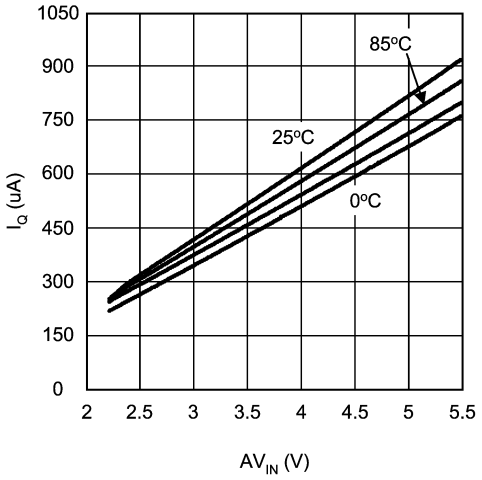
## Typical Performance Characteristics (Continued)

**Iq vs $AV_{IN}$ Temperature**

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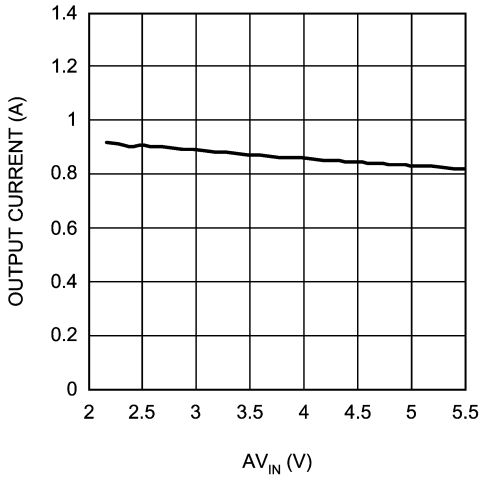
**Maximum Sourcing Current vs $AV_{IN}$ ($V_{DDQ}$ = 1.8V, $PV_{IN}$ = 1.8V)**

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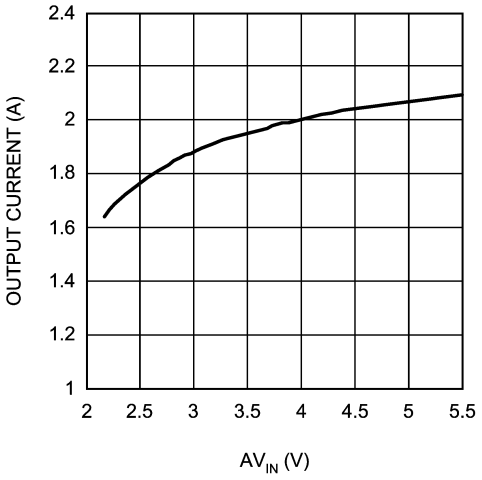
**Maximum Sinking Current vs $AV_{IN}$ ($V_{DDQ}$ = 1.8V)**

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## Block Diagram

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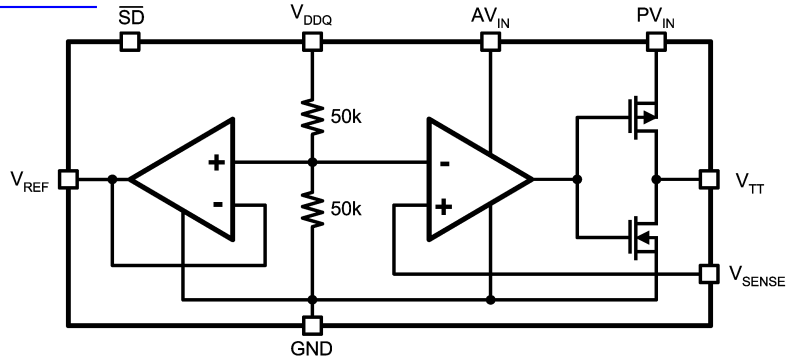


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## Description

The LP2997 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-18. The output, $V_{TT}$ is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2997 also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2997 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII).

## Pin Descriptions

### AVIN AND PVIN

AVIN and PVIN are the input supply pins for the LP2997. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create $V_{TT}$. These pins have the capability to work off separate supplies, under the condition that AVIN is always greater than or equal to PVIN. For SSTL-18 applications, it is recommended to connect PVIN to the 1.8V rail used for the memory core and AVIN to a rail within its operating range of 2.2V to 5.5V (typically a 2.5V supply). PVIN should always be used with either a 1.8V or 2.5V rail. This prevents the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where $V_{TT}$ is tri-stated and $V_{REF}$ remains active. A lower rail such as 1.5V can be used but it will reduce the maximum output current, therefore it is not recommended for most termination schemes.

### VDDQ

VDDQ is the input used to create the internal reference voltage for regulating $V_{TT}$. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that $V_{TT}$ will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 1.8V rail at the DIMM instead of PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-18 applications VDDQ will be a 1.8V signal, which will create a 0.9V termination voltage at $V_{TT}$ (See Electrical Characteristics Table for exact values of $V_{TT}$ over temperature).

### $V_{SENSE}$

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to $V_{TT}$ in a long plane. If the output voltage was regulated only at the output of the LP2997 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The $V_{SENSE}$ pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the $V_{SENSE}$ pin must still be connected to $V_{TT}$. Care should be taken when a long $V_{SENSE}$ trace is implemented in close proximity to the memory. Noise pickup in the $V_{SENSE}$ trace can cause problems with precise regulation of $V_{TT}$. A small 0.1uF ceramic capacitor placed next to the $V_{SENSE}$ pin can help filter any high frequency signals and preventing errors.

### SHUTDOWN

The LP2997 contains an active low shutdown pin that can be used for suspend to RAM functionality. In this condition the $V_{TT}$ output will tri-state while the $V_{REF}$ output remains active providing a constant reference signal for the memory and chipset. During shutdown $V_{TT}$ should not be exposed to voltages that exceed PVIN. With the shutdown pin asserted low the quiescent current of the LP2997 will drop, however, VDDQ will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section. The shutdown pin also has an internal pull-up current; therefore, to turn the part on the shutdown pin can either be connected to AVIN or left open

### $V_{REF}$

$V_{REF}$ provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from $V_{REF}$. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended.

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## Pin Descriptions (Continued)

This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

**$V_{TT}$**

$V_{TT}$ is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2997 is designed to handle continuous currents of up to +/- 0.5A with excellent load regulation. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop. If the LP2997 is to operate in elevated temperatures for long durations care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used. (Please refer to the Thermal Dissipation section) If the junction temperature exceeds the thermal shutdown point than $V_{TT}$ will tri-state until the part returns below the temperature hysteresis trip-point

## Component Selection

### INPUT CAPACITOR

The LP2997 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 22 µF. Ceramic capacitors can also be used. A value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2997 is placed close to the bulk capacitance from the output of the 1.8V DC-DC converter. For the AVIN pin, a small 0.1uF ceramic capacitor is sufficient to prevent excessive noise from coupling into the device.

### OUTPUT CAPACITOR

The LP2997 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of $V_{TT}$. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (100 kHz) should be used for the LP2997. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitors.

## Thermal Dissipation

Since the LP2997 is a linear regulator any current flow from $V_{TT}$ will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise ($T_{Rmax}$) can be calculated given the maximum ambient temperature ($T_{Amax}$) of the application and the maximum allowable junction temperature ($T_{Jmax}$).

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum power dissipation ($P_{Dmax}$) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The $\theta_{JA}$ of the LP2997 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the $\theta_{JA}$ of the SO-8 is 163˚C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2˚C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. *Figure 1* shows how the $\theta_{JA}$ varies with airflow for the two boards mentioned.

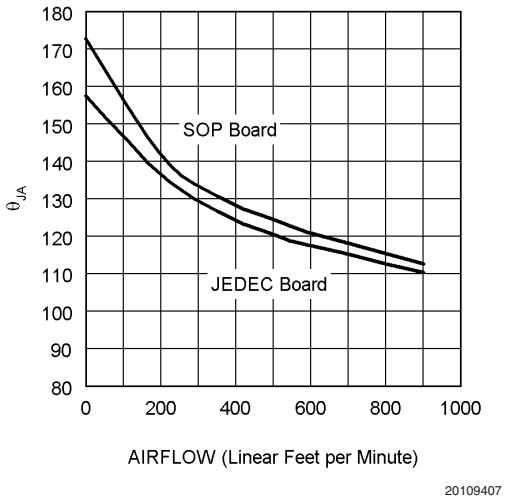


**FIGURE 1. $\theta_{JA}$ vs Airflow (SO-8)**

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the

## Thermal Dissipation (Continued)

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top side of the board can also help. With careful layout it is possible to reduce the $\theta_{JA}$ further than the nominal values shown in *Figure 1*

Optimizing the $\theta_{JA}$ and placing the LP2997 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at $V_{TT}$, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

Where,

$$P_{AVIN} = I_{AVIN} * V_{AVIN}$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ^2} \times R_{VDDQ}$$

To calculate the maximum power dissipation at $V_{TT}$ both conditions at $V_{TT}$ need to be examined, sinking and sourcing current. Although only one equation will add into the total, $V_{TT}$ cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \times I_{LOAD} \text{ (Sinking) or}$$

$$P_{VTT} = ( V_{PVIN} - V_{VTT}) \times I_{LOAD} \text{ (Sourcing)}$$

The power dissipation of the LP2997 can also be calculated during the shutdown state. During this condition the output $V_{TT}$ will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ}$$

$$P_{AVIN} = I_{AVIN} \times V_{AVIN}$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ^2} \times R_{VDDQ}$$

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## Typical Application Circuits

Several different application circuits have been shown to illustrate some of the options that are possible in configuring the LP2997. Graphs of the individual circuit performance can be found in the *Typical Performance Characteristics* section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

*Figure 2* shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 2.5V, 3.3V or 5V rail.

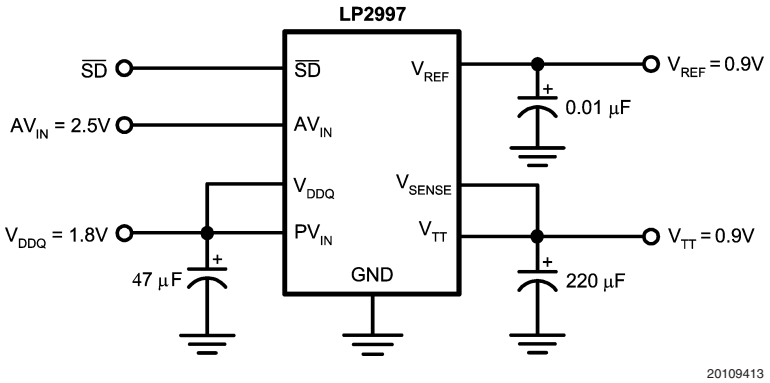


**FIGURE 2. Recommended DDR-II Termination**

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where $V_{TT}$ is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. The bulk output capacitors should be situated at both ends of the $V_{TT}$ plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

## PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. $V_{SENSE}$ should be connected to the $V_{TT}$ termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. $V_{DDQ}$ can be connected remotely to the $V_{DDQ}$ rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the $V_{SENSE}$ trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the $_{SENSE}$ can also be used to filter any unwanted high frequency signal. This can be an issue especially if long $_{SENSE}$ traces are used.
6. $V_{REF}$ should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the $V_{REF}$ pin.

## Physical Dimensions inches (millimeters) unless otherwise noted

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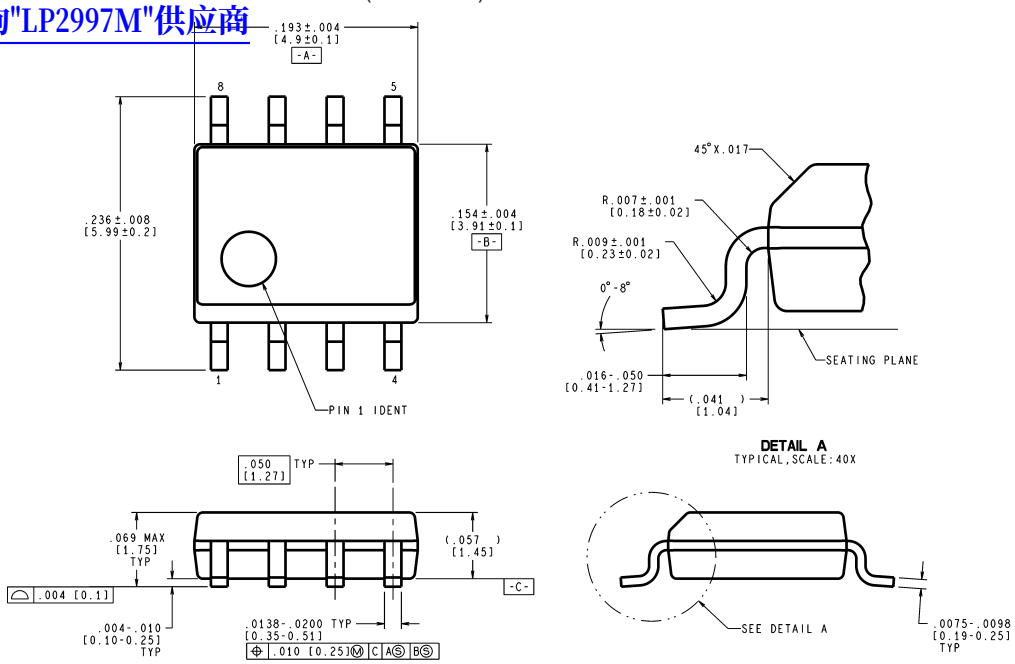
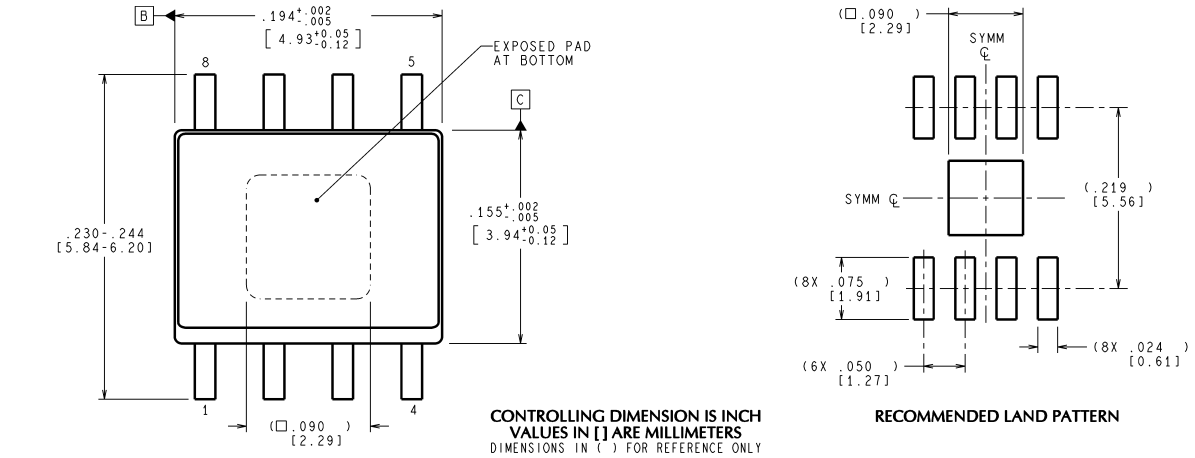



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

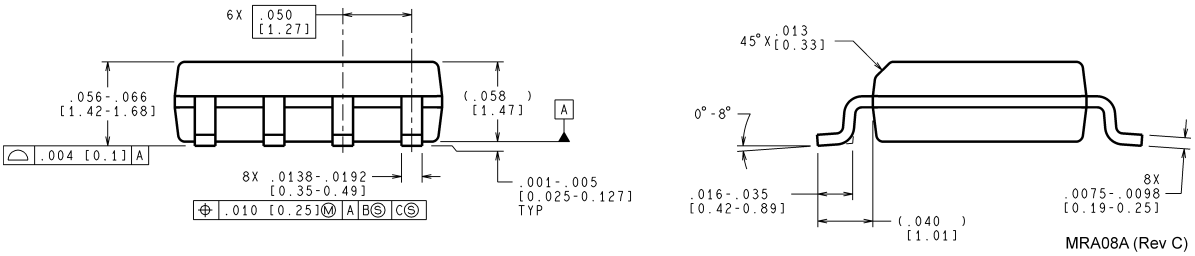
M08A (Rev J)

**8-Lead Small Outline Package (M8)**
**NS Package Number M08A**




CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

RECOMMENDED LAND PATTERN




MRA08A (Rev C)

**8-Lead PSOP Package (PSOP-8)**
**NS Package Number MRA08A**

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# Notes

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**BANNED SUBSTANCE COMPLIANCE**

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

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