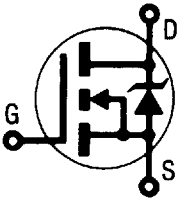
INTERNATIONAL RECTIFIER IOR

查询"2N7270"供应商

HEXFET® TRANSISTORS IRHM7450 IRHM8450 2N7270 JANSR2N7270 JANSH2N7270

N-CHANNEL

MEGA RAD HARD



500 Volt, 0.45Ω, MEGA RAD HARD HEXFET

International Rectifier's MEGA RAD HARD Technology HEXFETs demonstrate excellent threshold voltage stability and breakdown voltage stability at total radiation doses as high as $1x10^6$ Rads (Si). Under ***identical*** pre and post radiation test conditions, International Rectifier's RAD HARD HEXFETs retain ***identical*** electrical specifications up to $1x10^5$ Rads (Si) total dose. At $1x10^6$ Rads (Si) total dose, under the same pre-dose test conditions, only minor shifts in the electrical specifications are observed and are so specified in table 1. No compensation in gate drive circuitry required! In addition, these devices are capable of surviving transient ionization pulses as high as $1x10^{12}$ Rads (Si)/Sec, and return to normal operation within a few microseconds. Single Event Effect (SEE) testing of International Rectifier RAD HARD HEXFETs has demonstrated virtual immunity to SEE failure. Since the MEGA RAD process utilizes International Rectifier's patented HEXFET technology, the user can expect the highest quality and reliability in the industry.

RAD HARD HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits in space and weapons environments.

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRHM7450	500V	0.45Ω	11A
IRHM8450	500V	0.45Ω	11A

FEATURES:

- Radiation Hardened up to $1x10^6$ Rads (Si)
- Single Event Burnout (SEB) Hardened
- Single Event Gate Rupture (SEGR) Hardened
- Gamma Dot (Flash X-Ray) Hardened
- Neutron Tolerant
- Identical Pre and Post Electrical Test Conditions
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets

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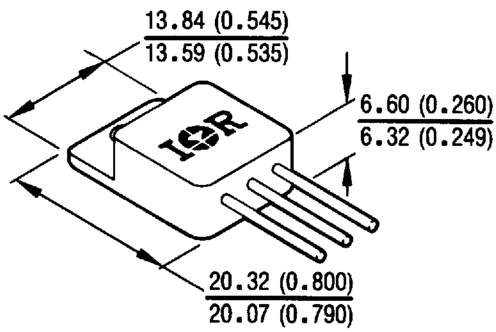
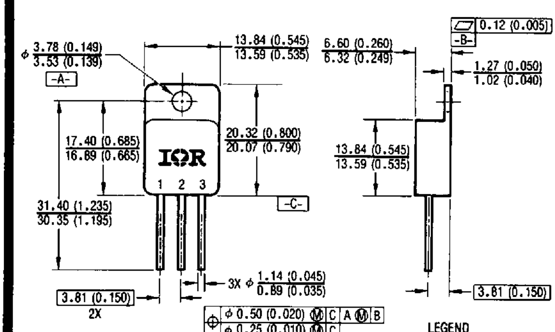
CASE STYLE AND DIMENSIONS





CAUTION

BERYLLIA WARNING PER MIL-S-19500
SEE PAGE H-262

LEGEND
1 DRAIN
2 SOURCE
3 GATE

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

*For optional leadform configurations see page H-262, fig. 33

Conforms to JEDEC Outline TO-254AA*

Dimensions in Millimeters and (Inches)

Absolute Maximum Ratings ①

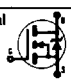
	Parameter	IRHM7450, IRHM8450	Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	11	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	7.0	
I_{DM}	Pulsed Drain Current ②	44	
P_D @ T_C = 25°C	Max. Power Dissipation	150	W
	Linear Derating Factor	1.2	W/K ⑥
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
I_{AR}	Avalanche Current ②	11	A
E_{AR}	Repetitive Avalanche Energy ②	15	mJ
dv/dt	Peak Diode Recovery dv/dt ④	3.5	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	−55 to 150	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	9.3 (typical)	g

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified) ①

	Parameter	Min.	Typ.	Max.	Units	Test Conditions ⑪
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 1.0 mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.6	—	V/°C	Reference to 25°C, I_D = 1.0 mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—		0.45	Ω	V_{GS} = 12V, I_D = 7.0A ⑤
		—		0.50		V_{GS} = 12V, I_D = 11A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0 mA
g_{fs}	Forward Transconductance	4.0		—	S (℧)	V_{DS} ≥ 15.0V, I_{DS} = 7.0A ⑤
I_{DSS}	Zero Gate Voltage Drain Current	—	—	50	µA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V
		—	—	250		V_{DS} = 0.8 x Max. Rating V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	−100		V_{GS} = −20V
Q_g	Total Gate Charge	—	—	150	nC	V_{GS} = 12V, I_D = 11A
Q_{gs}	Gate-to-Source Charge	—	—	30		V_{DS} = Max. Rating x 0.5
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	75		See Fig. 23 and 31
$t_{d(on)}$	Turn-On Delay Time	—	—	45	ns	V_{DD} = 250V, I_D = 11A, R_G = 2.35Ω
t_r	Rise Time	—	—	190		See Fig. 28
$t_{d(off)}$	Turn-Off Delay Time	—	—	190		
t_f	Fall Time	—	—	130		
L_D	Internal Drain Inductance	—	8.7	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal inductances.
L_S	Internal Source Inductance	—	8.7	—		Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	—	4000	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	330	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	—	52	—		See Fig. 22

Source-Drain Diode Ratings and Characteristics ①

	Parameter	Min.	Typ.	Max.	Units	Test Conditions ⑪
I_S	Continuous Source Current (Body Diode)	—	—	11	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	44		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J = 25°C, I_S = 11A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time	—	—	1100	ns	T_J = 25°C, I_F = 11A, di/dt ≤ 100 A/µs ⑤
Q_{RR}	Reverse Recovery Charge	—	—	16	µC	V_{DD} ≤ 50V
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	0.83	K/W ⑥	
R_{thJA}	Junction-to-Ambient	—	—	48		
R_{thCS}	Case-to-Sink	—	0.21	—		Typical socket mount

Radiation Performance of Rad Hard HEXFET's

International Rectifier Radiation Hardened HEXFETs are tested to verify their hardness capability. The hardness assurance program at International Rectifier uses two radiation environments.

Every manufacturing lot is tested in a low dose rate (total dose) environment per MIL-STD-750, test method 1019. International Rectifier has imposed a standard gate voltage of 12 volts per note 7 and figure 8a and a V_{DSS} bias condition equal to 80% of the device rated voltage per note 8 and figure 8b. Pre and Post radiation limits of the devices irradiated to $1x10^5$ Rads (Si) are identical and are presented in table 1, column 1, IRHM7450. Device performance limits at a post radiation level of $1x10^6$ Rads (Si) are presented in Table 1, column 2, IRHM8450. The values in Table 1 will be met for either of the two low dose rate test circuits that are used. Typical delta curves showing radiation response appear in Figures 1 through 5. Typical post radiation curves appear in Figures 10 through 17.

Both pre and post radiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison. It should be noted that at a radiation level of $1x10^5$ Rads (Si), no change in limits are specified in DC parameters. At a radiation level of $1x10^6$ Rads (Si), leakage remains low and the device is usable with no change in drive circuitry required.

High dose rate testing may be done on a special request basis, using a dose rate up to $1x10^{12}$ Rads (Si)/Sec. Photocurrent and transient voltage waveforms are shown in Figure 7, and the recommended test circuit to be used is shown in figure 9.

International Rectifier radiation hardened HEXFETs have been characterized in Neutron and heavy ion Single Event Effects (SEE) environments. The effects on bulk silicon of the type used by International Rectifier on RAD HARD HEXFETs are shown in figure 6. Single Event Effects characterization is shown in Table 3.

Table 1. Low Dose Rate ⑦ ⑧

	Parameter	IRHM7450 100K Rads (Si) min.	IRHM7450 100K Rads (Si) max.	IRHM8450 1000K Rads (Si) min.	IRHM8450 1000K Rads (Si) max.	Units	Test Conditions ⑪
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	—	500	—	V	V_{GS} = 0V, I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage ⑤	2.0	4.0	1.25	4.5	V	V_{GS} = V_{DS}, I_D = 1.0 mA
I_{GSS}	Gate-to-source Leakage Forward	—	100	—	100	nA	V_{GS} = +20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	50	—	100	µA	V_{DS} = 0.8 x Max Rating, V_{GS} = 0
$R_{DS(on)1}$	Static Drain-to-Source On-State Resistance One ⑤	—	0.45	—	0.6	Ω	V_{GS} = 12V, I_D = 7.0A
V_{SD}	Diode Forward Voltage ⑤	—	1.6	—	1.6	V	T_C = 25°C, I_S = 11A, V_{GS} = 0V

Table 2. High Dose Rate ⑨

	Parameter	10^{11} Rads (Si)/sec Min.	Typ.	Max.	10^{12} Rads (Si)/sec Min.	Typ.	Max.	Units	Test Conditions
V_{DSS}	Drain-to-Source Voltage	—	—	400	—	—	400	V	Applied drain-to-source voltage during gamma-dot
I_{PP}		—	8	—	—	8	—	A	Peak radiation induced photo-current
di/dt		—	—	15	—	—	3	A/µsec	Rate of rise of photo-current
L_1		27	—	—	133	—	—	µH	Circuit inductance required to limit di/dt

Table 3. Single Event Effects

Parameter	Typ	Units	Ion	LET (Si) (MeV/mg/cm²)	Range (µm)	V_{DS} Bias (V)	V_{GS} Bias (V)
V_{DS} ⑩	275	V	Ni	28	~41	275	-5

① See Figures 18 through 31 for pre-radiation curves.

② Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 26) Refer to Current HEXFET reliability report

③ @ V_{DD} = 25V, Starting T_J = 25°C, L ≥ 7.4 mH, R_G = 25Ω, Peak I_L = 11A

④ I_{SD} ≤ 11A, di/dt ≤ 140 A/µs, V_{DD} ≤ BV_{DSS}, T_J ≤ 150°C Suggested R_G = 2.35Ω

⑤ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑥ K/W = °C/W W/K = W/°C

⑦ **Total Dose Irradiation with V_{GS} Bias.** +12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019. (See figure 8a)

⑧ **Total Dose Irradiation with V_{DS} Bias.** V_{DS} = 0.8 rated BV_{DSS} (pre-radiation) applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019. (See figure 8b)

⑨ This test is performed using a flash x-ray source operated in the e-beam mode (energy ~2.5 Mev), 30 nsec pulse. See figure 9.

⑩ Study sponsored by NASA. Evaluation performed at Brookhaven National Labs.

⑪ All Pre-Radiation and Post-Radiation test conditions are identical to facilitate direct comparison for circuit applications.

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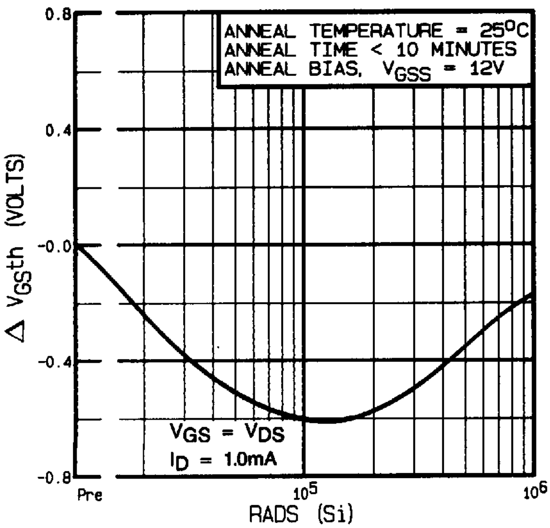

Fig. 1 — Typical Response of Gate Threshold Voltage Vs. Total Dose Exposure

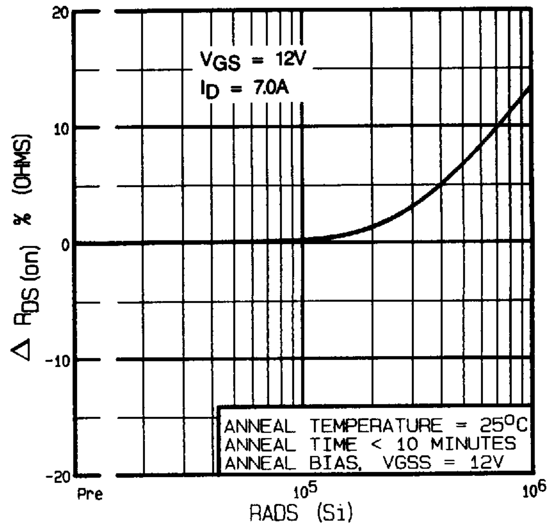

Fig. 2 — Typical Response of On-State Resistance Vs. Total Dose Exposure

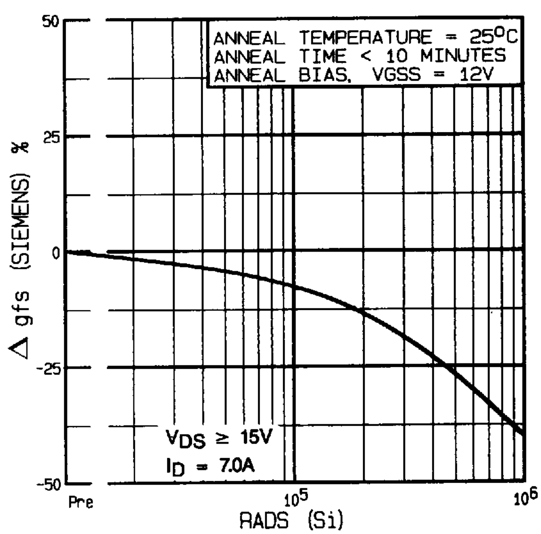

Fig. 3 — Typical Response of Transconductance Vs. Total Dose Exposure

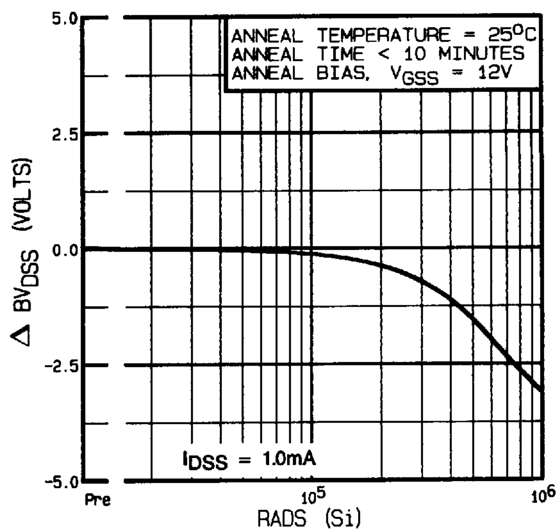

Fig. 4 — Typical Response of Drain-to-Source Breakdown Vs. Total Dose Exposure

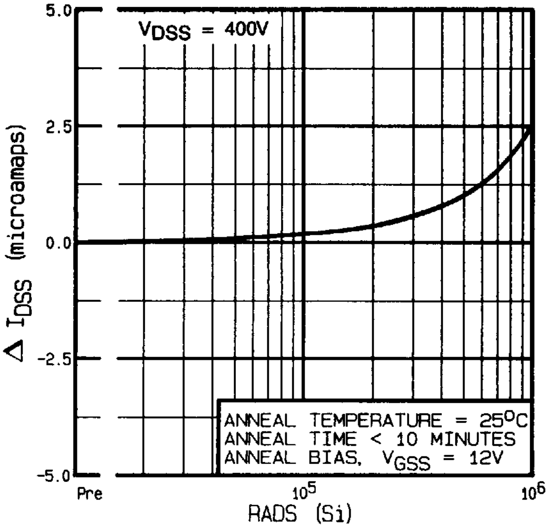

Fig. 5 — Typical Zero Gate Voltage Drain Current Vs. Total Dose Exposure

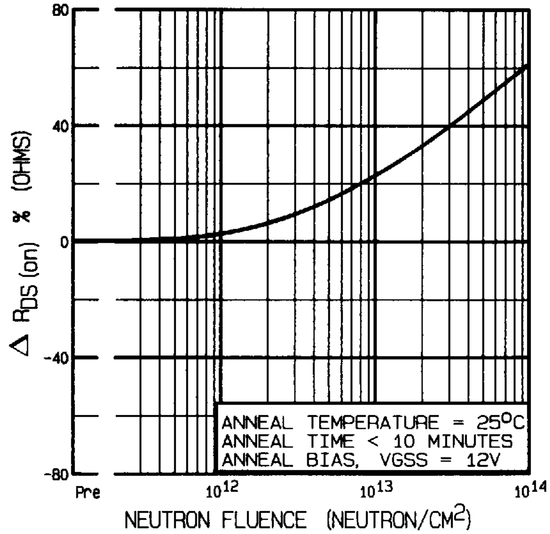

Fig. 6 — Typical On-State Resistance Vs. Neutron Fluence Level

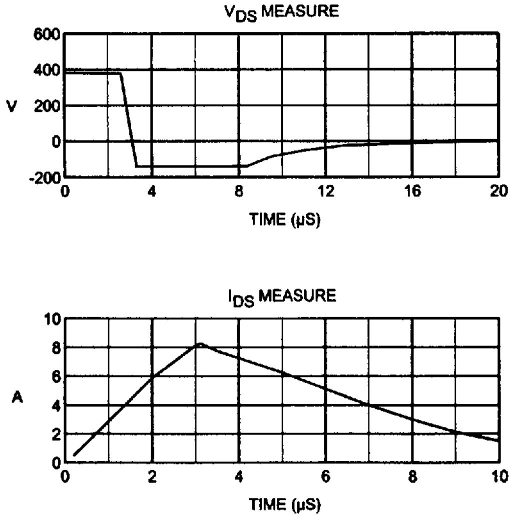

Fig. 7 — Typical Transient Response of Rad Hard HEXFET During 1 x 10^{12} Rad (Si)/Sec Exposure

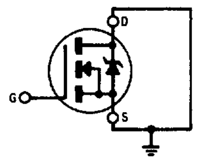

Fig. 8a — Gate Stress of V_{GSS} Equals 12 Volts During Radiation

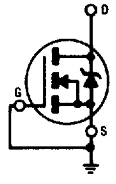

Fig. 8b — V_{DSS} Stress Equals 80% of BV_{DSS} During Radiation

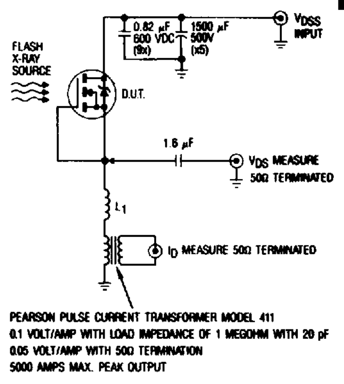

Fig. 9 — High Dose Rate (Gamma Dot) Test Circuit

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Note: Bias Conditions during radiation; V_{GS} = 12 Vdc, V_{DS} = 0 Vdc

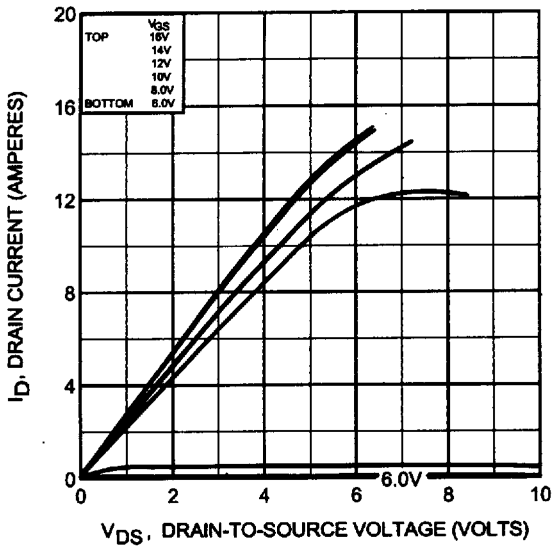

Fig. 10 — Typical Output Characteristics Pre-Radiation

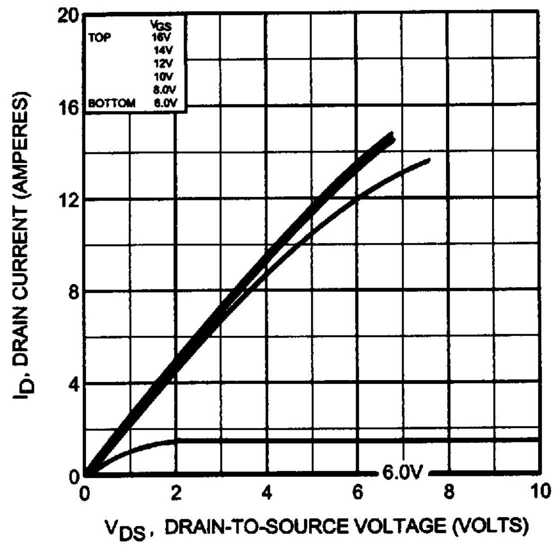

Fig. 11 — Typical Output Characteristics Post-Radiation 100K Rads (Si)

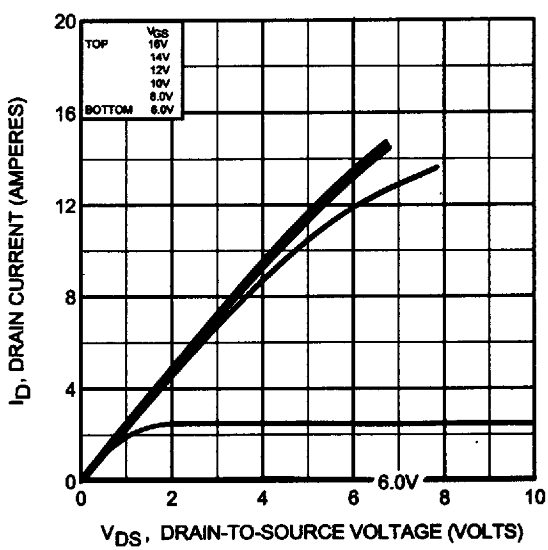

Fig. 12 — Typical Output Characteristics Post-Radiation 300K Rads (Si)

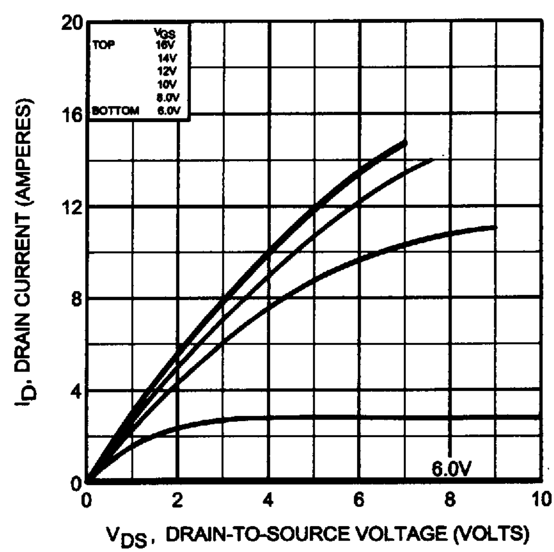

Fig. 13 — Typical Output Characteristics Post-Radiation 1 Mega Rads (Si)

Note: Bias Conditions during radiation; V_{GS} = 0 Vdc, V_{DS} = 400 Vdc

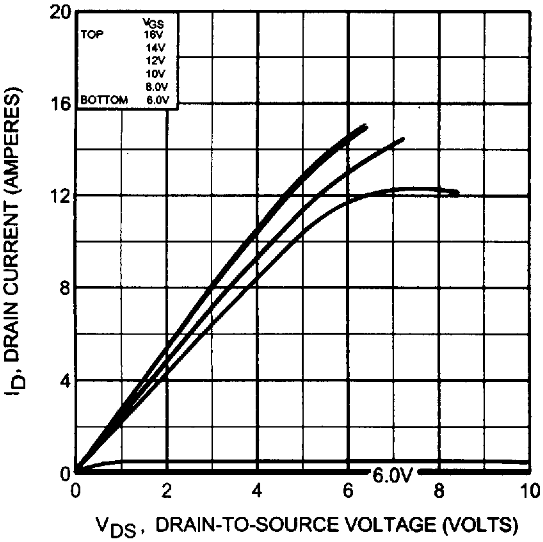

Fig. 14 — Typical Output Characteristics Pre-Radiation

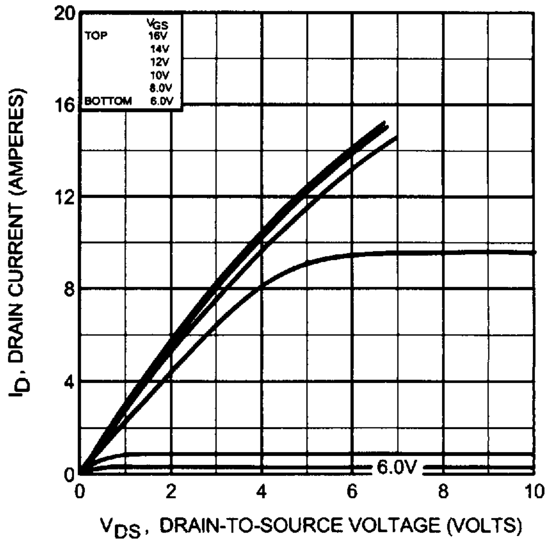

Fig. 15 — Typical Output Characteristics Post-Radiation 100K Rads (Si)

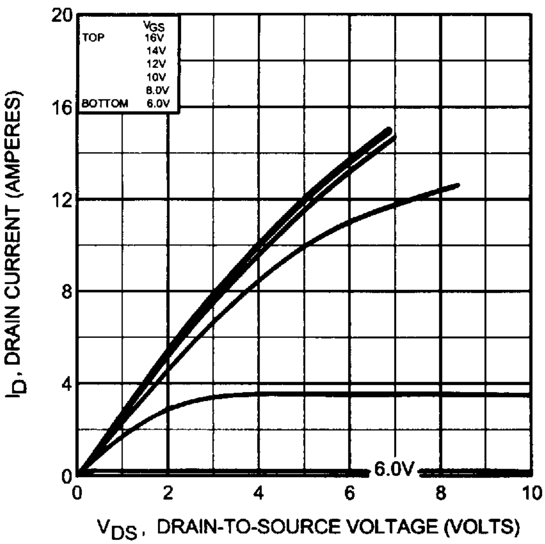

Fig. 16 — Typical Output Characteristics Post-Radiation 300K Rads (Si)

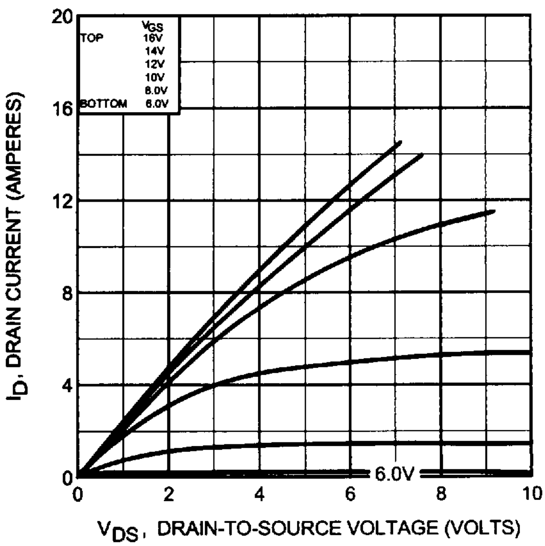

Fig. 17 — Typical Output Characteristics Post-Radiation 1 Mega Rads (Si)

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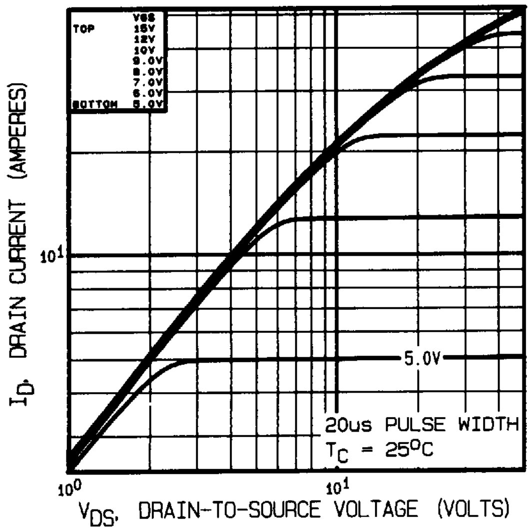

Fig. 18 — Typical Output Characteristics, T_C = 25°C

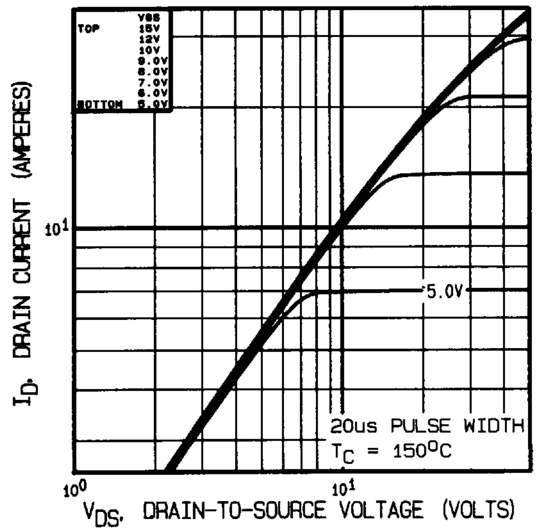

Fig. 19 — Typical Output Characteristics, T_C = 150°C

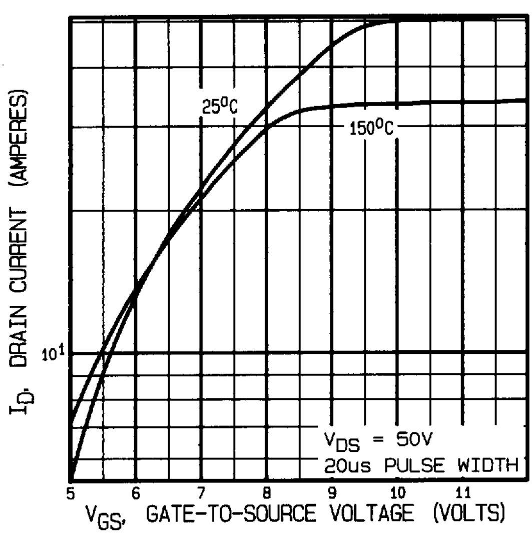

Fig. 20 — Typical Transfer Characteristics

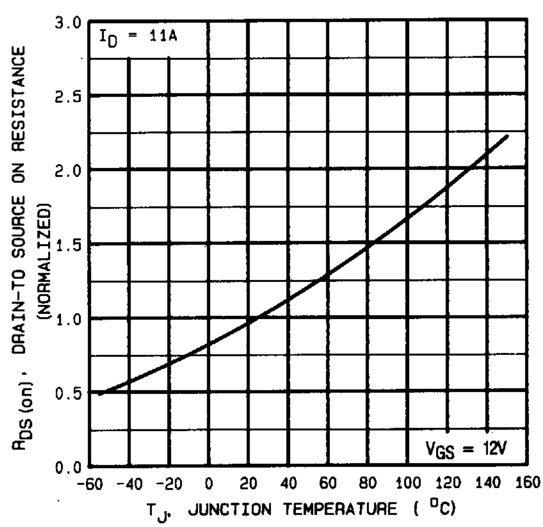

Fig. 21 — Normalized On-Resistance Vs. Temperature

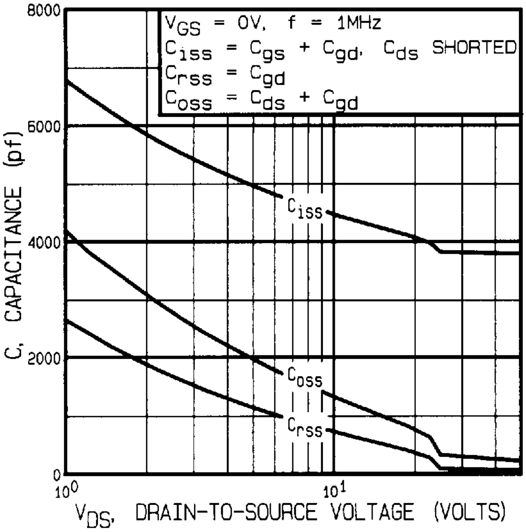

Fig. 22 — Typical Capacitance Vs. Drain-to-Source Voltage

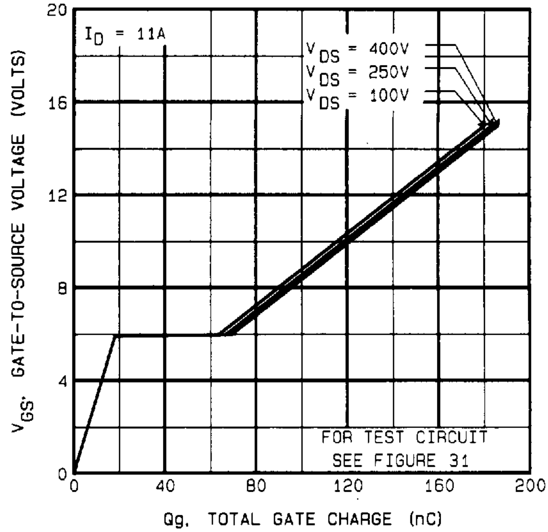

Fig. 23 — Typical Gate Charge Vs. Gate-to-Source Voltage

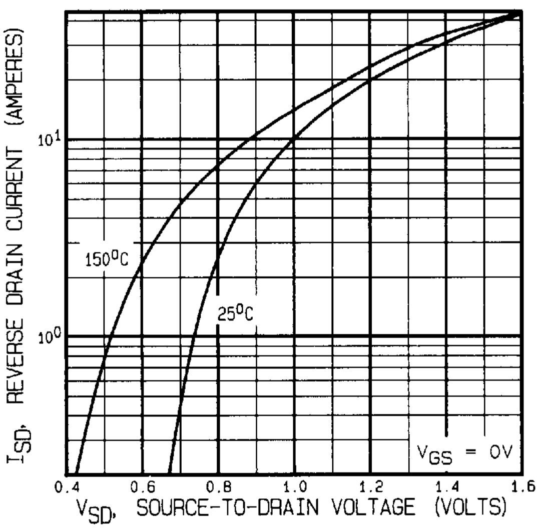

Fig. 24 — Typical Source-Drain Diode Forward Voltage

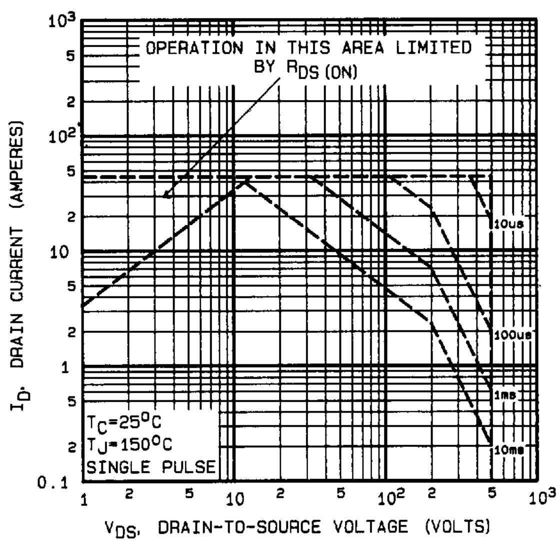

Fig. 25 — Maximum Safe Operating Area

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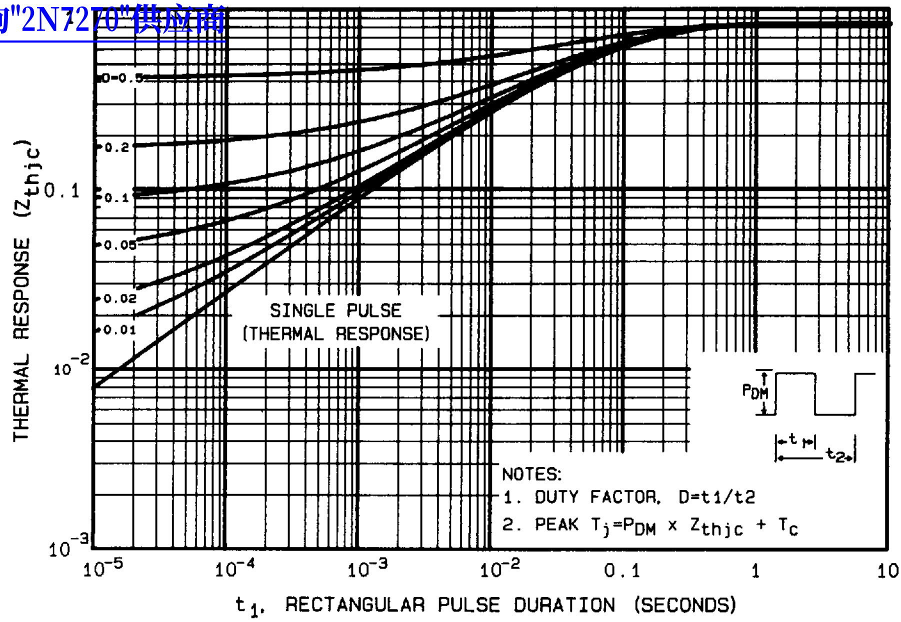

Fig. 26 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

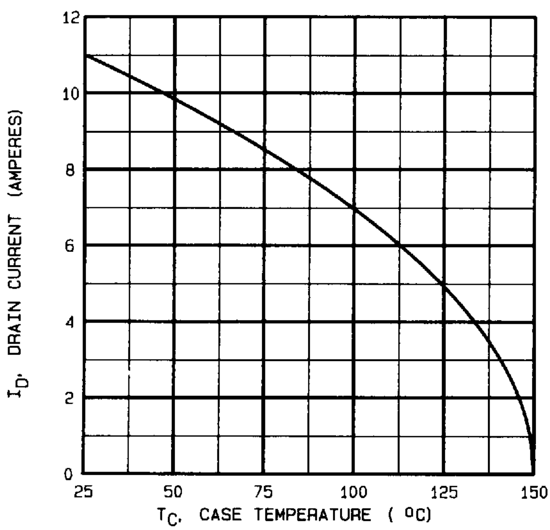

Fig. 27 — Maximum Drain Current Vs. Case Temperature

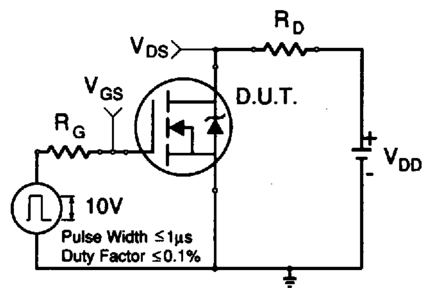

Fig. 28a — Switching Time Test Circuit

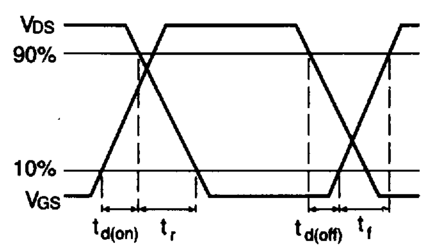

Fig. 28b — Switching Time Waveforms

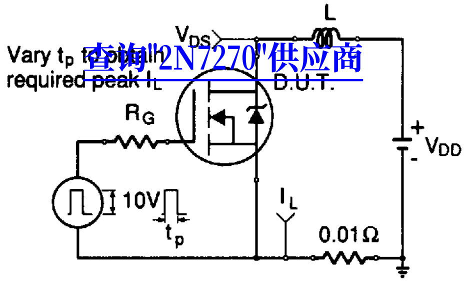

Fig. 29a — Unclamped Inductive Test Circuit

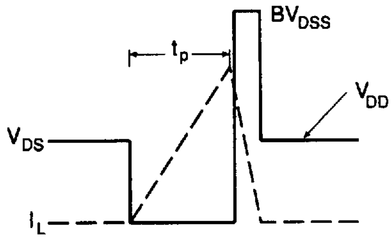

Fig. 29b — Unclamped Inductive Waveforms

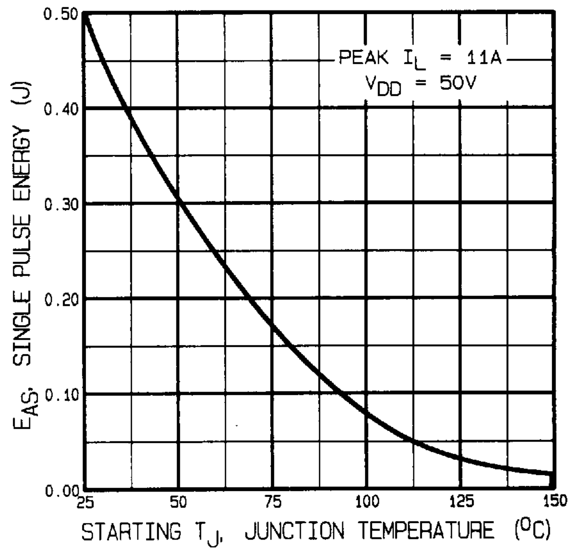

Fig. 29c — Maximum Avalanche Energy Vs. Starting Junction Temperature

H

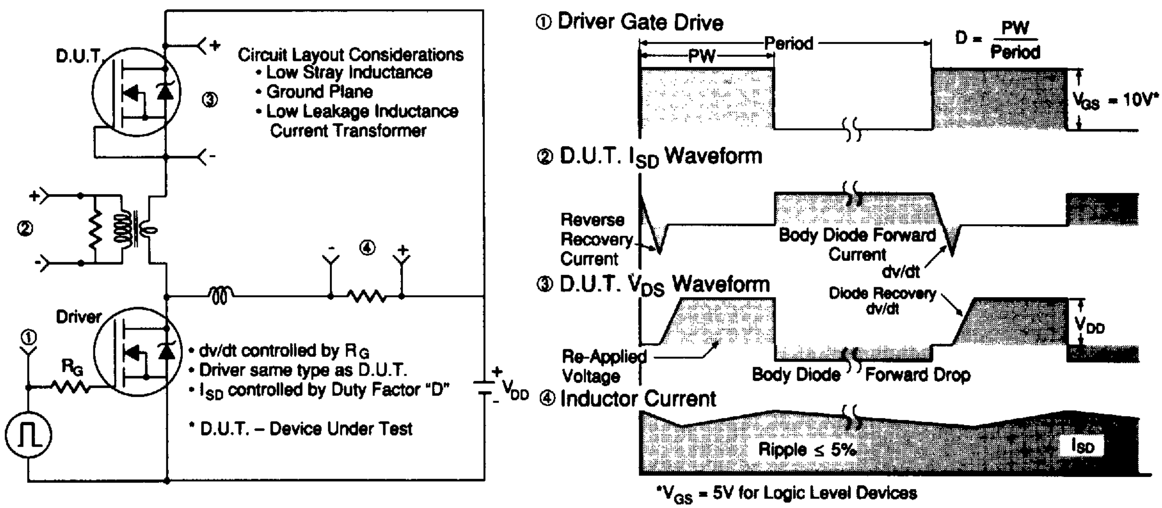

Fig. 30 — Peak Diode Recovery dv/dt Test Circuit

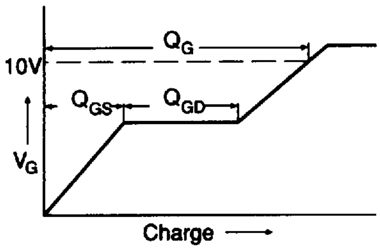

Fig. 31a — Basic Gate Charge Waveform

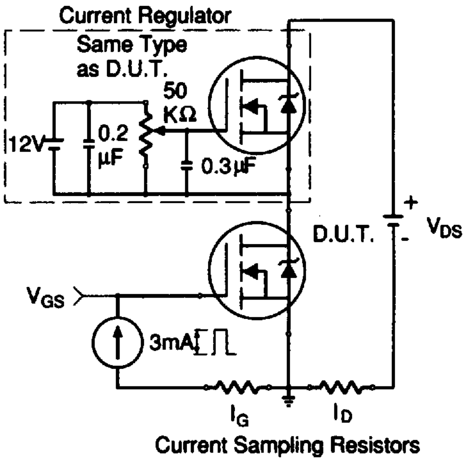

Fig. 31b — Gate Charge Test Circuit

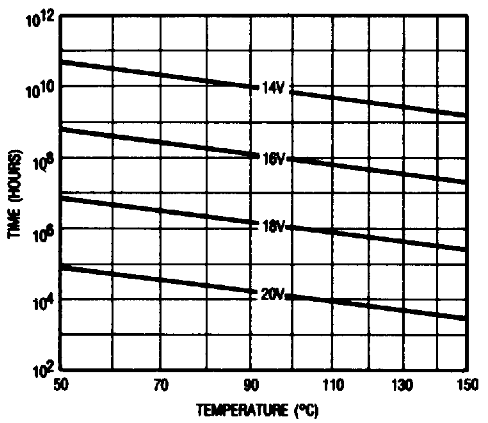

Fig. 32 — Typical Time to Accumulated 1% Failure

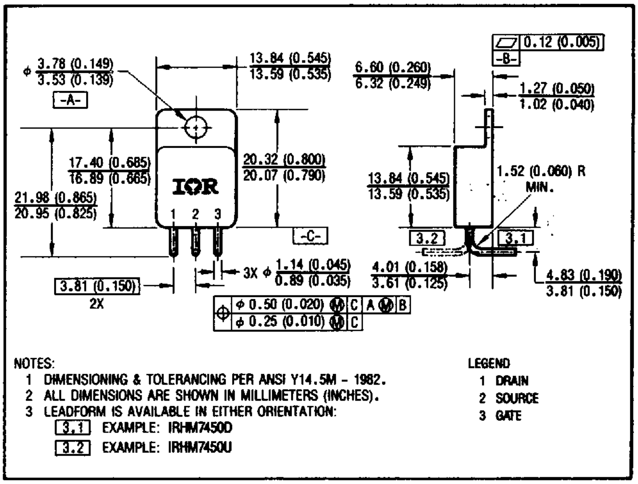

Fig. 33 – Optional Leadforms for Outline TO-254

BERYLLIA WARNING PER MIL-S-19500

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.