# MC44250

*Advance Information*

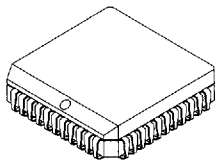
# Triple 8-Bit Video ADC

## CMOS

The MC44250 contains three independent parallel analog–to–digital flash converters (ADC). Each ADC consists of 256 latching comparators and an encoder. Video may be ac or dc coupled. With ac coupling, input clamping provides for internal dc restoration. The MC44250 also contains a dithering generator for video processing performance enhancements.

The MC44250 is especially suitable as a front–end converter in TV–picture digital processing (picture–in–picture, frame storage, etc.). The high speed conversion rate of the ADC is suitable for video bandwidth of well over 6 MHz.

- 15 MHz Maximum Sampling Rate
- Output Latching Minimizes Skew
- Input Clamps Suitable for RGB and YUV Applications
- Built–In Dither Generator with Subsequent Digital Correction
- Featured on the MC144000EVK PC Video Capture Evaluation Kit
- Single 5–Volt Power Supply
- Operating Temperature Range: – 40 to + 85°C

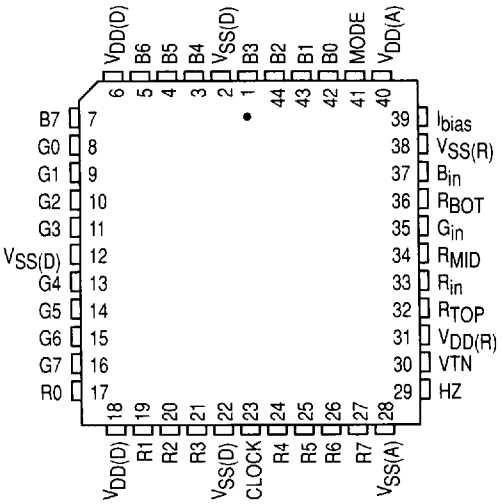


**FN SUFFIX**
44-LEAD PLCC
CASE 777–02

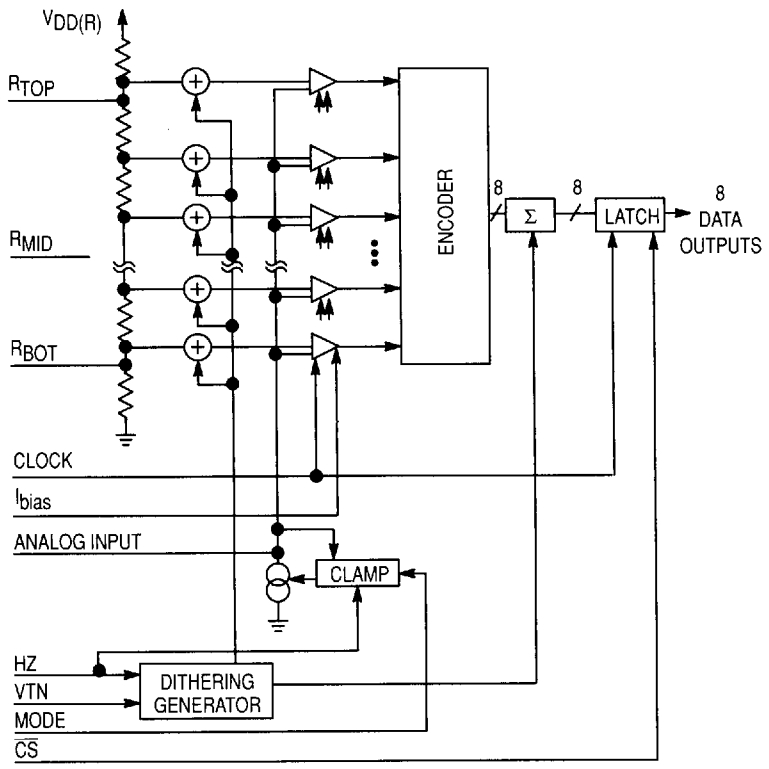
**ORDERING INFORMATION**

| | |
|---|---|
| MC44250FN | PLCC |

**PIN ASSIGNMENT**




**SIMPLIFIED BLOCK DIAGRAM OF ONE OF THE ADCs**




This document contains information on a new product. Specifications and information herein are subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS*



| Symbol | Characteristic | Value | Unit |
|---|---|---|---|
| $V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$ | DC Supply Voltage (referenced to $V_{SS}$) | – 0.5 to + 6.0 | V |
| $V_{in}$ | Input Voltage, All Pins | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | DC Input Current Per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current Per Pin | ± 25 | mA |
| $T_{stg}$ | Storage Temperature Range | – 65 to + 150 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the following Operating Ranges.

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$) ($V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$; $R_{bias}$ (pin 39) = 5 kΩ to ground)

### OPERATING RANGES

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD(A)}$, $V_{DD(D)}$, $V_{DD(R)}$ | Power Supply Voltage | 4.5 | 5.5 | V |
| $I_{DD(A)}$ | Analog Supply Current | — | 55 | mA |
| $I_{DD(R)}$ | Reference Supply Current | — | 28 | mA |
| $I_{DD(D)}$ | Digital Supply Current | — | 5 | mA |
| $T_A$ | Operating Ambient Temperature Range | – 40 | + 85 | °C |

### A/D CONVERTER

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $C_{in}$ | Input Capacitance | — | 60 | pF |
| $V_{min}$ | See Figure 12 | 0.3 x $V_{DD}$ | 0.36 x $V_{DD}$ | V |
| $V_{max}$ | See Figure 12 | 0.876 x $V_{DD}$ | 0.942 x $V_{DD}$ | V |
| $V_{range}$ | See Figure 12 | 0.576 x $V_{DD}$ | 0.6 x $V_{DD}$ | V |
| Gain | See Figure 12 (Note 1) | 0.96 | 1.0 | LSB |
| DNL | Differential Nonlinearity (Note 1) | — | ± 1.0 | LSB |
| INL | Integral Nonlinearity (Note 1) | — | ± 2.0 | LSB |
| $E_{gain}$ | Gain Difference (Note 2) | — | ± 1.0 | % |
| $E_{off}$ | Offset Difference (Notes 1, 2) | — | ± 4.0 | LSB |

### CLOCK INPUT

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | Clock Input High Level | 2 | — | V |
| $V_{IL}$ | Clock Input Low Level | — | 0.8 | V |
| $I_{IL}$ | Low Level Input Current | — | ± 2.0 | µA |
| $I_{IH}$ | High Level Input Current | — | ± 2.0 | µA |
| $F_{CLK}$ | Clock Frequency | — | 15 | MHz |
| $t_{wL}$ | Clock Low Duration, Figure 1 | 27.5 | — | ns |
| $t_{wH}$ | Clock High Duration, Figure 1 | 27.5 | — | ns |
| $t_r$ | Clock Rise Time (10% to 90%), Figure 1 | — | 15 | ns |
| $t_f$ | Clock Fall Time (10% to 90%), Figure 1 | — | 15 | ns |

### HZ AND VTN INPUTS



| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IH}$ | HZ and VTN High Level Voltage | 2.0 | — | V |
| $V_{IL}$ | HZ and VTN Low Level Voltage | — | 0.8 | V |
| $I_{IL}$ | Low Level Input Current | — | ± 2.0 | µA |
| $I_{IH}$ | High Level Input Current | — | ± 2.0 | µA |
| $t_H$ | HZ High Time, Figure 3 | 3 | — | ns |

### CLAMPING NETWORK (Measured on R, G, B Inputs)

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $I_{sink}$ | Clamping Sink Current | 2.0 | 5.0 | µA |
| $I_{source}$ | Clamping Source Current | – 5.0 | – 2.0 | µA |
| $D_{ICL}$ | Clamping Current Difference (Note 2) | — | 0.1 | µA |
| $\Delta V_{clamp}$ | Clamping Levels (Max. Deviation Compared to Table 1) | — | ± 1.0 | LSB |

NOTES:
1. Unit "LSB" means ideal LSB (see definitions section).
2. "Difference" means difference between any two converters in the same package.

### RESISTIVE REFERENCE NETWORK

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $Z_{TOP}$ | $R_{TOP}$ Output Impedance | 24 | 56 | Ω |
| $Z_{BOT}$ | $R_{BOT}$ Output Impedance | 60 | 140 | Ω |
| $Z_{MID}$ | $R_{MID}$ Output Impedance | 60 | 140 | Ω |

### MODE INPUT

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $V_{IL}$ | Logical "0" Level | 0 | 0.8 | V |
| $V_{IH}$ | Logical "1" Level | 4.2 | $V_{DD(D)}$ | V |
| $V_{IZ}$ | Logical "Open" Level | 1.8 | 3.2 | V |
| $I_{IL}$ | Input Current at "0" Level | — | ± 50 | µA |
| $I_{IH}$ | Input Current at "1" Level | — | ± 50 | µA |
| $I_{IZ}$ | Input Current at "Open" Level | — | ± 50 | µA |

### DATA OUTPUTS

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $t_d$ | Delay from Sample Clock to Valid Output, Figure 2 | 2.5 | 2.5 | Cycle |
| $I_{OL}$ | Output Sinking Current at $V_{out}$ = 0.4 V | 2.0 | — | mA |
| $I_{OH}$ | Output Sourcing Current at $V_{out} = V_{DD} - 0.1$ V | – 0.4 | — | mA |
| $t_{QLH}$, $t_{QHL}$ | Propagation Delay from the Clock Rising Edge to Valid Data Output ($C_L$ = 15 pF), Figure 1 | — | 40 | ns |

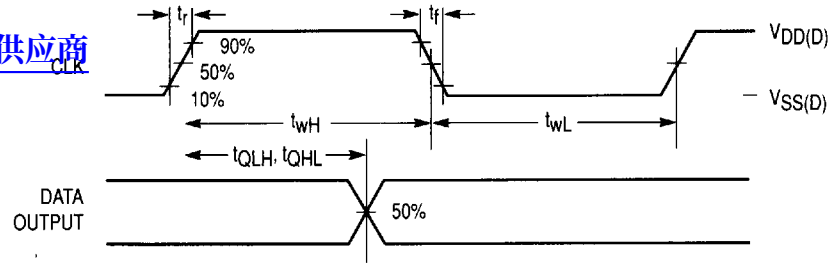



**Figure 1. Clock and Output Timing**

## PIN ASSIGNMENTS

| Pin No. | Name | Function |
|---|---|---|
| 1 | B3 | Output Blue, Bit 3 |
| 2 | $V_{SS(D)}$ | $V_{SS}$, Digital |
| 3 | B4 | Output Blue, Bit 4 |
| 4 | B5 | Output Blue, Bit 5 |
| 5 | B6 | Output Blue, Bit 6 |
| 6 | $V_{DD(D)}$ | $V_{DD}$, Digital |
| 7 | B7 | Output Blue, Bit 7 (MSB) |
| 8 | G0 | Output Green, Bit 0 (LSB) |
| 9 | G1 | Output Green, Bit 1 |
| 10 | G2 | Output Green, Bit 2 |
| 11 | G3 | Output Green, Bit 3 |
| 12 | $V_{SS(D)}$ | $V_{SS}$, Digital |
| 13 | G4 | Output Green, Bit 4 |
| 14 | G5 | Output Green, Bit 5 |
| 15 | G6 | Output Green, Bit 6 |
| 16 | G7 | Output Green, Bit 7 (MSB) |
| 17 | R0 | Output Red, Bit 0 (LSB) |
| 18 | $V_{DD(D)}$ | $V_{DD}$, Digital |
| 19 | R1 | Output Red, Bit 1 |
| 20 | R2 | Output Red, Bit 2 |
| 21 | R3 | Output Red, Bit 3 |
| 22 | $V_{SS(D)}$ | $V_{SS}$, Digital |

| Pin No. | Name | Function |
|---|---|---|
| 23 | CLK | Clock Input |
| 24 | R4 | Output Red, Bit 4 |
| 25 | R5 | Output Red, Bit 5 |
| 26 | R6 | Output Red, Bit 6 |
| 27 | R7 | Output Red, Bit 7 (MSB) |
| 28 | $V_{SS(A)}$ | $V_{SS}$, Analog |
| 29 | HZ | Horizontal Sync |
| 30 | VTN | Vertical Sync |
| 31 | $V_{DD(R)}$ | Reference Voltage |
| 32 | $R_{TOP}$ | Reference Tapping, Top |
| 33 | $R_{in}$ | Analog Input, Red |
| 34 | $R_{MID}$ | Reference Tapping, Middle |
| 35 | $G_{in}$ | Analog Input, Green |
| 36 | $R_{BOT}$ | Reference Tapping, Bottom |
| 37 | $B_{in}$ | Analog Input, Blue |
| 38 | $V_{SS(R)}$ | $V_{SS}$ for Reference Voltage |
| 39 | $I_{BIAS}$ | To External Bias Resistor |
| 40 | $V_{DD(A)}$ | $V_{DD}$, Analog |
| 41 | MODE | Clamp Level Select Input |
| 42 | B0 | Output Blue, Bit 0 (LSB) |
| 43 | B1 | Output Blue, Bit 1 |
| 44 | B2 | Output Blue, Bit 2 |

## PIN DESCRIPTIONS



### RESISTIVE REFERENCE NETWORK

**$R_{TOP}$ (Pin 32)**
**$R_{BOT}$ (Pin 34)**
**$R_{MID}$ (Pin 36)**

Taps on the reference ladder are pinned out, providing access to the bottom ($R_{BOT}$), the top ($R_{TOP}$), and the middle scale points. These pins are intended for ac bypassing as ladder noise may present a problem. The value of the decoupling capacitor should not exceed 47 nF. Large capacitance values can cause problems because of the amount of energy stored. When a system containing the MC44250 is rapidly powered down and up, the capacitor voltage may exceed the supply voltage during the power up and cause a latch–up condition. Failure to adequately decouple these pins can adversely affect the conversion process.

### SUPPLY PINS

**$V_{DD(A)}$ (Pin 40)**
**$V_{DD(D)}$ (Pins 6, 18)**
**$V_{DD(R)}$ (Pin 31)**

The three types of supply pins are analog, digital, and reference. The dc voltage applied to all four pins must be maintained such that

$$V_{DD(A)} = V_{DD(D)} = V_{DD(R)}.$$

Each pin must be carefully decoupled to ground as close to the package as possible, and particular care should be taken with $V_{DD(R)}$ as any noise present on this pin will appear in the output data as an equivalent input noise. This noise will be present on the $R_{in}$, $G_{in}$ and $B_{in}$ input pins in a ratio of 1:1 to the input noise (worst case condition). Noise reduction can be improved by incorporating choke coil inductors in series with the power supply rails.

### ANALOG INPUTS

**$R_{in}$ (Pin 33)**
**$G_{in}$ (Pin 35)**
**$B_{in}$ (Pin 37)**

The analog signals to be converted are input at these pins. An on–chip clamp circuit for dc restoration is available when using ac coupling. The clamp circuit operation is activated by the presence of the signal at the HZ input. This signal is derived from the composite sync information and must be coincident with the horizontal sync of the composite video waveform for proper operation. $Y_{in}$, $U_{in}$, and $V_{in}$ may be used instead of the RGB signals. In this case the conversion will be a YUV analog–to–digital conversion.

**$I_{bias}$ (Pin 39)**

The comparator bias current is set by connecting an external resistor between $I_{bias}$ and ground. The conversion rate is guaranteed for a resistor value of 5.1 kΩ ± 5% and will decrease logarithmically with increased resistance. The resistor must be placed adjacent to the $I_{bias}$ pin. No decoupling capacitor is allowed on this pin.

### DIGITAL OUTPUTS

**R0 – R7 (Pins 17, 19–21, 24–27)**
**G0 – G7 (Pins 8–11, 13–16)**
**B0 –B7 (Pins 42–44, 1,3–5, 7)**

These pins are the parallel output for the digital value for the RGB signals. R0 through R7 are the digital equivalent of the analog RED input, G0 through G7 are equivalent to the GREEN input, and B0 through B7 are equivalent to the BLUE input. If YUV analog signals have been input instead of the RGB signals the digital outputs will be Y0 through Y7, U0 through U7 and V0 through V7.

### DIGITAL INPUTS

**Clock (Pin 23)**

The analog input voltages to be converted are sensed at the falling edge of the clock signal and the corresponding data is present on the digital outputs at the clock signal rising edge, 2.5 cycles later (see Figure 2).

**HZ (Pin 29)**

This is the horizontal synchronization input, and is used to increment the dither generator. The clamp network is also controlled by HZ to ensure proper dc restoration for $R_{in}$, $G_{in}$, and $B_{in}$ before conversion.

**VTN (Pin 30)**

The vertical synchronization input, VTN, resets the dither generator after every second vertical sync pulse (after each frame).

**MODE (Pin 41)**

This pin is used to select the proper clamp levels (see Table 1).

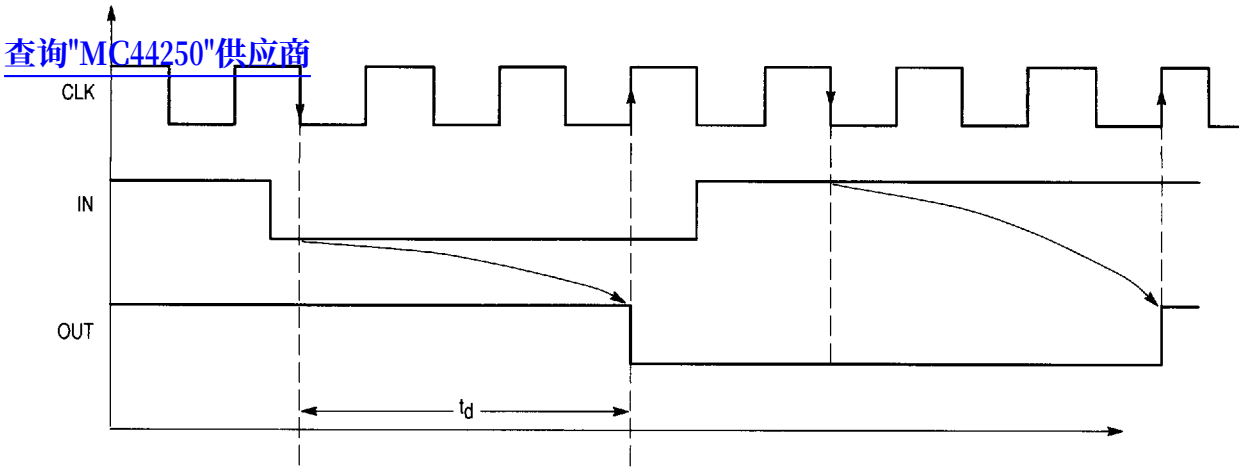



**Figure 2. Conversion Timing Functional Characteristics**

## CIRCUIT OPERATION

### GENERAL

The MC44250 contains three independent parallel analog–to–digital converters (ADC). Each ADC consists of 256 latching comparators and an encoder. The MC44250 may be used to convert RGB or YUV video information from an analog to a digital format, or as a triple ADC for non–video information. For video processing performance enhancement, each ADC has a dither generator with subsequent digital correction designed into it. The dithering generator reduces display degradation from granulation of the luminance information caused by quantization errors of the digitizing process. Each ADC is driven from a common clock and receives common sync information from the HZ and VTN pins. In addition, the VTN pin controls the dithering function and disables the dithering generator when VTN is pulled low. The sampling of the analog input signals occurs at the falling edge of the clock signal, whereas the digital outputs change state at the rising clock edge. The bias current of the comparators is set by an external resistor. Input clamps allow for ac coupling of the input signals.

### CLAMP NETWORK

The MC44250 can be operated either dc coupled or ac coupled. When dc coupled, the MC44250 will track the average dc level of the input waveform. For ac coupling, an on–chip dc restoration circuit samples and adjusts the average dc level of the input signal. The MC44250 has three selectable clamping levels for ac coupling. The clamp levels are selected by the MODE pin according to Table 1. In the RGB mode, the clamping levels are set to 16/256, corresponding to 6.3% of full range. In the YUV mode, the UV clamping levels are set to 128/256 (50%), and the Y input to either 16/256 or 64/256 (25%).

When input HZ (horizontal) is high, as illustrated in Figure 3, the voltage difference between the analog input voltage and the clamp reference voltage is integrated within each clamp network. At the falling edge of HZ, a latching comparator senses the sign of the integrator output voltage. Depending on this result, either a sinking or a sourcing current is applied to the analog input pin as long as input HZ remains low.

For video applications, the timing of HZ is critical to the proper operation of the ADC. The frequency of HZ should be locked to the line frequency of the video input. The pulse width and timing of HZ with respect to the video signal is shown in Figure 5. The top curve represents the horizontal synchronizing and blanking interval for a video signal. The pulse width of HZ, ($t_H$) should be less than the width of the back porch, ($t_{BP}$) and coincident with it. In all cases, HZ must return low before the end of the back porch, $t_{BP}$.

**Table 1. Clamping Levels**

| MODE (Pin 41) | Application | Clamp Levels | $G_{in}$ | $R_{in}$ | $B_{in}$ |
|---|---|---|---|---|---|
| L | RGB | | 16/256 | 16/256 | 16/256 |
| H | Y–UV Mode Without Sync | Format | 16/256 | 128/256 | 128/256 |
| Open | Y–UV Mode With Sync | | 64/256 | 128/256 | 128/256 |

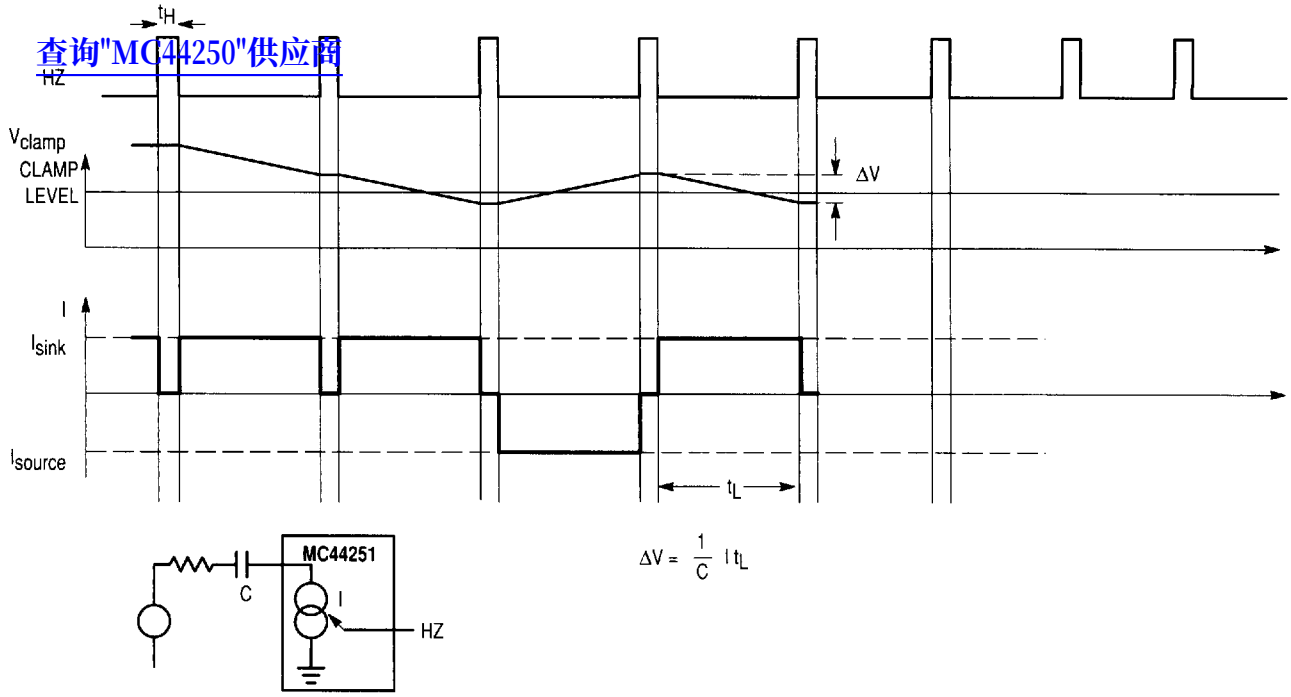



**Figure 3. Clamp Network Timing Diagram — Operation**

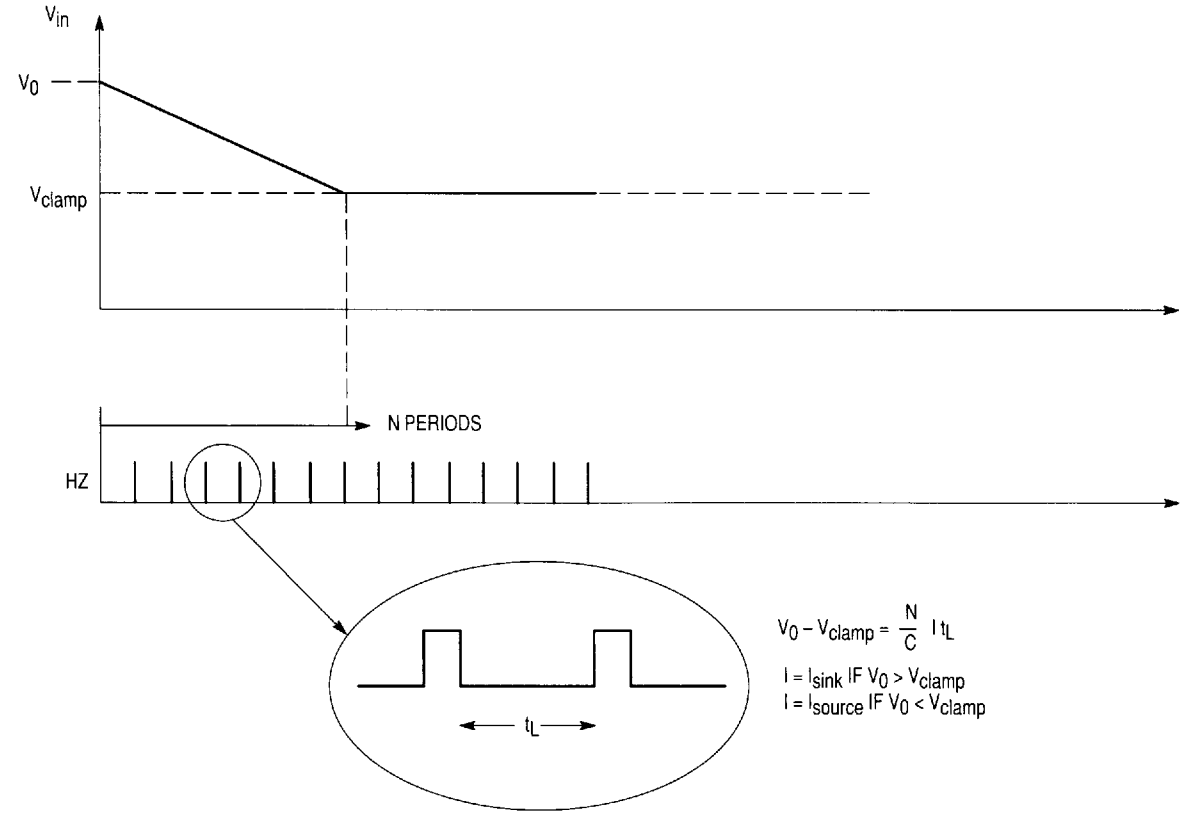



**Figure 4. Clamp Network Timing Diagram — Power Up**

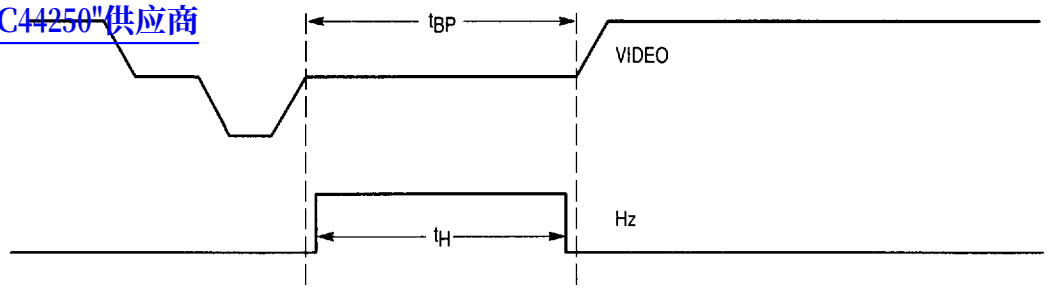



**Figure 5. Horizontal Timing**

## DITHERING

Dithering can be used to reduce the errors that are the result of the digitizing process used to convert video information between analog and digital forms. This method can also be applied to non–video signals. When converting analog signals to a digital format, errors can be introduced because of the limited number of discrete levels that the digital system imposes. For example, an 8–bit digital word can describe exactly 256 discrete analog levels. In some cases, this may not be sufficient for the application involved.

One solution is to increase the number of bits that describe the analog signal. The disadvantages of this approach are the increase in cost of the converter and the loss in speed associated with the increased number of bits. The addition of analog filters at the point where the digital information is converted back to analog is also possible, but this also has its limitations.

When a ramp voltage is generated from a digital source or an analog ramp is converted to a digital form and back to analog, the limited number of vertical samples causes the ramp to take the form of a "stair case" (see Figure 6). The severity of this distortion depends on the number of digital bits that generated the ramp. The "stair case" effect is less pronounced when the number of bits producing the ramp is increased.

When processing video information using a YUV form and a luminance ramp is displayed, granulation errors may become noticeable. This condition can also occur when one of the RGB signals is ramped and the other two are held constant. When processing video information using 24–bits or less, this "granulation" can be observed. Since the video is processed as three 8–bit signals, the maximum number of different luminance levels is reduced to 256. In cases where only a 7–bit luminance signal is used, the maximum number of luminance levels is reduced to 128. The uniform luminance ramp is observed on the display as vertical bars rather than a uniform luminance change.

The dithering technique consists of adding a small offset to the input signal. This offset (when it is equal to an integer number of LSB) is then subtracted from the digital output data. This offset is varied "line–to–line" by one half LSB steps. It allows each point of the waveform to be interpolated to higher precision by averaging the differential linearity errors on the screen.

The addition of the small offset forces the comparators to sample at a slightly different point on the input waveform (see Figure 7). When translated to the display, the effect is to shift this value slightly to the left. Overall accuracy of the display is maintained by subtracting this value from the output when the shift is equal to an integer number of LSB. For a uniform and continuous video waveform, the result of incrementing and decrementing the dither voltage is to effectively double the luminance levels from 256 to 512. The effect is to broaden the luminance range. This results in a more pleasing display with less visible quantization.

The dithering pattern is generated by means of a binary counter, which is incremented for every line by input HZ, and reset by every second vertical input VTN; thus, the dithering pattern is synchronized to the deflection of the screen. The effect of the dithering pattern is given in Figure 8. Subsequent subtraction of the introduced dithering signal at the output of each ADC is performed by a binary adder. The dithering function is suppressed when input VTN is low.

Depending on the position of the counter, the minimum output code may be $00 or $01 and the maximum output code may be $FE or $FF.

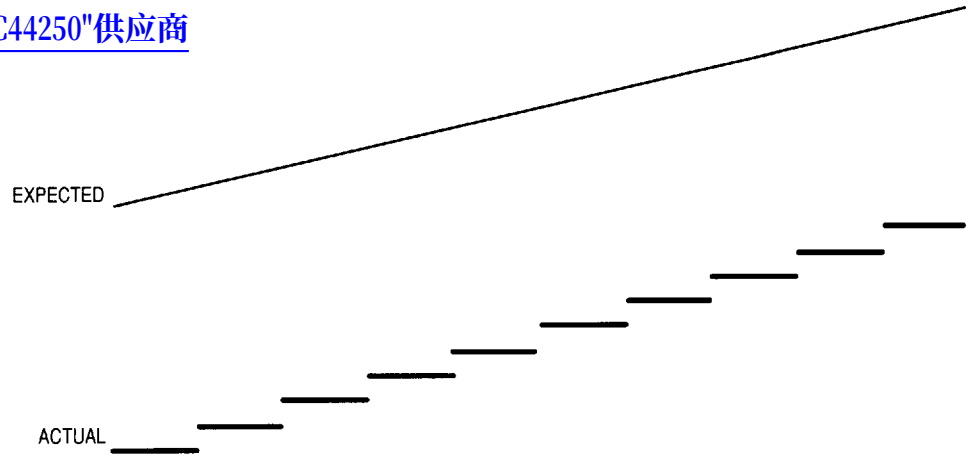



**Figure 6. Distortion Produced By Digitizing**

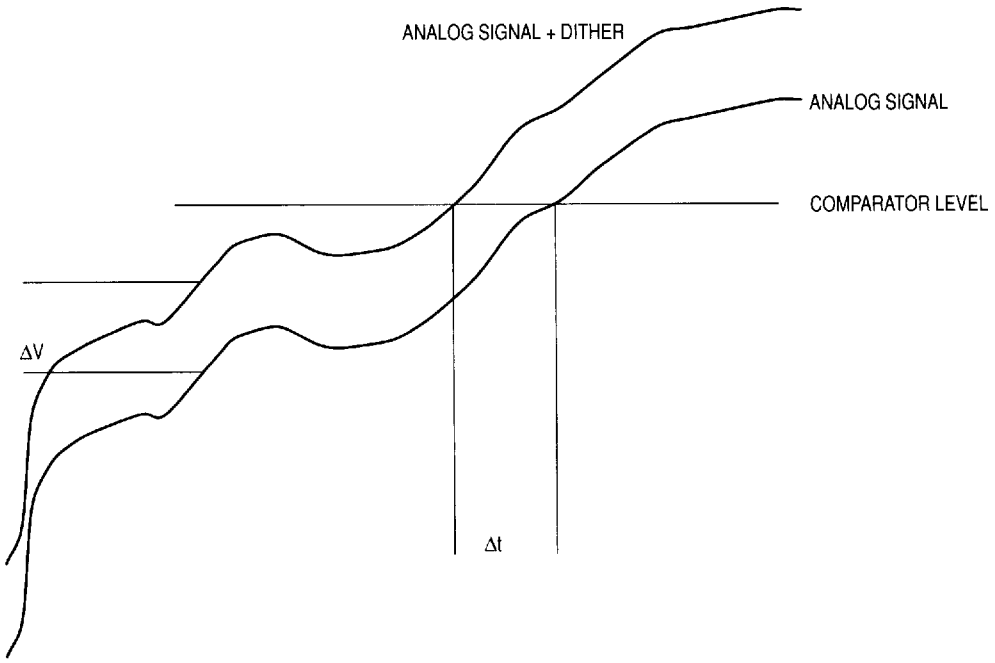



**Figure 7. Amplitude Dithering**

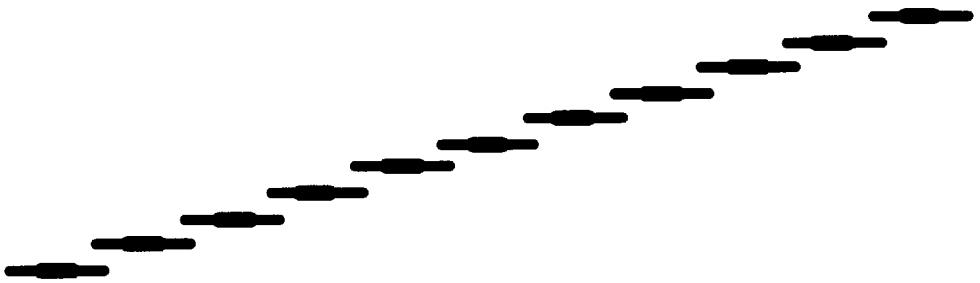


**Figure 8. Effect of Dithering Pattern**

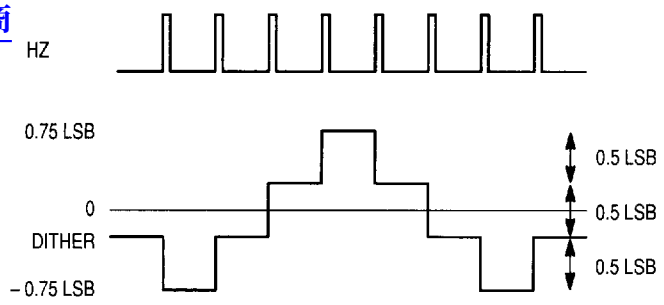



**Figure 9. Dithering Sequence**

## RESTRICTIONS ON $V_{DD(R)}$

The normal operating condition for the MC44250 is defined as $V_{DD(R)} = V_{DD(A)} = V_{DD(D)}$ and the safe operating range of $V_{DD(R)}$ is defined as $0 \le V_{DD(R)} \le V_{DD}$. In cases where $V_{DD(R)}$ is operated at values other than $V_{DD}$, it should be noted that the accuracy of the conversion process is reduced. In all cases $V_{DD(R)}$ should not be allowed to exceed $V_{DD}$.

The step size is defined as SS(n) and the ideal step size is defined as SSI. We may define an error component, $\partial$, as the difference between the actual step size and the ideal step size so that

$$\partial = |SSI - SS(n)|.$$

We may also define a worst case value for $\partial$ as

$$\partial \le \partial w$$

where $\partial w$ is the greatest value of $\partial$. The origin of this error is the offset mismatch from one comparator to another and is nearly independent of $V_{DD(R)}$ and $V_{DD}$.

Since $\partial$ is nearly independent of $V_{DD(R)}$, its value will remain constant for all values of $V_{DD(R)}$.

The step size error, SSE, is defined as

$$SSE(n) = (SSI - SS(n))/SSI = \partial(n)/SSI.$$

Furthermore, the ideal step size SSI is defined as

$$SSI = V_{DD(R)} \times 0.6/255.$$

Since $\partial$ is a constant and SSI is proportional to $V_{DD(R)}$, the step size error, SSE, will increase as $V_{DD(R)}$ is decreased. Further study will show that the differential nonlinearity, DNL, will also increase as $V_{DD(R)}$ is reduced. To minimize these errors it is desirable to keep $V_{DD(R)}$ as high as possible. Since the maximum value for $V_{DD(R)}$ is $V_{DD}$,

$$V_{DD(R)} = V_{DD(D)} = V_{DD(A)}$$

is the value that produces the greatest conversion accuracy.

## INPUT VOLTAGE RANGE

In applications where the input signals are dc coupled to the MC44250, the following restrictions apply:

If $V_{in} \le V_{min}$, then the output code = \$00 or \$01 (depending on the dither generator).

If $V_{in} \ge V_{max}$, then the output code = \$FE or \$FF (depending on the dither generator).

If $V_{min} \le V_{in} \le V_{max}$, then the output code reflects the correct value of the input voltage.

If the input is video based and ac coupled, then the input voltage range for $V_{in}$ without saturation is

$$0 \le V_{in} \le V_{range}.$$

For $V_{in}$ this reflects a maximum video input level before saturation of about 3 V for $V_{DD}$ = 5 V.

## DEFINITIONS



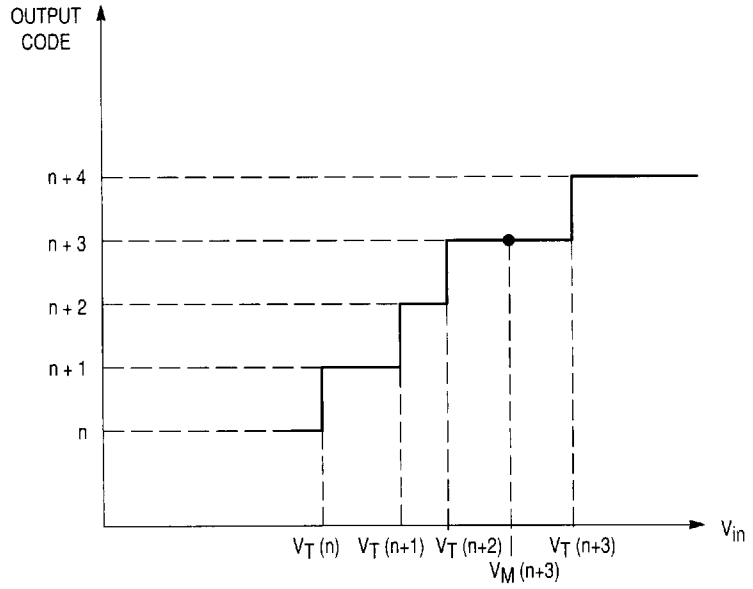



**Figure 10.**

- **Transition Voltage:** voltage at which transition from step n to step n+1 occurs = $V_T(n)$.

- **Step Size:** Difference between two consecutive transition voltages.

$$SS(n) = V_T(n) - V_T(n-1)$$

- **Mid–Point Voltage:**

$$V_M(n) = \frac{V_T(n) + V_T(n-1)}{2}$$

$$V_M(\text{max code}) = \frac{V_{DD(R)} + V_T(\text{max code} - 1)}{2}$$

- **Step Size Ideal:**

$$\frac{V_{range}}{255} = SSI$$

- **Differential Nonlinearity (DNL):**

$$DNL(n) = \frac{V_M(n+1) - V_M(n)}{SSI} - 1 \text{ in LSB}$$

- **Integral Nonlinearity ($I_{NL}$) and Offset:**

$$I_{NL}(n) = \frac{V_M(n) - a \bullet n - b}{SSI} \text{ in LSB}$$

Note: $I_{NL}$ (min code) and $I_{NL}$ (max code) is not defined.

- **Gain:** Gain = a in the formula Y = a • code + b
or the slope in the curve mid–points = f(code)

- **$V_{offset}$:** $V_{offset} = b - V_{min}$

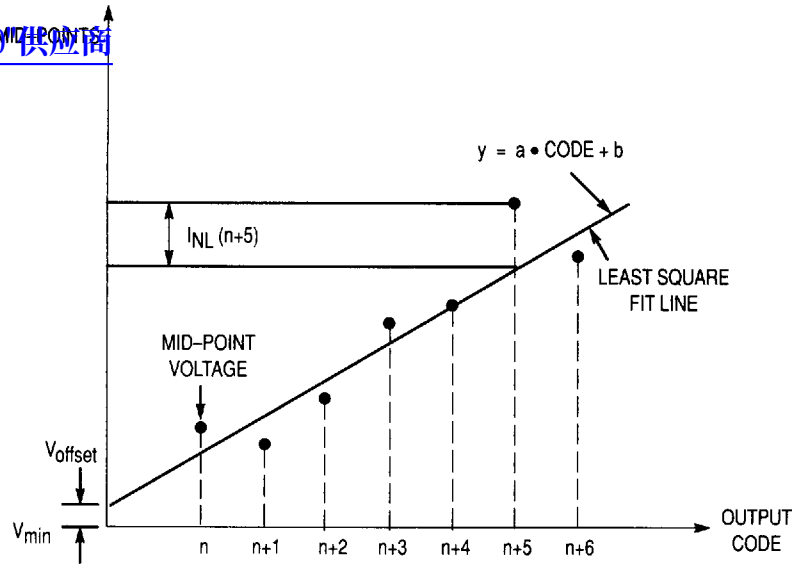
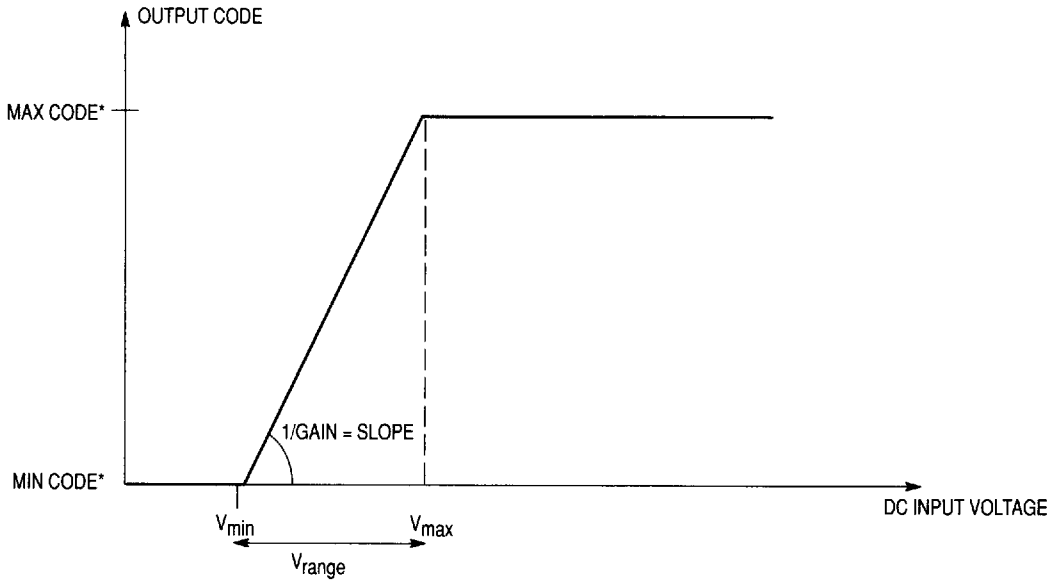



**Figure 11. Integral Nonlinearity and Offset**




*See dither generator.
LSB ideal = $V_{range}/255$
(Min code = 0 or 1; see dither generator)

**Figure 12.**

## PCB DESIGN

To maximize the performance of the MC44250, noise should be kept to a minimum. Good printed circuit board design will enhance the operation of the MC44250. Separate analog and digital grounds will reduce noise and conversion errors. In addition, separate filters on analog $V_{CC}$ and digital $V_{DD}$ will also help to minimize noise and conversion errors. Sufficient decoupling and short leads will also improve performance.

When designing mixed analog/digital printed circuit boards, separate ground planes for digital ground and analog ground should be employed. Large switching currents generated by digital circuits will be amplified by analog circuitry and can quickly make a circuit unusable. Care should be taken to ensure analog ground does not inadvertently become part of the digital ground. The analog and digital grounds should be connected together at only one point. This is usually at or near where power enters the printed circuit board. Additionally, when interconnecting several printed circuit boards together, care must be taken to ensure that cabling does not interconnect digital and analog grounds together to produce a path for digital switching currents through analog ground.

When using any device with the performance and speed of the MC44250, ground planes are essential. Loosely interconnected traces and/or random areas of ground strewn around the printed circuit board are inadequate for high performance circuitry. While distribution of $V_{DD}$ and $V_{CC}$ can be done by bussing, to do so with the ground system is disastrous.

An inch long conductor is an 18 nH inductor. The cross sectional area of the conductor affects the exact value of the inductance, but for most PCB traces this is approximately correct. If the ground system is composed of traces or clumps of ground loosely interconnected, it will be inductive. The amount of inductance will be proportional to the length of the conductors making up the ground. This inductance cannot be decoupled away. It must be designed out.

A CMOS device exhibits a characteristic input capacitance of about 10 pF. If this gate is driven by a digital signal that switches 2.5 V in a period of 5 ns, the equation for the average current flowing during the switching time will be:

$$I_{AV} = Cdv/dt.$$

A voltage change of 2.5 V in 5 ns requires an average current of 5 mA. If we assume a linear ramp starting from zero, the total change in current will be 10 mA. The change in current per nanosecond per gate can be found by dividing the change in current by the time

$$10\ mA/5\ ns = 2\ mA/ns.$$

For a device with 16 outputs driving one gate for each output,

$$di/dt = 16 \times 2\ mA/ns = 32\ mA/ns.$$

If the above 1–inch wire is in this current path, then the voltage dropped across it can be found from the formula

$$V = Ldi/dt = 18\ nH \times 32\ mA/ns = 0.576\ V.$$

If the inductor is in the ground system, it is in the signal path. The voltage generated by the switching currents through this inductor will be added to the signal. At best it will be superimposed on the analog signal as unwanted noise. At worst, it can render the entire circuit unusable. Even the digital signal path is not immune to this type of signal. It can false trigger clock circuits causing timing errors, confuse comparator type circuits, and cause digital signals to be misinterpreted as wrong values.

When laying out the PCB, use electrolytic capacitors of sufficient size at the power input to the printed circuit board. Adding low ESR decoupling capacitors of about 0.1 µF capacitance across $V_{CC}$ and/or $V_{DD}$ at each device will help reduce noise in general and ESD susceptibility. Implementation of a good ground plane ground system can all but eliminate the type of noise described above.

To summarize, use sufficient electrolytic capacitor filtering, make separate ground planes for analog ground and digital ground, tie these grounds together at one and only one point, keep the ground planes as continuous and unbroken as possible, use low ESR capacitors of about 0.1 µF capacitance on $V_{CC}$ and $V_{DD}$ at each device, and keep all leads as short as possible.

## EMI SUPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by ***all*** digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 13 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When

the relief pattern is equal to half the distance between pins, over-etching and process errors may remove ground between pins. If sufficient ground around enough pins is removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.



If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with adequate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 14. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 14. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4xfsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

## APPLICATIONS CIRCUIT

Figure 15 shows a typical applications circuit. This circuit will produce analog–to–digital conversion of either RGB information or YUV information by setting SW1. In the YUV mode, SW1 is set either to position '1' or to the open position depending on the desired clamp level (see Table 1). The RGB inputs then become YUV inputs and correspondingly, the RGB outputs are YUV. For RGB operation, SW1 is set to the '0' position.

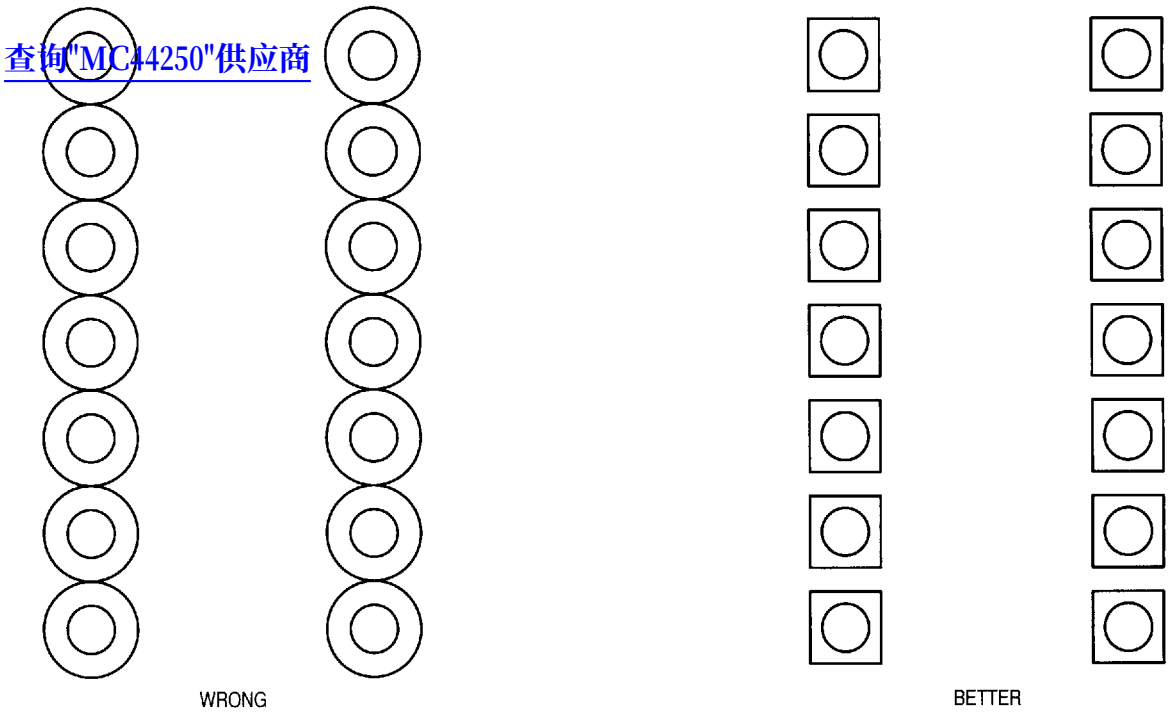



**Figure 13.**

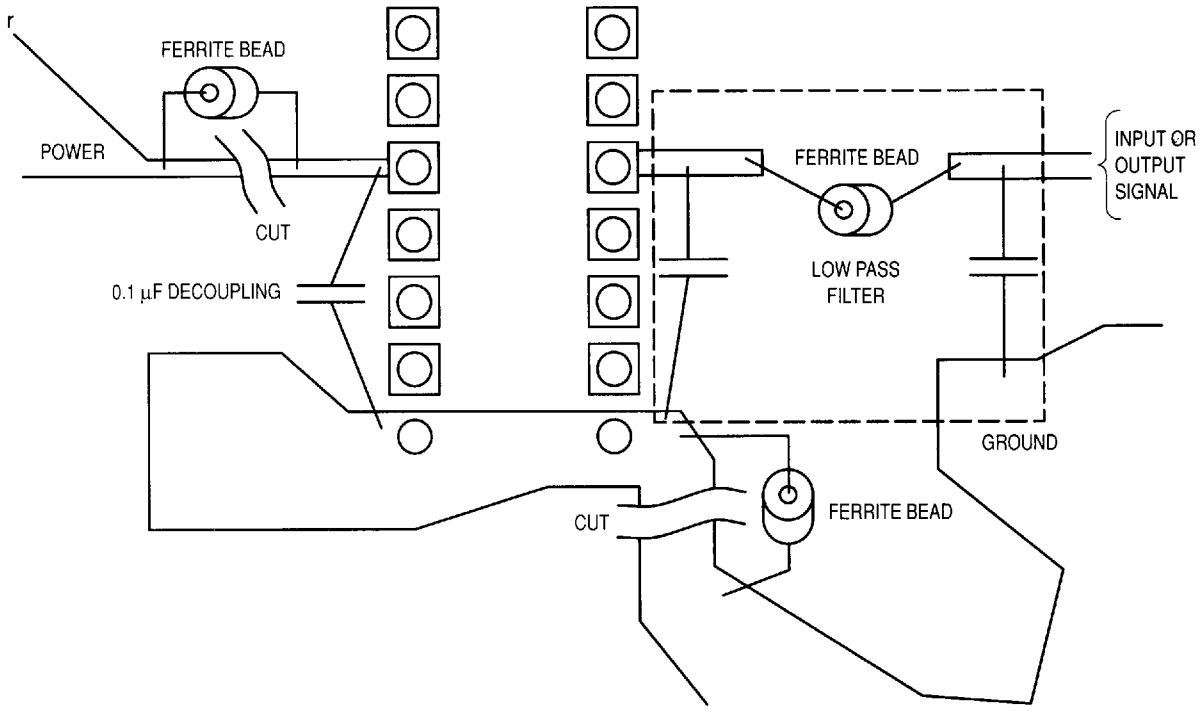



**Figure 14.**

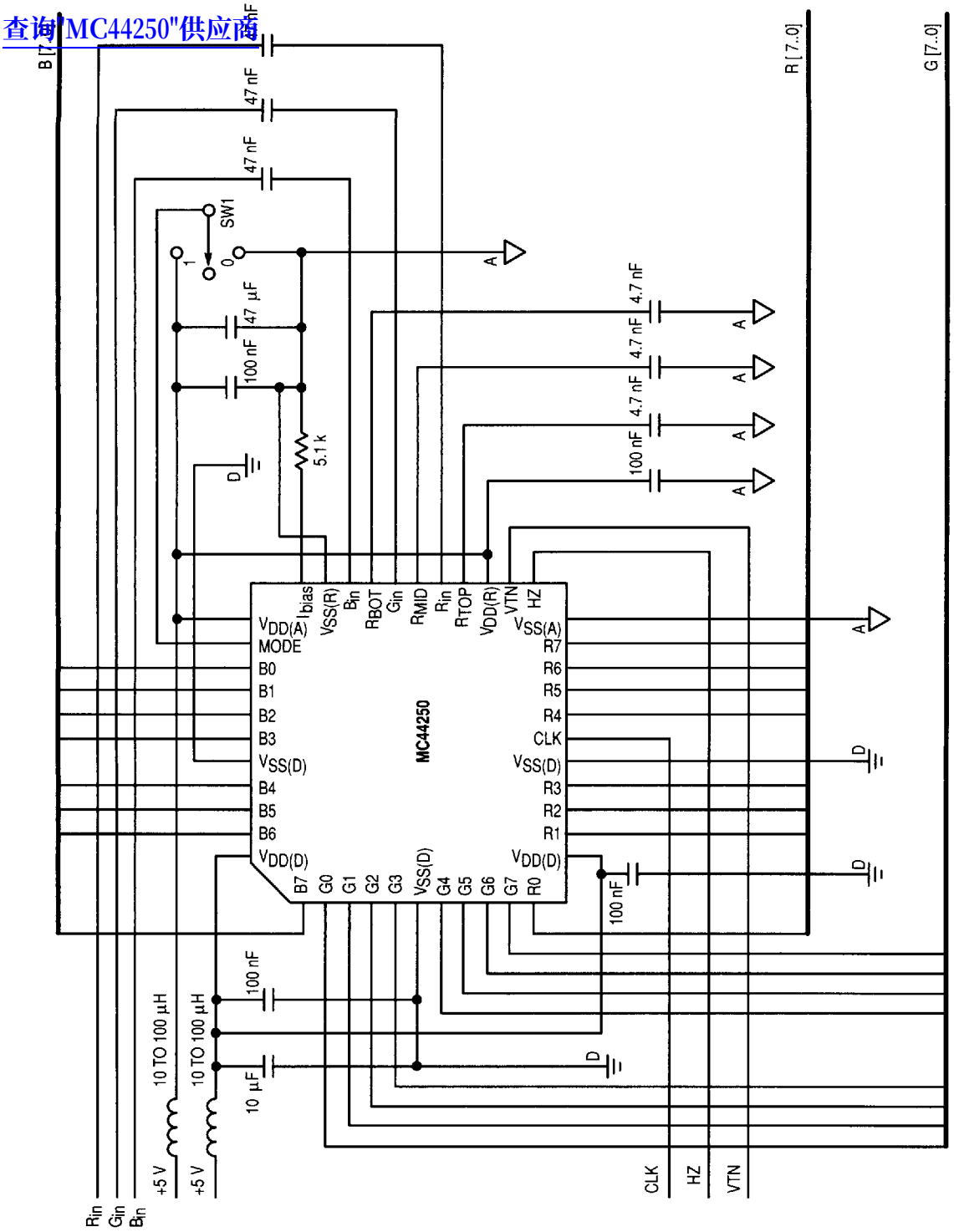
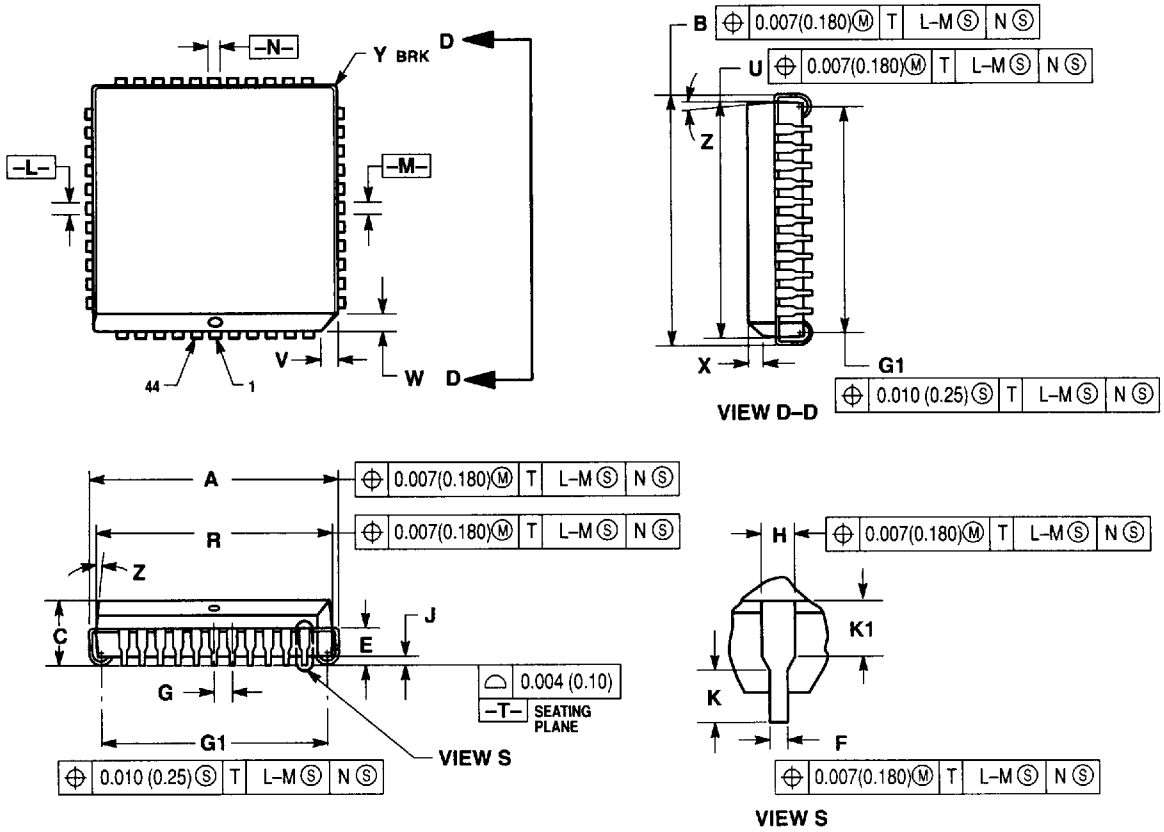



**Figure 15. Application Circuit**

## PACKAGE DIMENSIONS

**FN SUFFIX**
**PLCC**
**CASE 777**




NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.685 | 0.695 | 17.40 | 17.65 |
| B | 0.685 | 0.695 | 17.40 | 17.65 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.650 | 0.656 | 16.51 | 16.66 |
| U | 0.650 | 0.656 | 16.51 | 16.66 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.610 | 0.630 | 15.50 | 16.00 |
| K1 | 0.040 | — | 1.02 | — |