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REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-12-29

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, BIPOLAR, 12 X 48 X 8 FIELD PROGRAMMABLE LOGIC SEQUENCER (FPLS), MONOLITHIC SILICON

SIZE	CAGE CODE	5962-92012
A	67268	

SHEET 1 OF 23

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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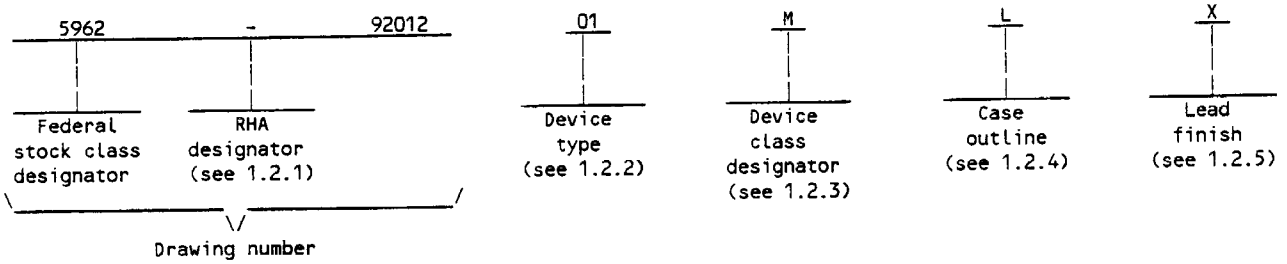
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PLS168	12 x 48 x 8 field programmable logic sequencer

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

Output voltage (V_O)	5.5 V dc
Supply voltage (V_{CC})	7.0 V dc
Input voltage (V_I)	10 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation 2/	900 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case L	See MIL-STD-1835
Junction temperature (T_J)	+200°C
Output sink current	100 mA
Input current (minimum)	-30 mA
Input current (maximum)	+30 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Must withstand the added PD due to short-circuit test; e.g., I_{OS}.
3/ When a QML source exists, a value shall be provided.

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BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. This is a fully characterized military detail specification and is suitable for qualification of device classes B and S to the requirements of MIL-M-38510. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table diagram shall be as specified on figure 2.

3.2.4 Logic diagram. The block or logic diagram shall be as specified on figure 3.

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3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

3.12 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.12.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1c and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.12.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device types	Group A Subgroups	Limits		Units
						Min	Max	
Low level input voltage	V_{IL}	V_{CC} = 4.5 V		All	1,2,3		0.8	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V		All	1,2,3	2		V
Input clamp voltage 2/	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA		All	1,2,3		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V		All	1,2,3		-150	µA
Low level input current (CLK input)	I_{IL}	V_{CC} = 5.5 V, V_I = 0.45 V		All	1,2,3		-350	µA
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 5.5 V		All	1,2,3		50	µA
Low level output voltage 3/	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OL} = 9.6 mA		All	1,2,3		0.5	V
High level output voltage 4/	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2 V, I_{OH} = -2 mA		All	1,2,3	2.4		V
Output short-circuit current 2/ 5/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V		All	1,2,3	-15	-85	mA
DC supply current 6/	I_{CC}	V_{CC} = 5.5 V		All	1,2,3		185	mA
Three-state output current 7/	I_{OZ}	V_{CC} = 5.5 V	V_{OUT} = 5.5 V	All	1,2,3		60	µA
			V_{OUT} = 0.45	All	1,2,3		-60	µA
Functional tests		See 4.4.1d		All	7,8			
Frequency (w/o C-array)	f_{max}	V_{CC} = 5.0 V ±10% R_1 = 470Ω, R_2 = 1 kΩ, C_L = 50 pF See figures 4 and 5		All	9,10,11		10.5	MHz
Propagation delay: Clock	t_{CKO}			All	9,10,11		35	ns
Output enable	t_{OE1}	To prevent spurious clocking, clock rise time (10%-90%) ≤ 30 ns		All	9,10,11		40	ns
Output disable	t_{OD1}			All	9,10,11		40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

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Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device types	Group A Subgroups	Limits		Units
					Min	Max	
Preset/reset	t_{PRO}	V_{CC} = 5.0 V ±10% R_1 = 470Ω, R_2 = 1 kΩ, C_L = 50 pF See figures 4 and 5 To prevent spurious clocking, clock rise time (10%-90%) ≤ 30 ns	All	9,10,11		45	ns
Power-on preset	t_{PPR}		All	9,10,11		20	ns
Pulse width: Clock high	t_{CKH}		All	9,10,11	40		ns
Clock low	t_{CKL}		All	9,10,11	40		ns
Period (w/o C-array)	t_{CKP1}		All	9,10,11	95		ns
Preset/reset pulse	t_{PRH}		All	9,10,11	40		ns
Setup time: Input	t_{IS1}		All	9,10,11	60		ns
Input (through complement array) 8/	t_{IS2}		All	9,10,11	100		ns

1/ All voltage values are with respect to ground.

2/ Test one at a time.

3/ Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ output sink current is applied through a resistor to V_{CC}.

4/ Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.

5/ Duration of short circuit should not exceed 1 second.

6/ I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5 V, and the outputs open.

7/ Measured with V_{IH} applied to PR/$\overline{OE}$.

8/ Not testable on unprogrammed devices.

4. QUALITY ASSURANCE PROVISIONS

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4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as 3.1.9 through 3.1.13 (preburn-in electrical parameters through interim postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the burn-in test circuit shall be submitted to DESC-EC for review with the certificate of compliance. For device classes B and S, the burn-in test circuit shall be submitted to the qualifying activity.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220 Ω to 47 kΩ. For static II burn-in, reverse all input connections (i.e., V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D) using the circuit submitted (see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

d. For classes S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

e. All devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include as a minimum, the final electrical tests as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-EC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

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c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device class B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die) to other device types on this specification, the slower device types may be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5 herein).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5 herein). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than four total device failures allowable.

Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

d. For device classes M, B, and S, subgroups 7 and 8 testing shall be sufficient to verify the functional operation of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

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4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1b herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. For device class M, the test circuit shall be submitted to DESC-EC for review with the certificate of compliance. For device class B, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-EC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. For group D inspection end-point electrical parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 1,2,8A,10	1,7,9 or 1,2,8A,10	1,7,9 or 1,2,8A,10	1,7,9 or 1,2,8A,10
2	Static burn-in I and II method 1015	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7*		1*,7*
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1		1
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10 11	1*,2,3,7*, 8A,8B,9,10 11	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3,7*, 8A,8B,9,10 11	1*,2,3, 7*,8A,8B, 9,10,11
7	Group A test requirements	1,2,3,7, 8A,8B,9, 10,11	1,2,3,7, 7,8A,8B,9, 10,11	1,2,3,7, 7,8A,8B,9 10,11	1,2,3,7, 8A,8B,9, 10,11	1,2,3,7, 7,8A,8B,9 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B		1,2,3,7, 8A,8B	1,2,3, 7,8A,8B,9, 10,11
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ * indicates PDA applies to subgroup 1 and 7.
4/ Subgroups 7 and 8 functional tests shall verify the truth table.
5/ Subgroups 10 and 11, if not tested shall be guaranteed to the limits specified in table I.

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TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

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Device type	01
Case outline	L
Terminal number	Terminal symbol
1	CK
2	I_5
3	I_4
4	I_3
5	I_2
6	I_1
7	I_0
8	F_0
9	F_1
10	F_2/P_4
11	F_3/P_5
12	GND
13	P_0/P_6
14	P_1/P_7
15	P_2/P_8
16	P_3/P_9
17	$PR/\overline{OE}$
18	I_{11}
19	I_{10}
20	I_9
21	I_8
22	I_7
23	I_6
24	V_{CC}

FIGURE 1. Terminal connections.

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V_{CC}	OPTION PR	OPTION $\overline{OE}$	D	CK	S	R	$Q_{P/F}$	F
+5V	H		•	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(\overline{Q})_n$
	L		X	X	X	X	Q_n	$(\overline{Q})_n$
		H	•	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(\overline{Q})_n$
		L	X	X	X	X	Q_n	$(\overline{Q})_n$
		L	X	↑	L	L	Q_n	$(\overline{Q})_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND	IND
↑	X	X	X	X	X	X	H	

NOTES:
1. Positive logic:
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$.
2. Either preset (active-HIGH) or $\overline{\text{OUTPUT ENABLE}}$ (active-LOW) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from LOW to HIGH level.
4. R = S = HIGH is an illegal input condition.
5. • = H/L/+10 V.
6. X = don't care (≤ 5.5 V).

FIGURE 2. Truth table.

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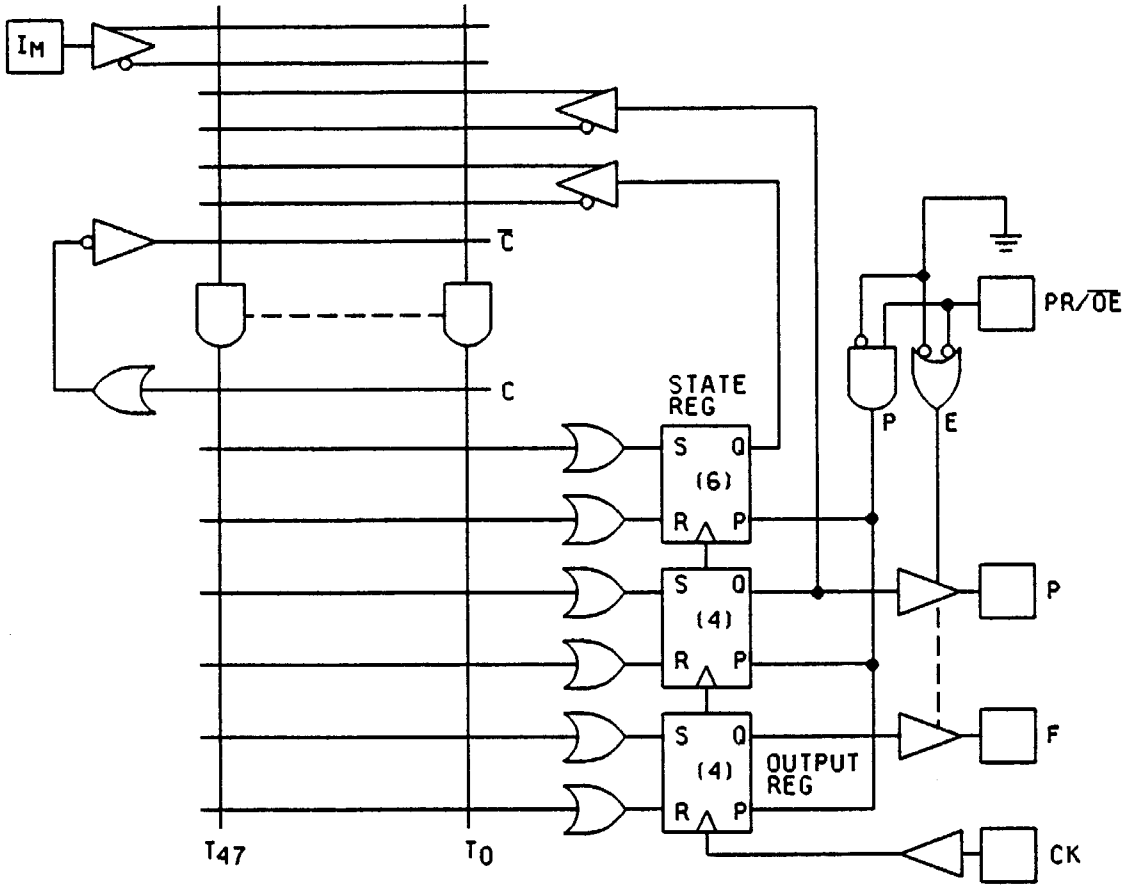

FIGURE 3. Logic diagram.

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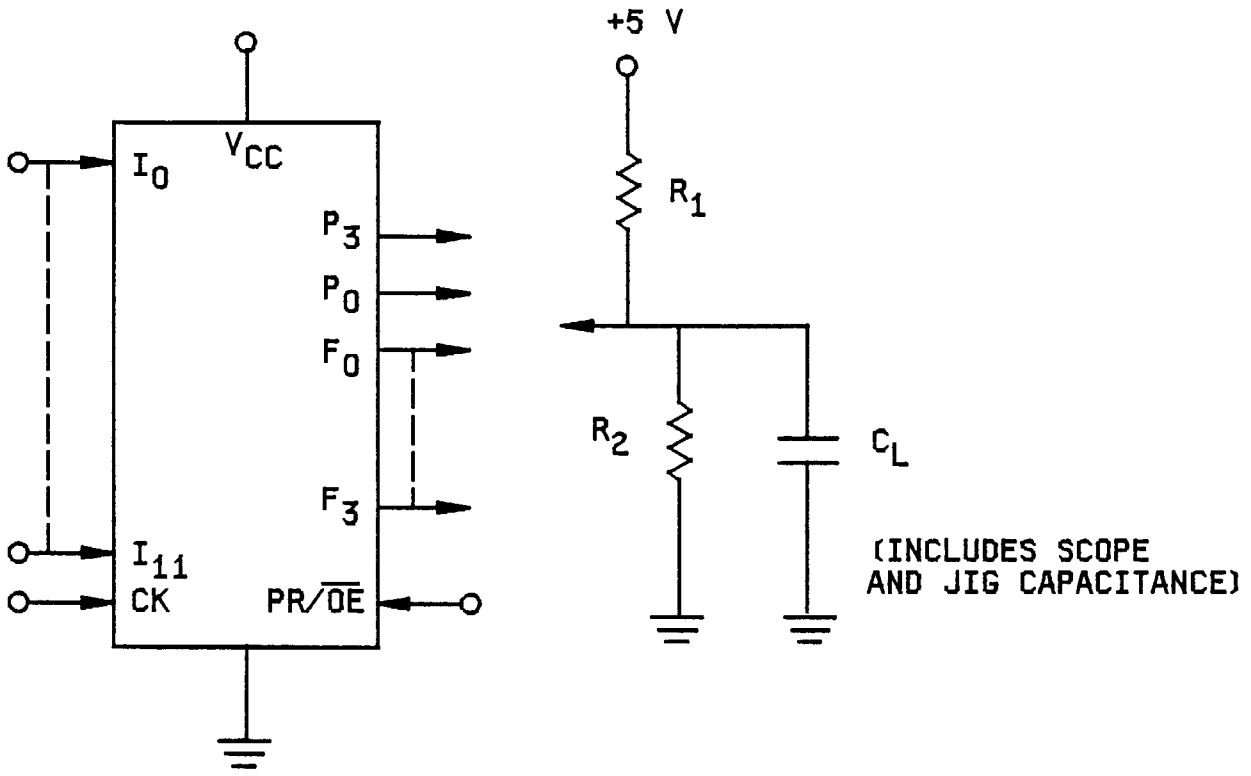

NOTE: R_1 = 470Ω, R_2 = 1 kΩ, and C_L = 50 pF.

FIGURE 4. Test load circuit.

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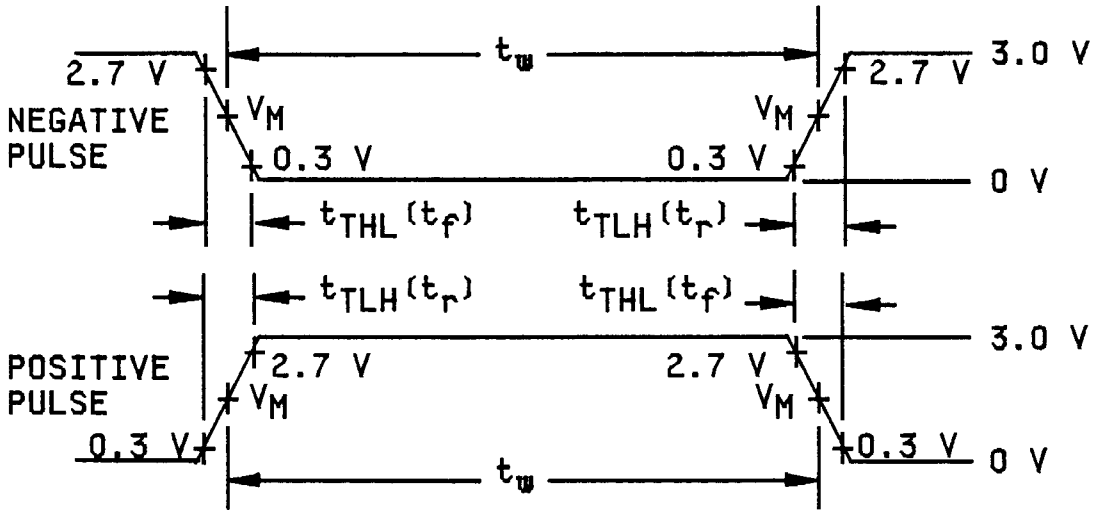
VOLTAGE WAVEFORMS



INPUT PULSE DEFINITIONS

Input pulse characteristics				
V_M	Rep. rate	Pulse width	t_{TLH}	t_{THL}
1.5 V	1 MHz	500 ns	≤ 5 ns	≤ 5 ns

FIGURE 5. Timing waveforms.

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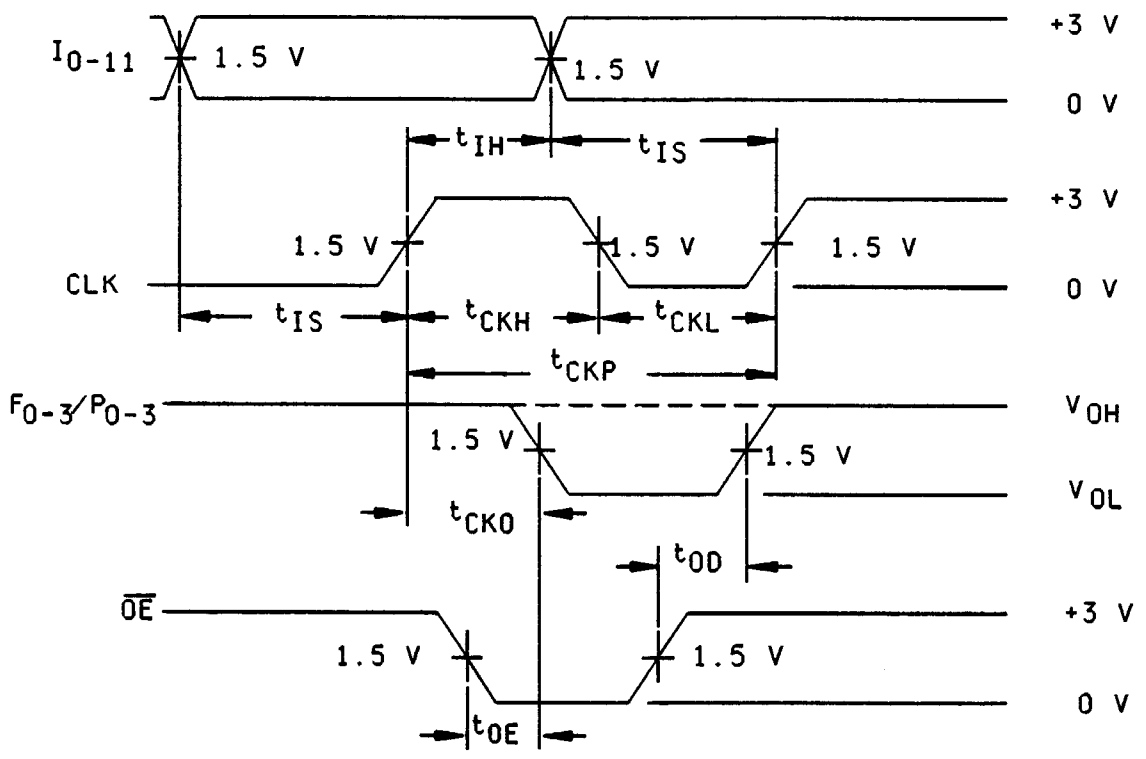

FIGURE 5. Timing waveforms - Continued.

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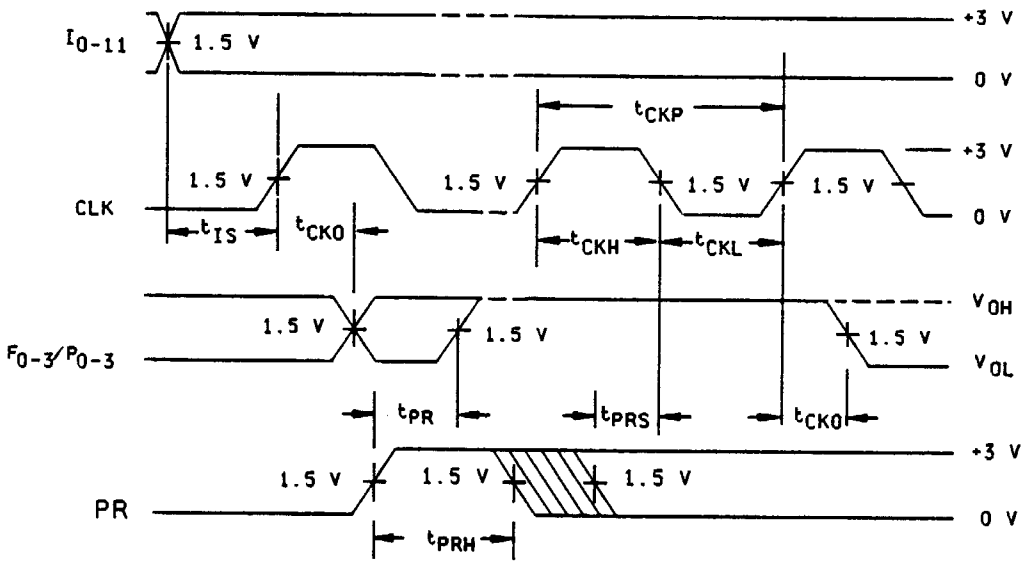

FIGURE 5. Timing waveforms - Continued.

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POWER-ON PRESET

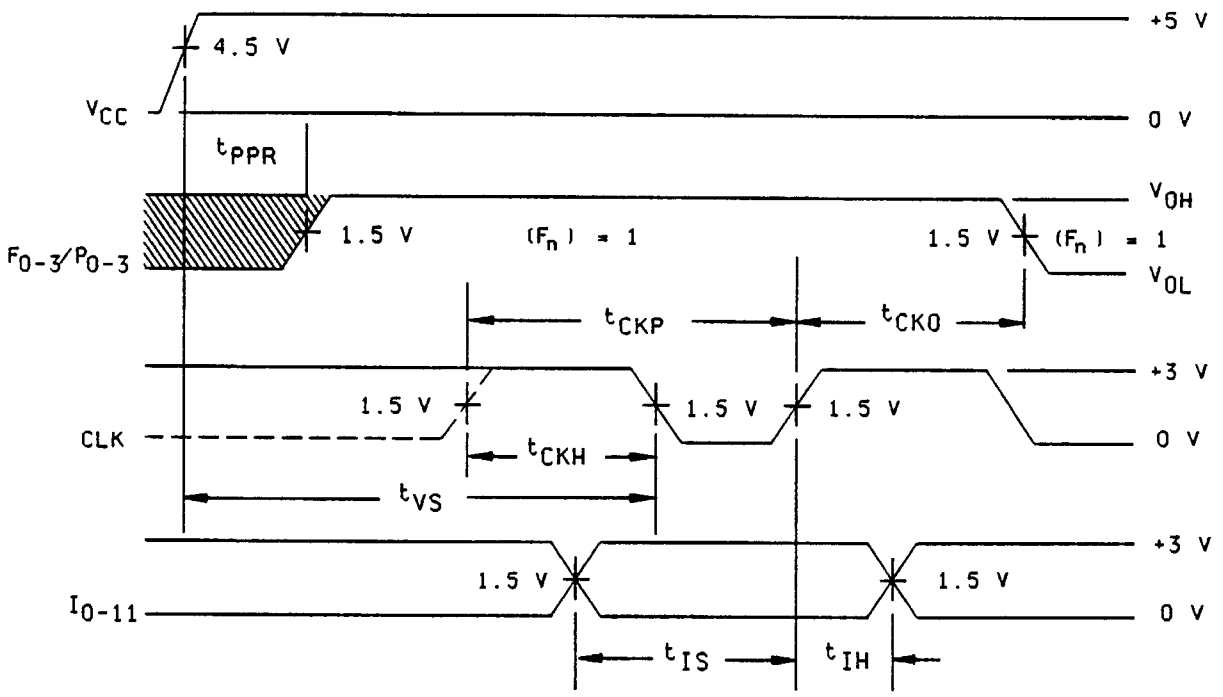

FIGURE 5. Timing waveforms - Continued.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured. The RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document or to a higher qualified level. RHA tests for device classes Q and V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B, S, Q, and V for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IA herein. RHA samples need not be tested at -55°C or +125°C prior to total dose irradiation.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. The samples shall pass the specified group A electrical parameters for subgroups specified in table IIA herein. Additionally classes Q and V, for quality conformance inspection may be at wafer level.

d. The devices shall be subjected to radiation hardness assurance tests as specified in MIL-M-38510, (device classes M, B, and S) and MIL-I-38535, (device classes Q and V) for the RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure.

e. Prior to and during, total dose irradiation, the devices shall be biased to the worst case conditions established during characterization.

f. SEP testing shall be performed on all class S and V devices. SEP testing shall be performed at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics of the device. Test four devices with zero failures. ASTM standard F1192-88 may be used as a guideline when performing SEP testing. For device class V, the device parametrics that influence single event upset immunity shall be monitored at the wafer level as part of a TRB approved wafer level hardness plan. The test conditions for SEP are as follows:

(1) The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e., 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

(2) The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm^2.

(3) The flux shall be between 10^2 and 10^5 ion/cm^2/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.

(4) The particle range shall be ≥ 20 microns in silicon.

(5) The test temperatures shall be +25°C and also the maximum rated operating temperature ±10°C.

(6) Bias conditions shall be V_{CC} = 4.5 V dc for the upset measurements and V_{CC} = 5.5 V dc for the latch-up measurements.

(7) For SEP test limits, see table IB herein.

g. For device classes M, B, and S subgroups 1 and 2 of table V method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

h. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

i. Transient dose rate survivability testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-I-38535. Device parametric parameters that influence latch-up and device burn-out shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-I-38535.

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(a) When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

(1) RHA delta limits.

(2) RHA upset levels.

(3) Test conditions (SEP).

(4) Number of upsets (SEP).

(5) Number of transients.

(6) Occurrence of latch-up.

4.5 Programming procedures. Programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

C_{IN} C_{OUT}	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{IL}	Input current low
I_{IH}	Input current high
T_C	Case temperature.
T_A	Ambient temperature
V_{CC}	Positive supply voltage.
V_{IC}	Positive input clamp voltage
O/V	Latch-up over-voltage
O/I	Latch-up over-current

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between the various generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

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DATE: 92-12-29

Approved sources of supply for SMD 5962-92012 are listed below for immediate procurement only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/
5962-9201201MLX	18324	PLS168/BLA

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Fusible line
18324	Signetics Corporation 811 East Arques Ave. Sunnyvale, CA 94088-3409	Ni-chrome

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.