

OVERVIEW

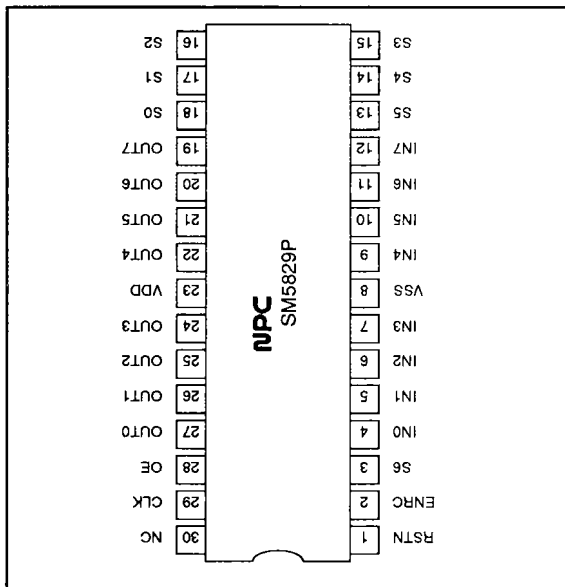
The SM5829P is a variable-length shift register fabricated in Molybdenum-gate CMOS. The length can be set to any value between 2 and 129.

The SM5829P features a maximum operating frequency of 25.0 MHz (2 to 65 steps) and 33.3 MHz (66 to 129 steps), and static registers for data retention during periods when the shift clock is halted, making it ideal for digital video processing and similar applications.

FEATURES

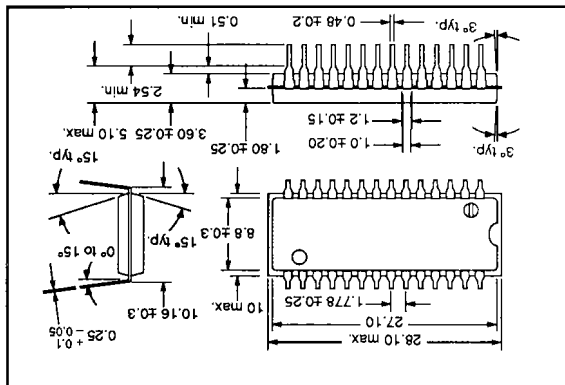
- 2- to 129-step selectable length
- 8-bit (1-byte) parallel input/output
- Uses static registers
- 33.3 MHz (max) operating frequency (66 to 129 steps) and 25.0 MHz (max) operating frequency (2 to 65 steps)
- Shift rotate/non-rotate select function
- Data reset function
- TTL-compatible input/outputs
- 5 $\pm$ 0.25 V power supply
- 30-pin shrink DIP
- Molybdenum-gate CMOS process

PINOUT



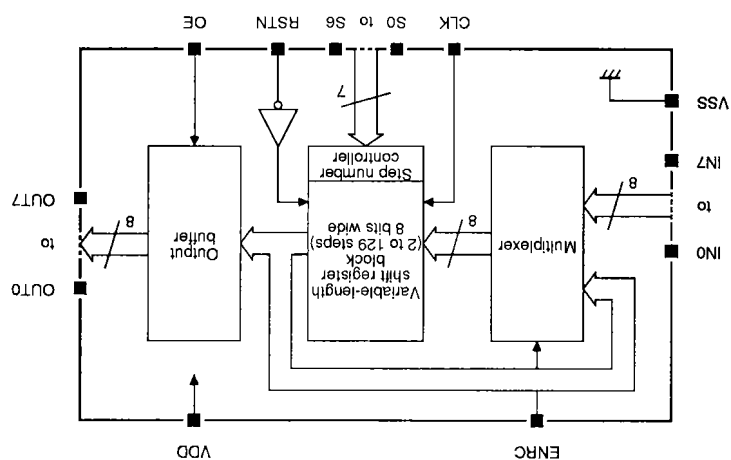
PACKAGE DIMENSIONS

Unit: mm



Number	Name	I/O	Description
1	RSTN	I	Data reset
2	ENRC	I	Data rotation control
3	S6	I	Register step select bit 6 (MSB)
4	IN0	I	Data input bit 0 (LSB)
5	IN1	I	Data input bit 1
6	IN2	I	Data input bit 2
7	IN3	I	Data input bit 3
8	VSS		Ground (0 V)
9	IN4	I	Data input bit 4
10	IN5	I	Data input bit 5
11	IN6	I	Data input bit 6
12	IN7	I	Data input bit 7
13	S5	I	Register step select bit 5
14	S4	I	Register step select bit 4
15	S3	I	Register step select bit 3
16	S2	I	Register step select bit 2
17	S1	I	Register step select bit 1
18	S0	I	Register step select bit 0 (LSB)
19	OUT7	O	Data output bit 7
20	OUT6	O	Data output bit 6
21	OUT5	O	Data output bit 5
22	OUT4	O	Data output bit 4
23	VDD		5 V (typ) supply
24	OUT3	O	Data output bit 3

BLOCK DIAGRAM



Number	Name	I/O	Description
25	OUT2	O	Data output bit 2
26	OUT1	O	Data output bit 1
27	OUT0	O	Data output bit 0 (LSB)
28	OE	I	Output enable
29	CLK	I	Clock input
30	NC		No connection

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V _{DD}	−0.3 to 7.0	V
Input voltage range	V _{IN}	−0.3 to V _{DD} + 0.3	V
Power dissipation	P _D	750	mW
Storage temperature range	T _{stg}	−40 to 125	deg. C
Soldering temperature	T _{sd}	255	deg. C
Soldering time	t _{sd}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V _{DD}	4.75 to 5.25	V
Operating temperature range	T _{op}	−20 to 70	deg. C

DC Electrical Characteristics

T_a = −20 to 70 deg. C, V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby supply current	I _{ST}	V _{DD} = 5.25 V	−	1	100	μA
Operating current consumption	I _{DD}	f _{CLK} = 33.3 MHz, V _{IH} = 2.4 V, V _{IL} = 0.5 V, V _{OE} = 0 V, V _{DD} = 5 V	−	−	110	mA
IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE HIGH-level input voltage	V _{IH}	See note 1.	2.4	−	−	V
IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE LOW-level input voltage	V _{IL}	See note 1.	−	−	0.5	V
OUT0 to OUT7 HIGH-level output voltage	V _{OH}	I _{OH} = −0.4 mA, See note 2.	2.5	−	−	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
OUT0 to OUT7 LOW-level output voltage	V _{OL}	I _{OL} = 1.6 mA. See note 2.	—	—	0.4	V
IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE input current	I _{IL}	V _{IN} = 0 V. See note 1.	—	10	20	μA
IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE input leakage current	I _{IH}	V _{IN} = V _{DD} . See note 1.	—	—	1	μA
OUT0 to OUT7 high-impedance output HIGH-level leakage current	I _{ZH}	V _{OUT} = V _{DD} . See note 2.	—	—	5	μA
OUT0 to OUT7 high-impedance output LOW-level leakage current	I _{ZL}	V _{OUT} = 0 V. See note 2.	—	—	5	μA

Notes

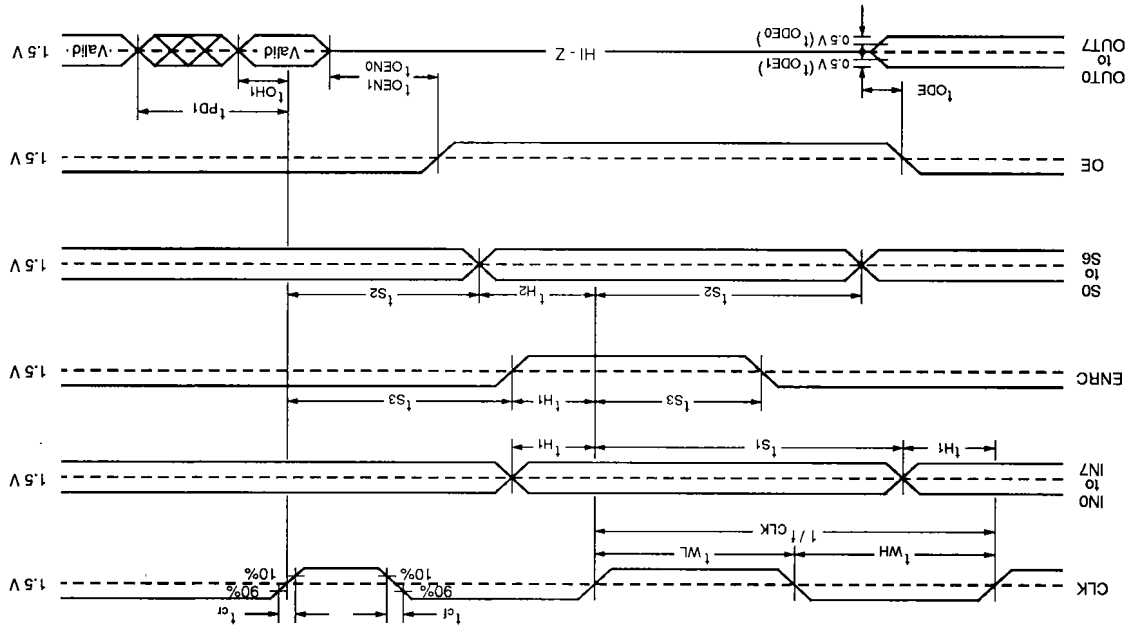
1. Pins IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE are inputs with internal pull-up resistances.
2. Pins OUT0 to OUT7 are tristate outputs.

AC Electrical Characteristics

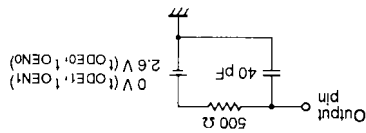
T_a = -20 to 70 deg. C, V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency (2 to 65 steps)	f _{CLK}	V _{IH} = 2.4 V, V _{IL} = 0.5 V	—	—	25.0	MHz
Clock frequency (66 to 129 steps)	f _{CLK}	V _{IH} = 2.4 V, V _{IL} = 0.5 V	—	—	33.3	MHz
Clock rise time	t _r		—	—	100	ns
Clock fall time	t _f		—	—	100	ns
Clock HIGH-level pulsewidth	t _{WH}		13	—	—	ns
Clock LOW-level pulsewidth	t _{WL}		13	—	—	ns
IN0 to IN7 input setup time	t _{S1}		13	—	—	ns
S0 to S6 input setup time	t _{S2}		50	—	—	ns
ENRC input setup time	t _{S3}		20	—	—	ns
IN0 to IN7 and ENRC input hold time	t _{H1}		0	—	—	ns
S0 to S6 input hold time	t _{H2}		5	—	—	ns
OE to OUT _n output enable delay time	t _{OEN0, 1}	See note 4.	—	—	25	ns
OE to OUT _n output disable delay time	t _{ODE0, 1}	See note 4.	—	—	25	ns
CLK to OUT _n output data hold time	t _{OH1}	See note 3.	10	—	—	ns
RSTN to OUT _n output data hold time	t _{OH2}	See note 3.	10	—	—	ns
CLK to OUT _n output data propagation delay time	t _{PD1}	See note 3.	—	—	28	ns
RSTN to OUT _n output data propagation delay time	t _{PD2}	See note 3.	—	—	28	ns

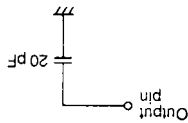
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Timing Diagrams



4. Measurement circuit 2



3. Measurement circuit 1

1. Pins IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE are inputs with internal pull-up resistances.
2. Pins OUT0 to OUT7 are tristate outputs.
3. Measurement circuit 1
4. Measurement circuit 2

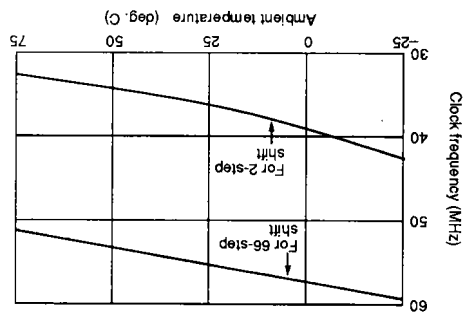
Notes

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
IN0 to IN7, S0 to S6, ENRC, CLK, RSTN and OE input capacitance	C _{IN}	f = 1 MHz	—	—	10	pF
OUT0 to OUT7 output capacitance	C _{OUT}	f = 1 MHz, V _{OE} = 0 V	—	—	20	pF

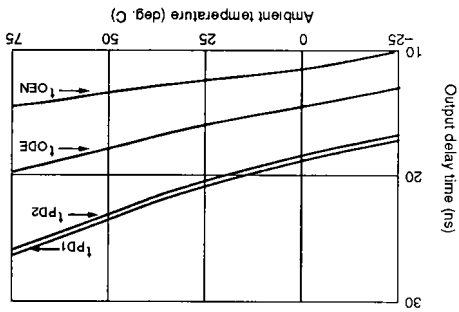
Typical Performance Characteristics

Typical values at $V_{DD} = 5.0\text{ V}$

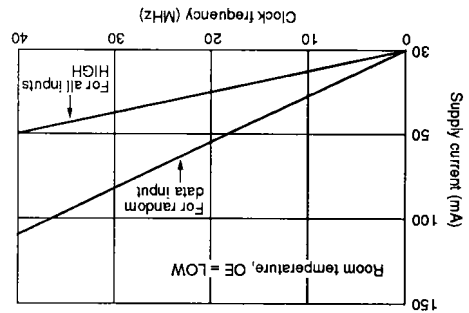
Maximum clock frequency vs. ambient temperature



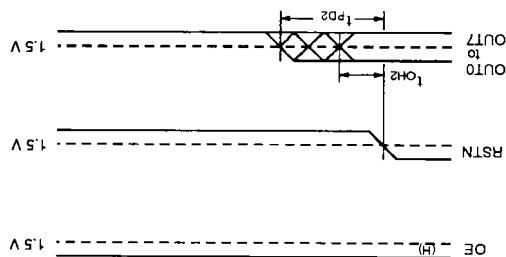
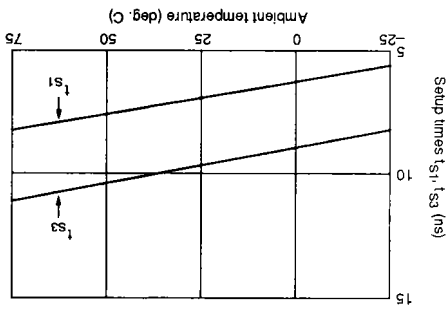
Output delay time vs. ambient temperature



Operating supply current vs. clock frequency

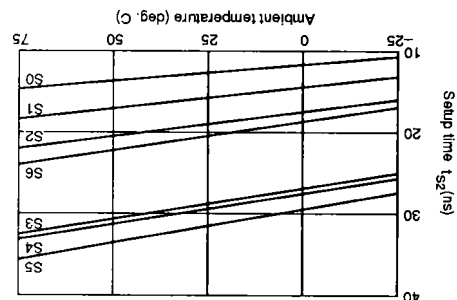


Minimum setup time vs. ambient temperature



Minimum setup time vs. ambient temperature 2

2. t_{s2} varies with the length of the shift register. All values are measured under worst conditions.
- a. All step select inputs are LOW except the one being measured.
- b. The value of t_{s2} of the measured step select input may be less than the value shown if any other step select input is HIGH, except for S0 which is not affected by other step select inputs.



Notes

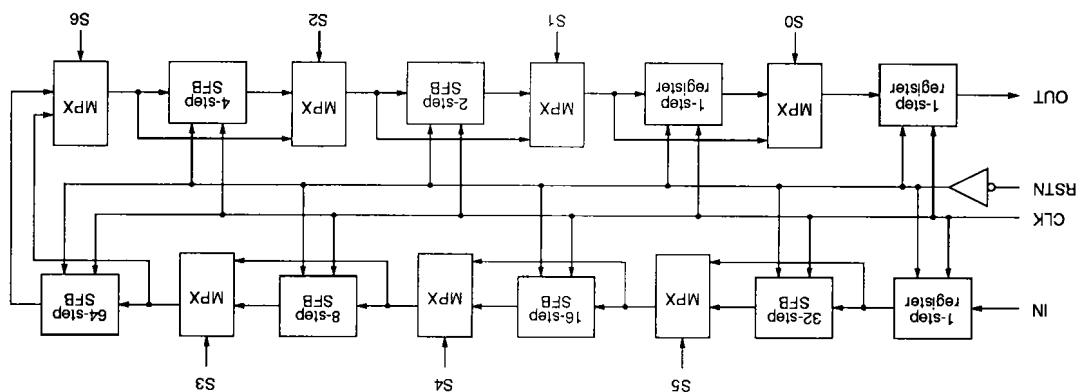
1. t_{s1} and t_{s3} do not vary with the length of the shift register.

FUNCTIONAL DESCRIPTION

Register Step Selection

Register operation

The internal structure of the shift register is shown in the following figure. Inputs S0 to S6 select or bypass the outputs of their corresponding shift register blocks. Combinations of S0 to S6 thus select the shift register length of between 2 and 129. Note that the first and last registers are always enabled.



Register length select

The S0 to S6 inputs select the register length. The length is given by the decimal value (S6 is MSB) plus 2.

$$\text{Length} = 64 \cdot (S6) + 32 \cdot (S5) + 16 \cdot (S4) + 8 \cdot (S3) + 4 \cdot (S2) + 2 \cdot (S1) + (S0) + 2$$

Step number	S6	S5	S4	S3	S2	S1	S0
126	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LOW
127	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH
128	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW
129	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

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Step number	S6	S5	S4	S3	S2	S1	S0
67	HIGH	LOW	LOW	LOW	LOW	LOW	HIGH
66	HIGH	LOW	LOW	LOW	LOW	LOW	LOW
65	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
4	LOW	LOW	LOW	LOW	LOW	HIGH	LOW
3	LOW	LOW	LOW	LOW	LOW	LOW	HIGH
2	LOW	LOW	LOW	LOW	LOW	LOW	LOW

Note

Pins S0 to S6 have internal pull-up resistances. Therefore, only LOW-level pins need be tied to ground. However, it is recommended that HIGH-level inputs be tied to VDD for applications using fixed-length shifting.

Input/Output Control

Inputs				Shift register (internal)		Outputs
RSTN	ENRC	CLK	OE			
×	×	×	LOW			High impedance
×	×	×	HIGH			Enable
HIGH	HIGH	LOW-to-HIGH	×	×	Rotate shift	
HIGH	LOW	LOW-to-HIGH	×	×	Non-rotate shift	
LOW	×	×	×	×	Reset	

Note

× = don't care

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