SONY

Direct Conversion IC for Digital Satellite Broadcast Tuner

CXA3685ER

Description

The CXA3685ER is an IC developed for direct orthogonal detection of L band (1 to 2GHz) IF signals in a digital satellite broadcast reception tuner.
This direct conversion (Zero-IF) technology eliminates the need for the SAW filter that was formerly necessary. In addition, the CXA3685ER incorporates an RF gain control amplifier, oscillator circuit, wide-band phase shifter circuit and other RF circuits, a baseband LPF, baseband gain control amplifier, tuning PLL, and the inductor and varactor diode needed for a tuning VCO. This makes it possible to realize the front-end RF block without tuning the RF circuits.
(Applications: BS/CS digital broadcast (ISDB-S) tuner)

Features

- ◆ Low power consumption: 430mW (typ.)
- ◆ No need for an external inductor and varactor diode
- ◆ 3.3V single power supply
- ◆ Reception frequency: 950MHz to 2150MHz
- ◆ Wide input range (typ. –65dBm to –15dBm)
- ◆ Internal wide band 90° phase shifter
- ◆ Internal output for controlling an external attenuator
- ◆ Reference signal output for the demodulation circuit
- ◆ Enables to use external reference signals
- ◆ Small package: 48-pin VQFN
- ◆ Enables to reduce power consumption in power save mode when not used: 180mW (typ.)

Package

48-pin VQFN (Plastic)

Note) This IC has pins whose electrostatic discharge strength is weak as the high-frequency process is used. Take care of handling the IC.

Absolute Maximum Ratings

◆ Supply voltage	AVcc, REFVcc, DVcc, OSCVcc, RFVcc	–0.3 to +3.6	V	(Ta = 25℃)
◆ Storage temperature	Tstg	–55 to +150	℃	

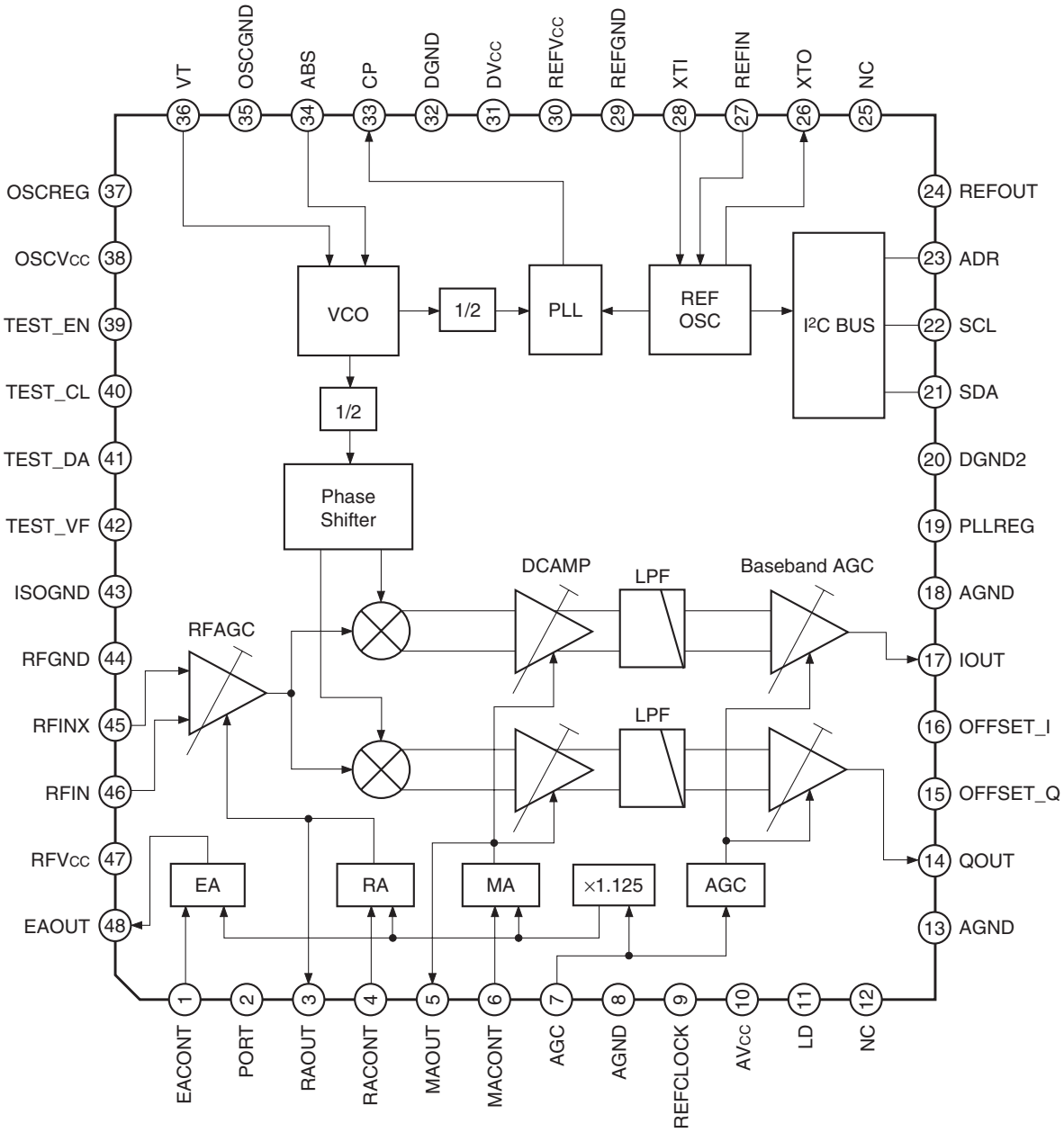
Operating Conditions

◆ Supply voltage	AVcc, REFVcc, DVcc, OSCVcc, RFVcc	3.15 to 3.45	V
◆ Operating temperature	Topr	–10 to +70	℃

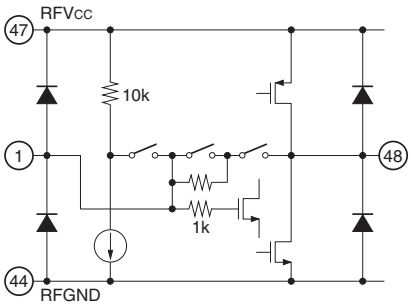
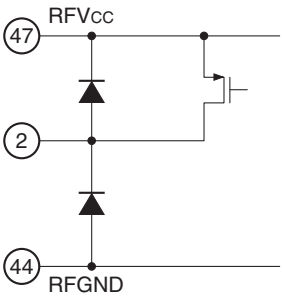
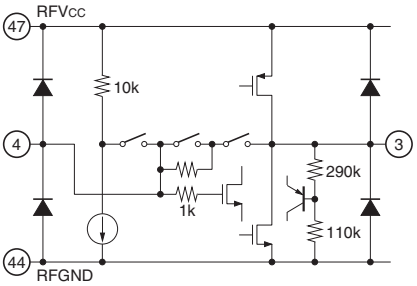
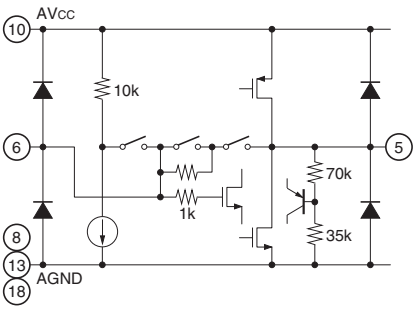
Outline Specifications

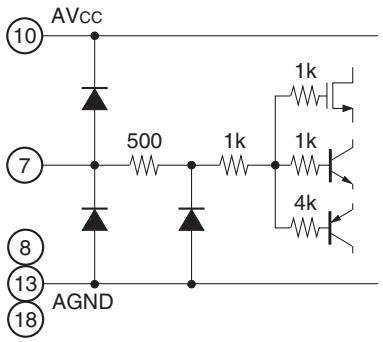
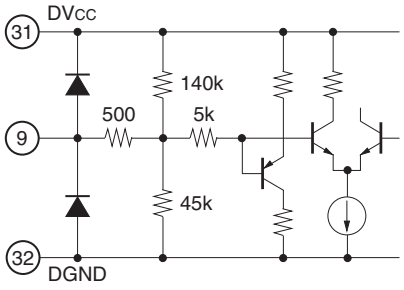
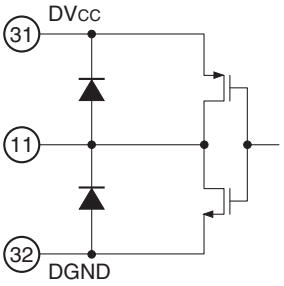
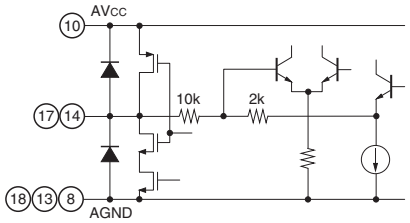
Structure	Direct conversion
Reception frequency	950MHz to 2150MHz
Reception bandwidth	22.5MHz
IF output level	0.7Vp-p
Crystal oscilaltor frequency	4MHz to 32MHz
PLL control	I²C bus
Supply voltage	3.15V to 3.45V
Power consumption	430mW (typ.)
in power save mode	180mW (typ.)

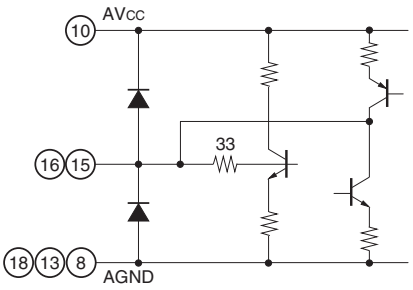
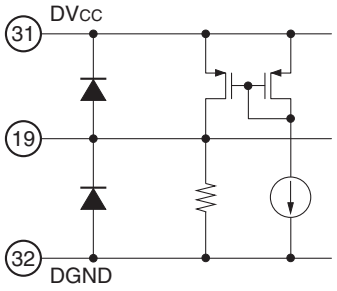
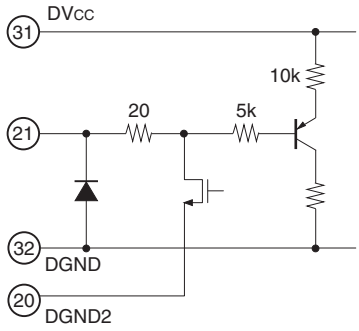
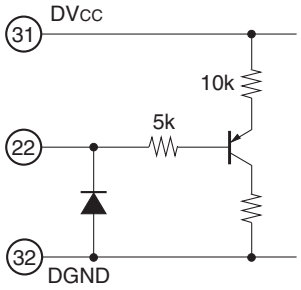
Block Diagram and Pin Configuration

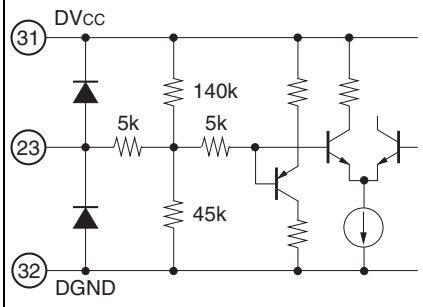
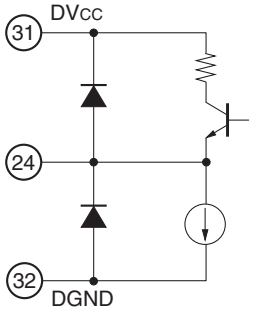
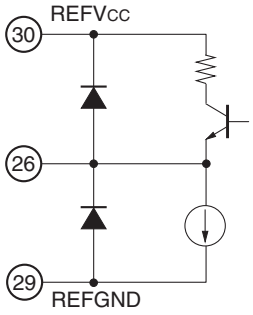
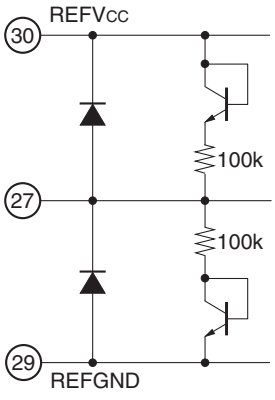


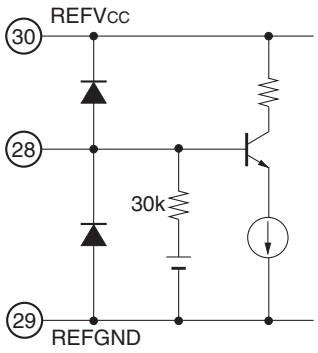
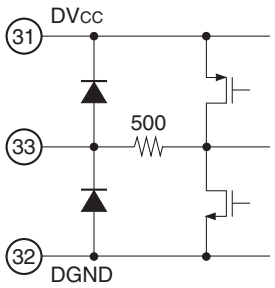
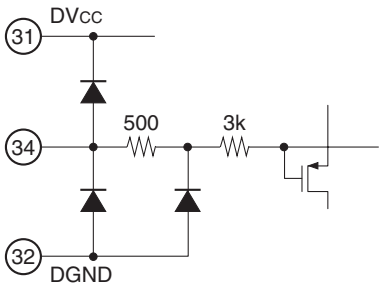
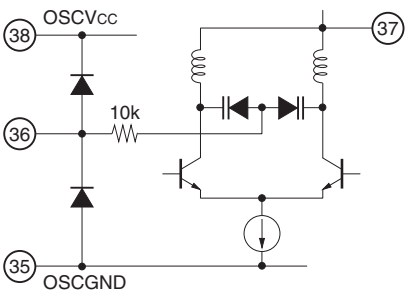
Pin Description and Input/Output Pin Equivalent Circuit

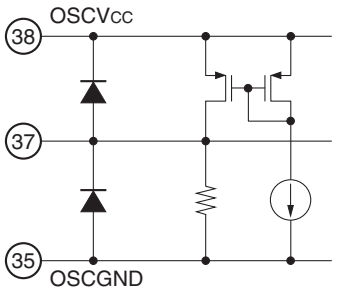
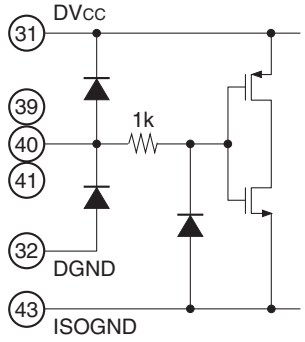
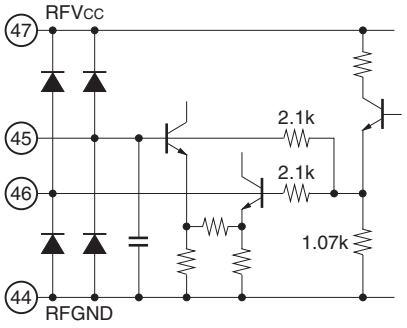
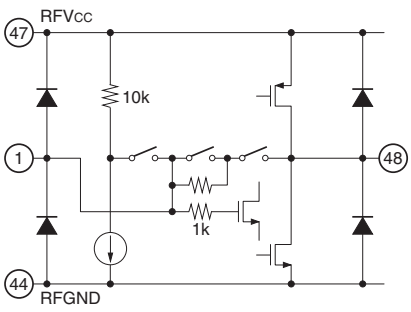
Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
1	EACONT	2.7		Gain control for an external attenuator circuit. (This pin voltage depends on the AGC voltage. This is an example of 3.3V.) (See page 18.)
2	PORT	0 or 3.2		Port output
3	RAOUT	3.2		Gain control for the RFAGC circuit. (This pin voltage depends on the AGC voltage. This is an example of 3.3V.) (See page 18.)
4	RACONT	3.0		
5	MAOUT	3.3		Gain control for the DCAMP circuit. (This pin voltage depends on the AGC voltage. This is an example of 3.3V.) (See page 18.)
6	MACONT	1.7		

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
7	AGC	0 to 3.3		AGC control voltage input
8, 13, 18	AGND	0		GND for the mixer and baseband circuit
9	REFCLOCK	—		Frequency change for the reference signal output (See page 19.)
10	AVCC	3.3		Power supply for the mixer and baseband circuit
11	LD	0 or 3.3		PLL lock detection
12	NC	—		Not used
14	QOUT	1.6		Baseband signal output
17	IOUT	1.6		

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
15	OFFSET_Q	2.2		DC offset correction output for the baseband circuit
16	OFFSET_I	2.2		
19	PLLREG	2.6		Reference voltage output for a PLL circuit
20	DGND2	0		GND for the ACK circuit
21	SDA	0 or 3.3		Data input
22	SCL	0 or 3.3		Clock input

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
23	ADR	0		Address select
24	REFOUT	2.0 or 2.5		Reference signal output
25	NC	—		Not used
26	XTO	2.4		Crystal oscillator connection for reference signal oscillation
27	REFIN	0		External reference signal input

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
28	XTI	2.6		Crystal oscillator connection for reference signal oscillation
29	REFGND	0		GND for the REFOSC block
30	REFVCC	3.3		Power supply for the REFOSC block
31	DVCC	3.3		PLL Power supply
32	DGND	0		PLL GND
33	CP	—		Charge pump output for tuning PLL
34	ABS	—		Auto band select input
35	OSCGND	0		oscillator GND
36	VT	—		Control voltage for tuning PLL

Pin No.	Symbol	Pin voltage [V]	Equivalent circuit	Description
37	OSCREG	2.6		Regulator output for an oscillator
38	OSCVCC	3.3		Power supply for an oscillator
39	TEST_EN	—		Test enable
40	TEST_CL	—		Test clock input
41	TEST_DA	—		Test data input
42	TEST_VF	—		Test power supply
43	ISOGND	0		Isolation GND
44	RFGND	0		GND for the RF block
45	RFINX	1.4		RF input
46	RFIN	1.4		
47	RFVCC	3.3		Power supply for the RF block
48	EAOUT	3.3		Gain control for an external attenuator circuit

Electrical Characteristics

(See the Electrical Characteristics Measurement Circuit.)

V_{CC} = 3.3V, Ta = 25℃

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current	REFICC		1	3	5	mA
	DICC		7	14	21	mA
	OSCICC		8	18	28	mA
	AICC	AGC voltage = 3.3V	40	71	100	mA
	RFICC		10	18	26	mA
Input level range	RFDR	IQ output = 0.7Vp-p/1kΩ load	–65		–15	dBm
IQ phase error	EPH		–5	1.5	7	deg
IQ amplitude error	EAMP		–2	0.5	2	dB
LPF cutoff frequency	FC		19	22.5	26	MHz
Noise figure	NF	RF = 950MHz AGC voltage = 3.3V f_{IF} = 10MHz		10	15	dB
OSC phase noise	PN	RF = 2150MHz 100kHz offset	–78	–82		dBc/Hz
RF pin leakage	LO	50Ω termination, AGC voltage = 3.3V	–50	–60		dBm

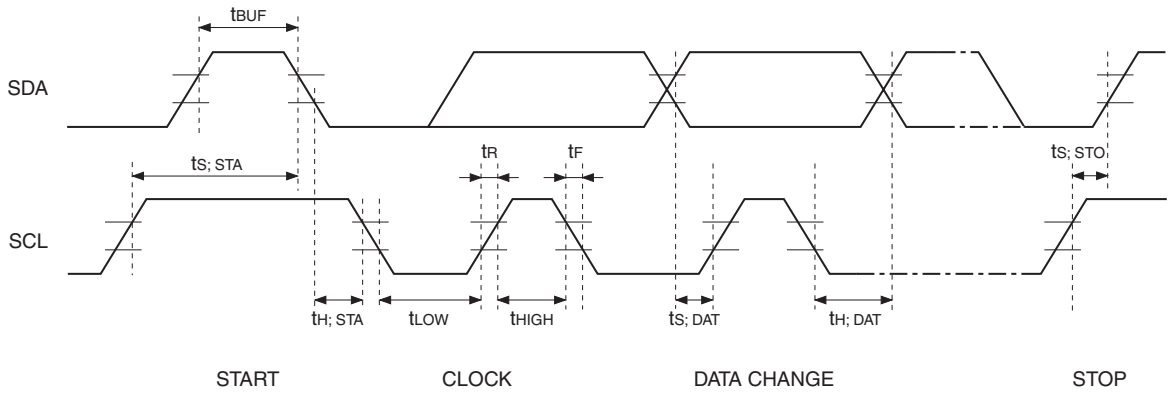
PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
SCL and SDA input						
High level input voltage	V_{IH}		2.3		3.3	V
Low level input voltage	V_{IL}		GND		1	V
High level input current	I_{IH}	V_{IH} = V_{CC}		0	1	µA
Low level input current	I_{IL}	V_{IL} = GND	–30	–20		µA
CPO (Charge pump)						
Output current 1	ICPO1	when 100µA is selected	±50	±100	±150	µA
Output current 2	ICPO2	when 150µA is selected	±75	±150	±225	µA
Output current 3	ICPO3	when 200µA is selected	±100	±200	±300	µA
Output current 4	ICPO4	when 300µA is selected	±150	±300	±450	µA
Output current 5	ICPO5	when 500µA is selected	±250	±500	±750	µA
Output current 6	ICPO6	when 1000µA is selected	±500	±1000	±1500	µA
Output current 7	ICPO7	when 1500µA is selected	±750	±1500	±2250	µA
Output current 8	ICPO8	when 2000µA is selected	±1000	±2000	±3000	µA
REFOSC						
Oscillation frequency range	FXTOSC		4		32	MHz
REFOUT output level	REFOUT	No load, 4MHz output	0.2	0.5	0.8	Vp-p
PORT output voltage	PORTV	ON, 1kΩ load	3	3.2	3.3	V
EAOUT output voltage	EAOUTV	Max. Gain, 350Ω load	2.7	3	3.3	V

Register Block

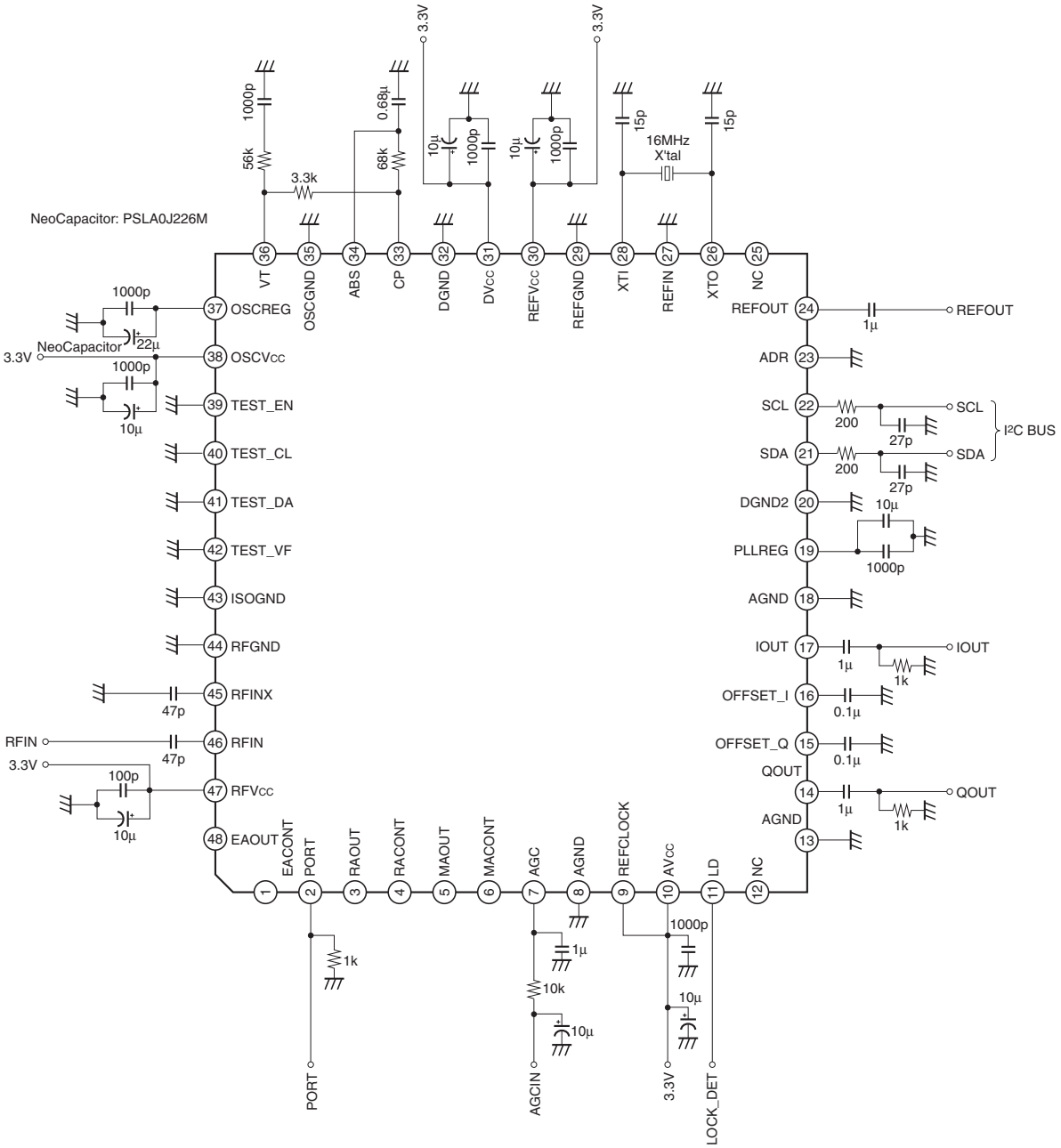
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bus timing (I^2C bus)						
SCL clock frequency	f_{SCL}		0		400	kHz
Bus free time between "STOP" condition and "STOP" condition	t_{BUF}		1300			ns
Start-Hold time	$t_{H;\,STA}$		600			ns
Low hold time	t_{LOW}		1300			ns
High hold time	t_{HIGH}		600			ns
Start-Setup time	$t_{S;\,STA}$		600			ns
Data-Hold time	$t_{H;\,DAT}$		0		900	ns
Data-Setup time	$t_{S;\,DAT}$		100			ns
Rise time	t_R				300	ns
Fall time	t_F				300	ns
Stop-Setup time	$t_{S;\,STO}$		600			ns
Capacitive load of bus line	Cb				400	pF

I^2C Bus Timing Chart



t_{BUF}= Bus free time
$t_{W;\,STA}$= Start waiting time
$t_{H;\,STA}$= Start hold time
t_{LOW}= Low clock pulse width
t_{HIGH}= High clock pulse width
$t_{S;\,DAT}$= Data setup time
$t_{H;\,DAT}$= Data hold time
$t_{S;\,STO}$= Stop setup time
t_R= Rise time
t_F= Fall time

Electrical Characteristics Measurement Circuit



Description of Operation

Control Registers

Most of the functions of this IC can be programmed and controlled by the control registers.

I²C Bus Control

The various registers are controlled by setting values in the internal control registers via the serial interface which is comprised of the two pins SDA (Pin 21) and SCL (Pin 22).
This IC supports the Write mode for receiving various data, and the Read mode for transmitting various data. The mode is set by S0 (R/W bit).
The Write mode for receiving various data is set when the R/W bit is “0”, and the Read mode for transmitting various data is set when the R/W bit is “1”.

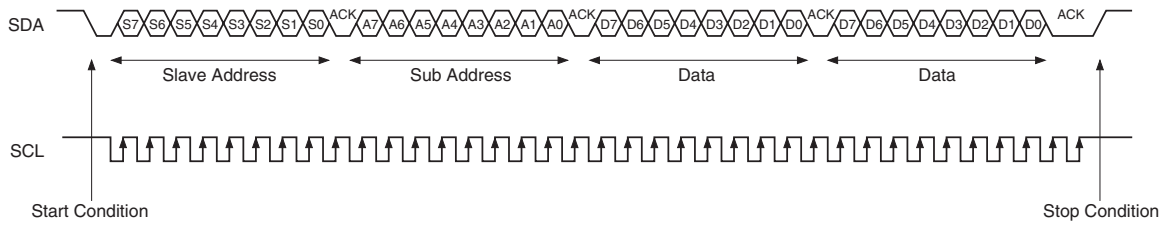
	S7	S6	S5	S4	S3	S2	S1	S0
Slave Address	1	1	0	0	0	MA1	MA0	R/W

Four different slave addresses (IC addresses) can be set by externally setting the ADR pin (Pin 23) to specific voltages so that multiple PLL can exist within a single system.

ADR pin voltage	0 to 0.1Vcc (Default)	Open or 0.2 to 0.3Vcc	0.4 to 0.6Vcc	0.9 to Vcc
Slave Address	1100 000R/W	1100 001R/W	1100 010R/W	1100 011R/W

Note) When leaving the ADR pin (Pin 23) open, always connect a capacitor of approximately 1000pF to the ADR pin.

The 8-bit slave address (IC address), 8-bit sub address, and a number of 8-bit data strings are input MSB first in series to the SDA pin.
An ACK is returned to confirm that the data was accepted each time 8 bits of data are input to the SDA pin.
To set the data for only a specific separate sub address, either send the Stop condition and then reset the sub address, or send the data continuously including the data portions that are not to be changed.
Only the auto increment mode is supported, and modes that specify only specific sub addresses in the manner of “sub address + data + sub address + data” are not supported.



Start Condition
The Start condition is established when the signal input to the SDA pin falls while the SCL pin is High level.

Stop Condition
The Stop condition is established when the signal input to the SDA pin rises while the SCL pin is High level.

Description of the Setting in Write Mode

The CXA3685ER enables to write data to registers when the R/W bit is set to “0”.
Input clock to the SCL pin. The SDA pin data is written to registers at the rising edge of the clock.

Register name	Bit name / Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Ack
Byte0	00	M11	M10	M9	M8	M7	M6	M5	M4	A
Byte1	01	M3	M2	M1	M0	S3	S2	S1	S0	A
Byte2	02	M12	BAND2	BAND1	BAND0	C2	C1	C0	PORT	A
Byte3	03	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	A
Byte4	04	PS9	R2	R1	R0	REFOUT	0	0	0	A
Byte5	05	EA_7	EA_6	EA_5	EA_4	EA_3	EA_2	EA_1	EA_0	A
Byte6	06	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0	A
Byte7	07	RA_7	RA_6	RA_5	RA_4	RA_3	RA_2	RA_1	RA_0	A
Byte8	08	0	0	0	0	1	0	0	0	A
Byte9	09	REFOSC1	REFOSC0	0	0	0	0	0	0	A
Byte10	0A	0	0	0	0	0	0	0	0	A
Byte11	0B	0	0	0	0	0	0	0	0	A

A : Acknowledge bit
M12 to M0 : Main counter
S3 to S0 : Swallow counter
BAND2 to BAND0 : VCO band selection
C2 to C0 : Charge pump current setting
PORT : Port output setting
PS9 to PS1 : Power save mode setting
R2 to R0 : Number of frequency divisions for reference counter setting
REFOUT : REFOUT pin output setting
EA_7 to EA_0 : EAOUT output adjustment
MA_7 to MA_0 : MAOUT output adjustment
RA_7 to RA_0 : RAOUT output adjustment
REFOSC1 to REFOSC0 : Crystal oscillator-Oscillation amplitude switching

Main Counter and Swallow Counter Setting

Main Counter (M0 to M12), Swallow Counter (S0 to S3)

The VCO tuning frequency is obtained by the following formula.

$RF = (1/2) \times fosc = fref \times (16M + S)$

RF : Tuning frequency
fosc : Local oscillator circuit frequency
fref : Comparison frequency
M : Main counter frequency division ratio
S : Swallow counter frequency division ratio

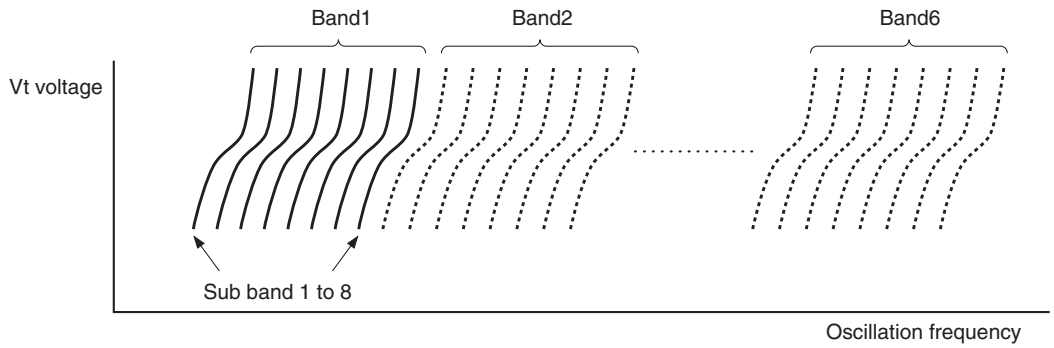
The variable frequency division ranges of M and S are as follows, and are set as binary.

$S < M \leq 8191$
$0 < S \leq 15$

VCO Band Selection

VCO consists of 6 bands and 8 sub bands in each band.
Band data is required to be input according to each oscillation frequency.
Sub bands are automatically set when the band is set.

VCO oscillation frequency vs. Vt voltage



VCO Band Setting

BAND2	BAND1	BAND0	VCO band setting	Reception frequency
0	0	0	Band1	950MHz ≤ Band1 ≤ 1125MHz
0	0	1	Band2	1125MHz < Band2 ≤ 1350MHz
0	1	0	Band3	1350MHz < Band3 ≤ 1625MHz
0	1	1	Band4	1625MHz < Band4 ≤ 1875MHz
1	0	0	Band5	1875MHz < Band5 ≤ 2050MHz
1	0	1	Band6	2050MHz < Band6 ≤ 2150MHz

Charge Pump Current Setting

C2	C1	C0	Output current [μA]
0	0	0	±100
0	0	1	±200
0	1	0	±300
0	1	1	±400
1	0	0	±500
1	0	1	±1000
1	1	0	±1500
1	1	1	±2000

Port Output Setting

PORT	Output
0	Low
1	High

Power Save Mode Setting

The CXA3685ER can be set to power save mode by registers (reduction of power consumption when not using the IC).
Operate the following bits simultaneously in power save mode.

Sets PS9 to PS1 to High

Number of Frequency Divisions for Reference Counter Setting

R2	R1	R0	Number of frequency divisions
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

REFOUT Output Setting

REFOUT	Output
0	ON
1	OFF

Crystal Oscillator – Amplitude Switching Setting

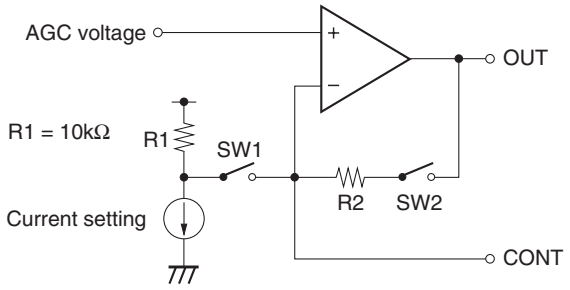
REFOSC1	REFOSC0	Oscillation amplitude
0	0	Large
0	1	Middle
1	0	Small
1	1	Ultra small

REFIN Pin

Connect the REFIN pin to GND when using the internal REFOSC circuit by connecting a crystal oscillator. Input signal to the REFIN pin at CMOS level (3.3Vp-p) when using an external reference signal.

AGC Control Circuit Setting Method

This IC incorporates a circuit for controlling an external ATT circuit (EA), a circuit for controlling RFAGC (RA) and a circuit for controlling DCAMP (MA).
The internal equivalent circuit for each circuit is an operational amplifier as shown bellow.
The characteristics of each amplifier can be controlled by setting an external resistance, or current and internal resistance.



Turn off both SW1 and SW2 when using an external resistor.
Turn on both SW1 and SW2 when using the internal resistor.

SW1 Setting

EA, MA, RA_0	SW1
0	OFF
1	ON

SW2 Setting

EA, MA, RA_4	SW2
0	OFF
1	ON

Current Setting

EA, MA, RA_3	EA, MA, RA_2	EA, MA, RA_1	Current value [μA]
0	0	0	25
0	0	1	50
0	1	0	75
0	1	1	100
1	0	0	125
1	0	1	150
1	1	0	175
1	1	1	200

Resistance Value (R2) Setting

EA, RA, MA_7	EA, MA, RA_6	EA, MA, RA_5	Resistance value [Ω]
0	0	0	40k
0	0	1	35k
0	1	0	30k
0	1	1	25k
1	0	0	20k
1	0	1	15k
1	1	0	10k
1	1	1	5k

Set the current and R2 to the following values to realize the AGC control characteristics (data on page 21) in the Electrical Characteristics Measurement Circuit.

EA : Current value = 75μA, R2 = 40kΩ
MA : Current value = 200μA, R2 = 40kΩ
RA : Current value = 50μA, R2 = 10kΩ

REFOUT Frequency

The REFOUT pin outputs the signal which frequency is divided from the reference signal by changing the voltage of Pin 9.

Voltage of Pin 9	Frequency division ratio
0 to 0.1Vcc	1
0.2 to 0.3Vcc	2
0.4 to 0.6Vcc	8
0.9 to Vcc	4

Example

Voltage of Pin 9 (when Vcc = 3.3V) [V]	Crystal oscillator frequency [MHz]	REFOUT output frequency [MHz]
0 to 0.33	4	4
0.66 to 0.99	8	4
1.33 to 1.98	32	4
2.97 to 3.3	16	4

Description of the Setting in Read Mode

When the R/W bit is set to “1”, the 8-bit data written to registers can be read.
This IC can read the PLL locked or unlocked status and VCO sub band setting.
The read data formats are as follows.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Ack
Slave Address	1	1	0	0	0	MA1	MA0	1	A

	D7	D6	D5	D4	D3	D2	D1	D0	Ack
Status Byte	FL	0	SBAND2	SBAND1	SBAND0	0	0	0	A

MA0 to MA1 : Slave address
FL : PLL lock detection (0: Unlocked, 1: Locked)
SBAND2 to SBAND0 : Sub band detection

SBAND2	SBAND1	SBAND0	VCO sub band setting
0	0	0	Sub Band1
0	0	1	Sub Band2
0	1	0	Sub Band3
0	1	1	Sub Band4
1	0	0	Sub Band5
1	0	1	Sub Band6
1	1	0	Sub Band7
1	1	1	Sub Band8

Measurement Conditions for Representative Characteristics

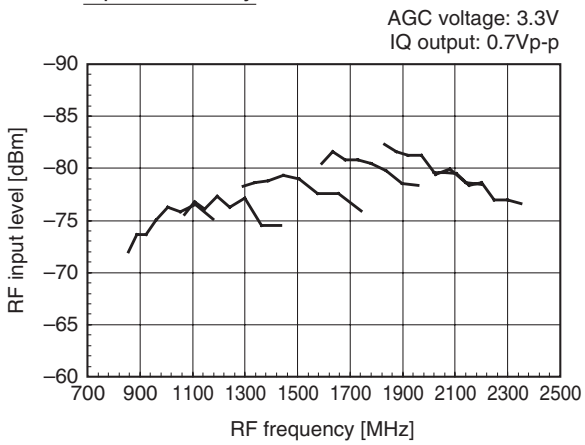
Supply voltage: 3.3 [V]
AGC voltage : 0 to 3.3 [V]

I²C Bus Register Conditions

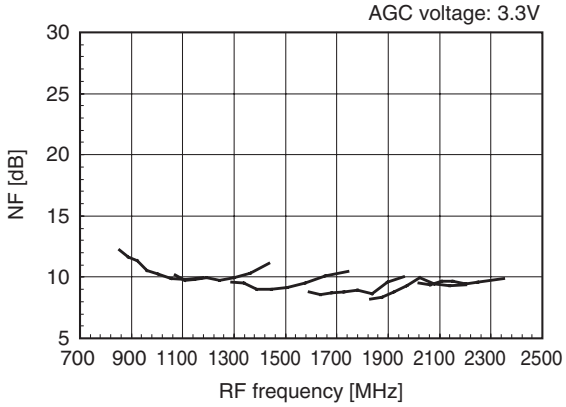
Register name	Bit name / Sub Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Ack
Byte0	00	M11	M10	M9	M8	M7	M6	M5	M4	A
Byte1	01	M3	M2	M1	M0	S3	S2	S1	S0	A
Byte2	02	M12	BAND2	BAND1	BAND0	1	0	0	0	A
Byte3	03	0	0	0	0	0	0	0	0	A
Byte4	04	0	0	1	1	0	0	0	0	A
Byte5	05	0	0	0	1	0	1	0	1	A
Byte6	06	0	0	0	1	1	1	1	1	A
Byte7	07	1	1	0	1	0	0	1	1	A
Byte8	08	0	0	0	0	1	0	1	0	A
Byte9	09	0	0	0	0	0	0	0	0	A
Byte10	0A	0	0	0	0	0	0	0	0	A
Byte11	0B	0	0	0	0	0	0	0	0	A

Representative Characteristics

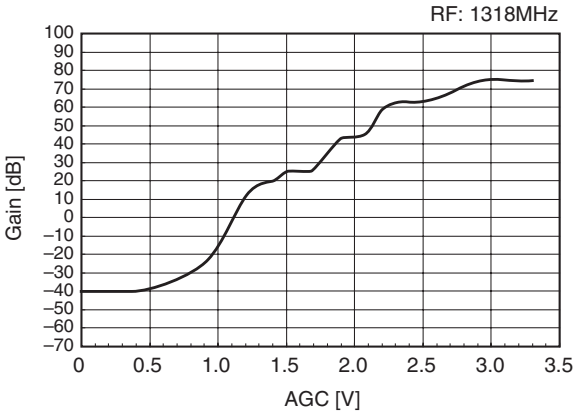
Input Sensitivity



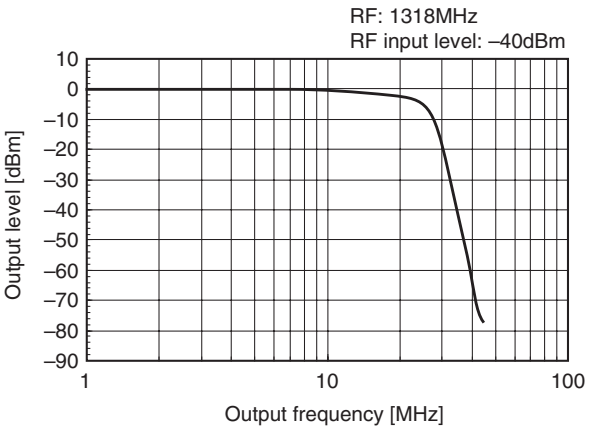
Noise Figure



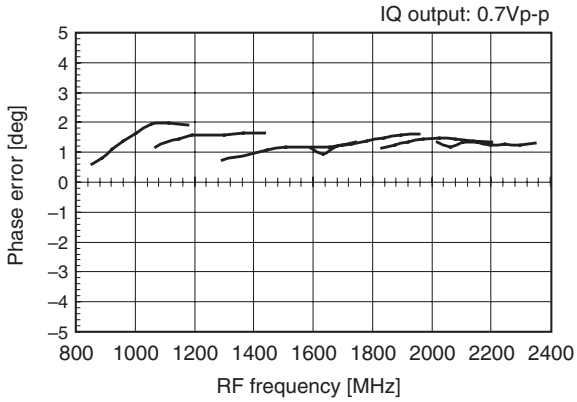
AGC Control Characteristic



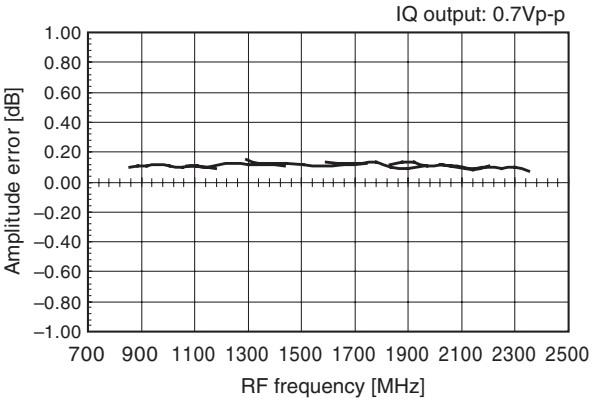
Baseband LPF Frequency Response



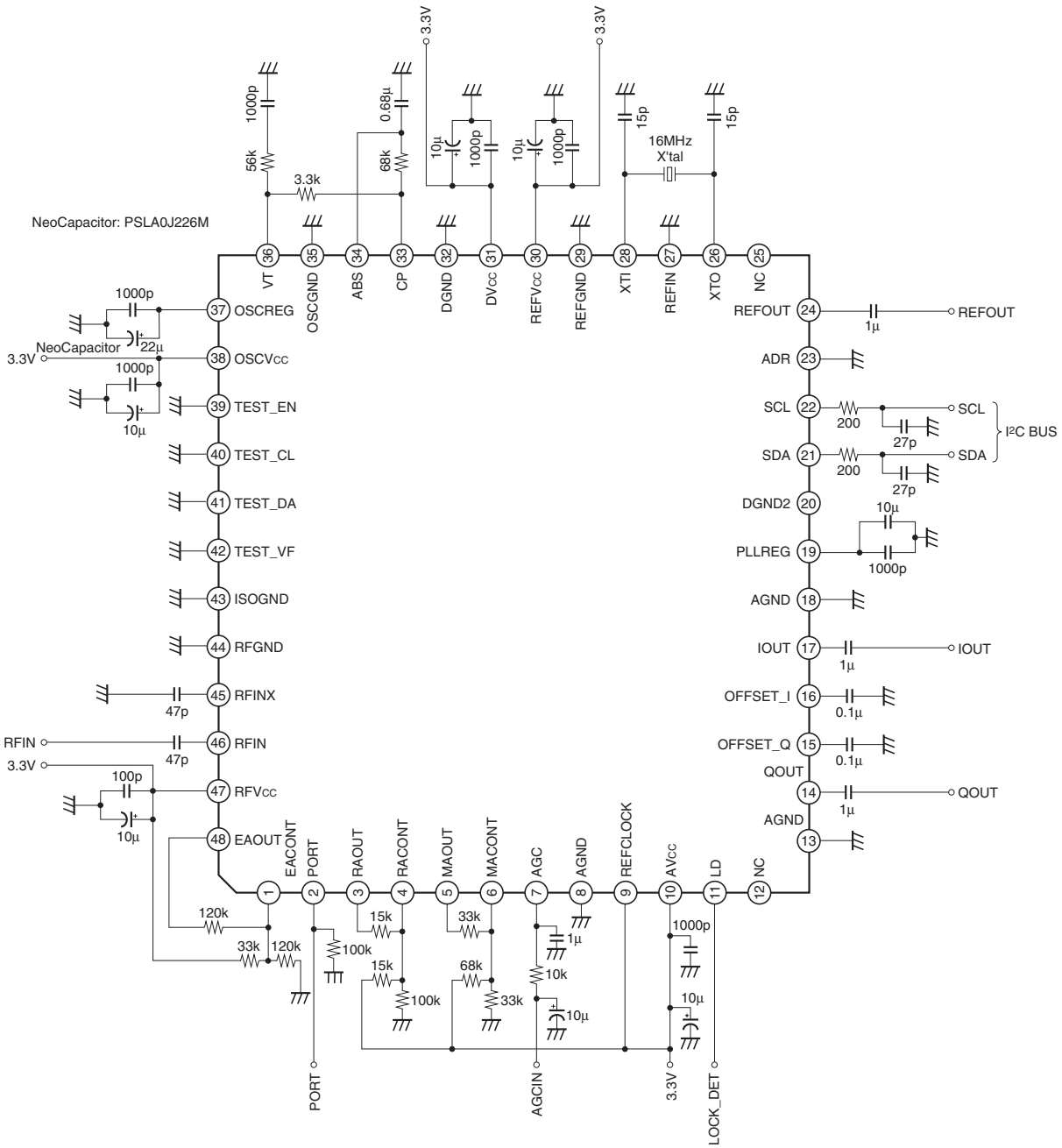
Phase Error



Amplitude Error



Application Circuit

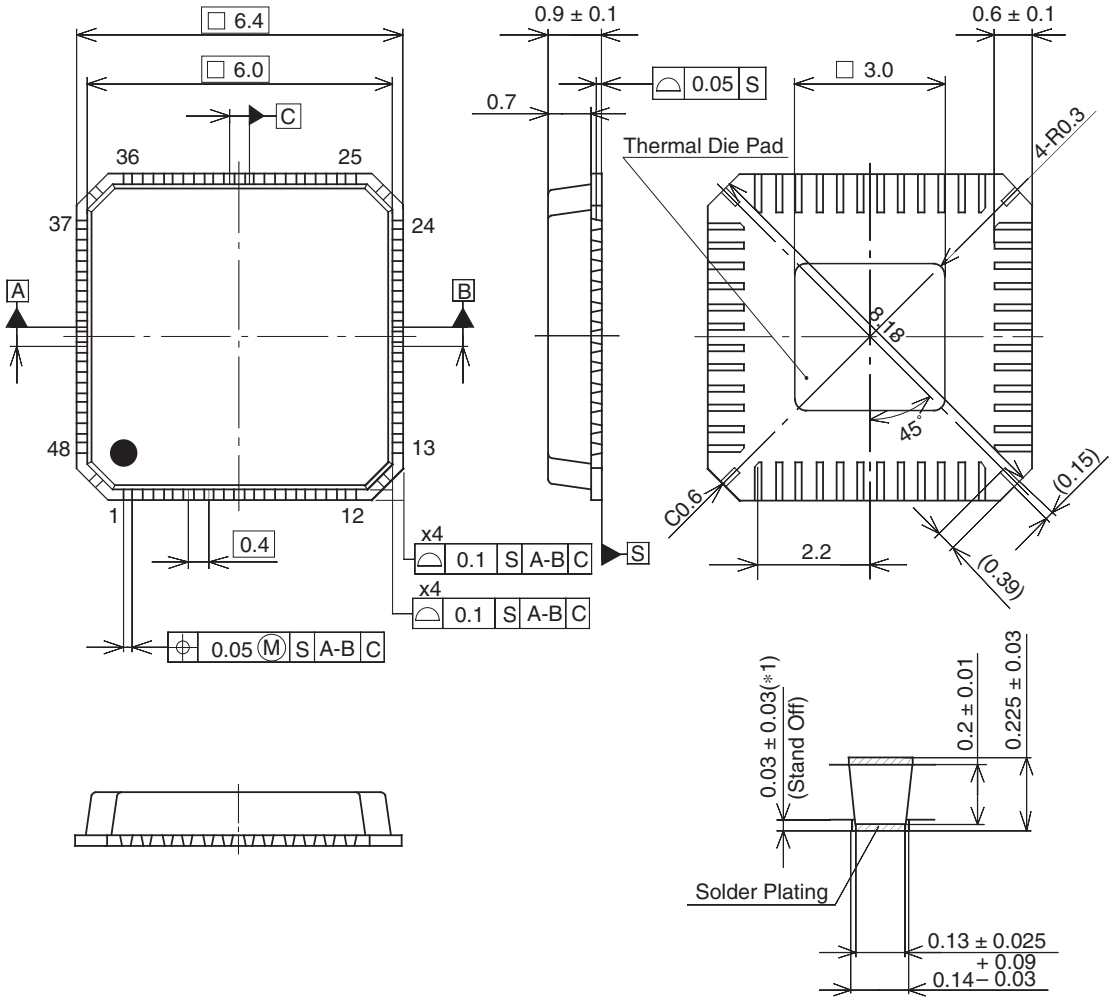


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same

Package Outline

(Unit: mm)

48PIN VQFN (PLASTIC)



NOTE: 1)The dimension of (*1) is apply to DiePad and the lead.

TERMINAL SECTION

SONY CODE	VQFN-48P-02
EIAJ CODE	P-VQFN48-6.0X6.0-0.4
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm