October 2007

LM2755
Charge Pump LED Controller with I2C Compatible Interface in Micro SMD

General Description

The LM2755 is a charge-pump-based, constant current LED driver capable of driving 3 LEDs with a total output current up to 90mA. The diode current waveforms of each LED can be trapezoidal with timing and level parameters (rise time, fall time, high level, low level, delay, high time, low time) programmed via an I²C compatible interface. The 32 brightness levels found on the LM2755 are exponentially spaced (as opposed to linearly spaced) to better match the response of the human eye to changing brightness levels.

The device requires only four small and low-cost ceramic capacitors. The LM2755 provides excellent efficiency without the use of an inductor by operating the charge pump in a gain of 3/2 or in a gain of 1. Maximum efficiency is achieved over the input voltage range by actively selecting the proper gain based on the LED forward voltage requirements.

The pre-regulation scheme used by the LM2755 is optimized to ensure low conducted noise on the input. An internal soft-start circuitry eliminates high inrush current at start-up. The LM2755 consumes 3µA (typ.) of supply current in shut-down.

The LM2755 is available in National's tiny 18-bump thin micro SMD package.

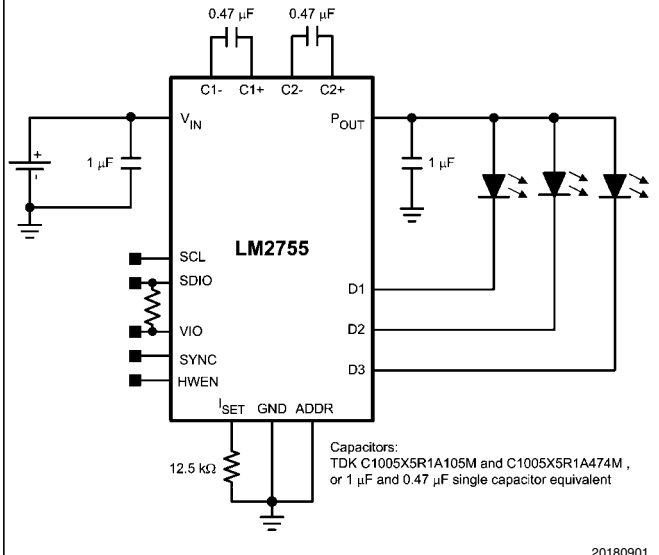
Features

- 90% Peak Efficiency
- Total solution size < 13mm²
- No Inductor Required: Only 4 Inexpensive Ceramic Caps
- 3 Independently Controlled Constant Current Outputs
- Programmable Trapezoidal Dimming Waveform on Each Output
- Programmable Timing Control Via Internal Registers and External Clock Synchronization Input
- 32 Exponential Dimming Steps with 800:1 Dimming Ratio
- Programmable brightness control via I²C compatible interface
- Hardware Enable Pin
- Wide input voltage range: 2.7V to 5.5V
- Tiny 18-bump thin micro SMD: 1.8mm x 1.6mm x 0.6mm

Applications

- Indicator LEDs
- Keypad LED Backlight
- Display LED Backlight
- Fun-light LEDs

Typical Application Circuit



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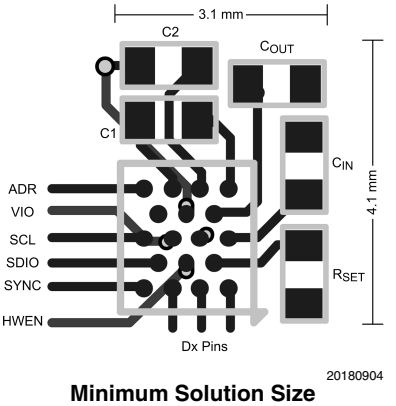

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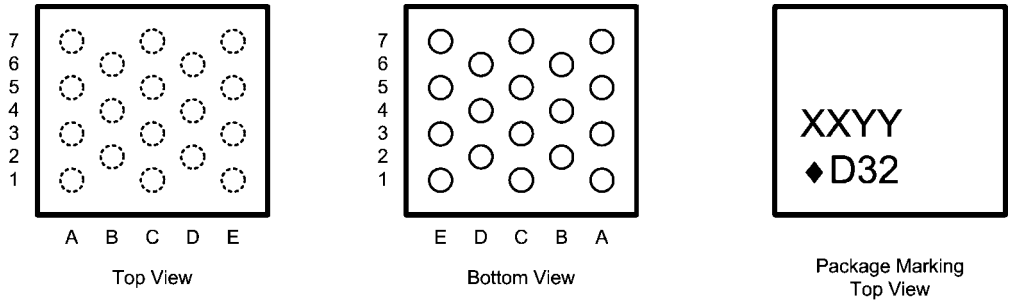
Minimum Solution Size

Connection Diagram

18-Bump Thin Micro SMD Package
1.615mm × 1.807mm × 0.6mm
NS Package Number TMD18AAA



Note: The actual physical placement of the package marking will vary from part to part. The package marking "XX" designates the date code. "YY" is a NSC internal code for die traceability. Both will vary considerably. "♦D32" identifies the device (part number, option, etc.). "♦" indicates the A1 bump location.

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Pin Descriptions

Pin #s	Pin Names	Pin Descriptions
A1	ID1	LED Driver 1
A3	ID2	LED Driver 2
A5	ID3	LED Driver 3
A7	SYNC	External clock synchronization input
B2	ISET	LED Driver Current Set Pin
B4	HWEN	Hardware EN Pin. Low '0' = RESET, High '1' = Normal Operation
B6	SDIO	Serial data Input/Output pin
C1	VIN	Input Voltage Connection
C3	GND	Ground Connection.
C5	VIO	Serial Bus Voltage Level Input
C7	SCL	Serial Clock Pin
D2	P_{OUT}	Charge Pump Output
D4	C2-	Flying Capacitor Connect
D6	GND	Ground connection
E1	C1+	Flying Capacitor Connect
E3	C2+	Flying Capacitor Connect
E5	C1-	Flying Capacitor Connect
E7	ADDR	Chip Address Select Input. VIN = 0x67. Ground = 0x18.

Ordering Information

Order Information	Package	Supplied As
LM2755TM	TMD18AAA, μSMD-18	250 Units, Tape & Reel
LM2755TMX		3000 Units, Tape & Reel

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} pin voltage	-0.3V to 6.0V
SCL, SDIO, VIO, ADDR, SYNC pin voltages	-0.3V to (V_{IN}+0.3V) w/ 6.0V max
I_{Dx} Pin Voltages	-0.3V to (V_{POUT}+0.3V) w/ 6.0V max
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering)	(Note 4)
ESD Rating(Note) Human Body Model	2.5kV

Operating Rating

(Notes 1, 2)

Input Voltage Range	2.7V to 5.5V
Junction Temperature (T_J) Range	-30°C to 105°C
Ambient Temperature (T_A) Range (Note 6)	-30°C to +85°C

Thermal Properties

Juntion-to-Ambient Thermal Resistance (θ_{JA}), TMD18AAA Package (Note 7)	56°C/W

ESD Caution Notice

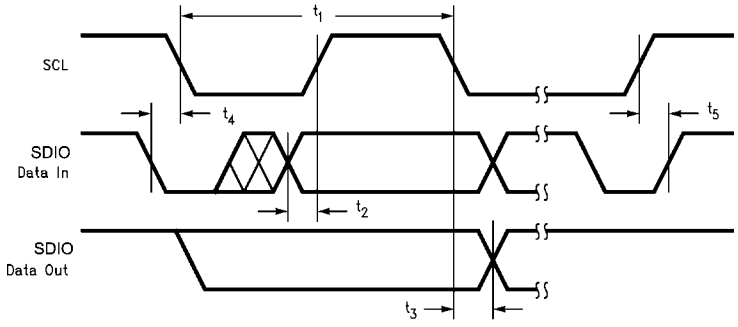
National Semiconductor recommends that all integrated circuits be handled with appropriate ESD precautions. Failure to observe proper ESD handling techniques can result in damage to the device.

Electrical Characteristics (Notes 2, 8)

Limits in standard typeface are for T_J = 25°C, and limits in boldface type apply over the full operating temperature range. Unless otherwise specified: V_{IN} = 3.6V; V_{D1} = 0.4V; V_{D2} = 0.4V; V_{D3} = 0.4V; R_{SET} = 12.5kΩ; D1, D2, and D3 = Fullscale Current; EN1, EN2, and EN3 Bits = "1"; CLK bit = '0'; C1=C2= 0.47µF, C_{IN}=C_{OUT}= 1µF; Specifications related to output current(s) and current setting pins (I_{Dx} and I_{SET}) apply to D1, D2 and D3. (Note 9)

Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{Dx}	Output Current Regulation	3.0V ≤ V_{IN} ≤ 5.5V		**18.7**	20.7	**22.7**	mA
I_{MATCH}	Output Current Matching	3.0V ≤ V_{IN} ≤ 5.5V (Note 10)			1		%
I_Q	Quiescent Supply Current	Gain = 3/2 D_{1-3} = OPEN, R_{SET} = OPEN			1.0	**1.3**	mA
I_{SD}	Shutdown Supply Current	3.0V ≤ V_{IN} ≤ 5.5V EN1 = EN2 = EN3 = 0			5	**9.5**	µA
V_{SET}	I_{SET} Pin Voltage	3.0V ≤ V_{IN} ≤ 5.5V			1.25		V
I_{DX} / I_{SET}	Output Current to Current Set Ratio	(Note 11)			200		
V_{DxTH}	V_{Dx} 1x to 3/2x Gain Transition Threshold	V_{D1} and/or V_{D2} and/or V_{D3}Falling			350		mV
V_{HR}	Current Source Headroom Voltage Requirement (Note 12)	I_{Dx} = 95% ×I_{Dx} (nom.) (I_{Dx} (nom) ≈ 20mA) Gain = 3/2			200		mV
f_{SW}	Switching Frequency			**0.975**	1.25	**1.525**	MHz
t_{START}	Start-up Time	P_{OUT} = 90% steady state			300		µs
f_{PWM}	Internal Diode Current PWM Frequency				20		kHz
f_{SYNC}	Maximum External Sync Frequency				1.0		MHz
V_{HWEN}	HWEN Voltage Thresholds	2.7V ≤ V_{IN} ≤ 5.5V	Reset	**0**		**0.5**	V
			Normal Operation	**1.23**		**VIN**	
I²C Compatible Interface Voltage Specifications (SCL, SDIO, VIO)							
V_{IO}	Serial Bus Voltage Level	2.7V ≤ V_{IN} ≤ 5.5V(Note 13)		**1.44**		**V_{IN}**	V
V_{IL}	Input Logic Low "0"	2.7V ≤ V_{IN} ≤ 5.5V, VIO = 3.0V		**0**		**0.35 × V_{IO}**	V
V_{IH}	Input Logic High "1"	2.7V ≤ V_{IN} ≤ 5.5V, VIO = 3.0V		**0.65 × V_{IO}**		**V_{IO}**	V
V_{OL}	Output Logic Low "0"	I_{LOAD} = 3mA				**400**	mV
I²C Compatible Interface Timing Specifications (SCL, SDIO, VIO)(Note 14)							

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_1	SCL Clock Period		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out stable After SCL Low		**0**			ns
t_4	SDIO Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDIO High Hold Time After SCL High (Stop)		**100**			ns



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 155°C (typ.).

Note 4: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1112: Micro SMD Wafer Level Chip Scale Package (AN-1112).

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Note 5: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7)

Note 6: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 105°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 7: Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to National Semiconductor Application Note 1112: Micro SMD Wafer Level Chip Scale Package (AN-1112).

Note 8: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 9: C_{IN}, C_{POUT}, C_1, and C_2 : Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics

Note 10: For the current sinks on a part, the following are determined: the maximum sink current in the group (MAX), the minimum sink current in the group (MIN), and the average sink current of the group (AVG). Two matching numbers are calculated: (MAX-AVG)/AVG and (AVG-MIN)/AVG. The larger number of the two (worst case) is considered the matching figure. The typical specification provided is the most likely norm of the matching figure for all parts

Note 11: The maximum total output current for the LM2755 should be limited to 90mA. The total output current can be split among any of the three banks (I_{D1} = I_{D2} = I_{D3} = 30mA Max.). Under maximum output current conditions, special attention must be given to input voltage and LED forward voltage to ensure proper current regulation. See the Maximum Output Current section of the datasheet for more information.

Note 12: For each I_{Dx} output pin, headroom voltage is the voltage across the internal current sink connected to that pin. For $V_{HR} = V_{OUT} - V_{Dxx}$. If headroom voltage requirement is not met, LED current regulation will be compromised.

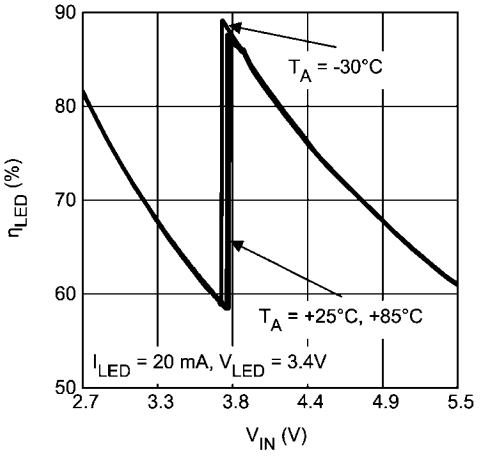
Note 13: SCL and SDIO signals are referenced to VIO and GND for minimum VIO voltage testing.

Note 14: SCL and SDIO should be glitch-free in order for proper brightness control to be realized.

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C; V_{IN} = 3.6V; V_{HWEN} = V_{IN}; V_{D1} = V_{D2} = V_{D3} = 2.75V, R_{SET} = 12.5kΩ, C_1=C_2= 0.47µF, C_{IN} = C_{VOUT} = 1µF; ENA = ENB = ENC = '1'.

LED Drive Efficiency vs Input Voltage



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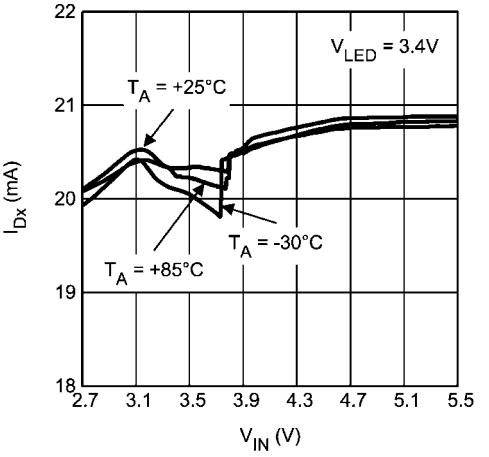
Diode Current vs Input Voltage



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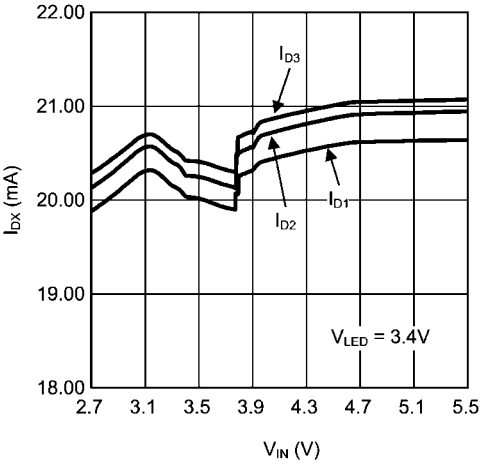
Current Matching vs Input Voltage
3 LEDs



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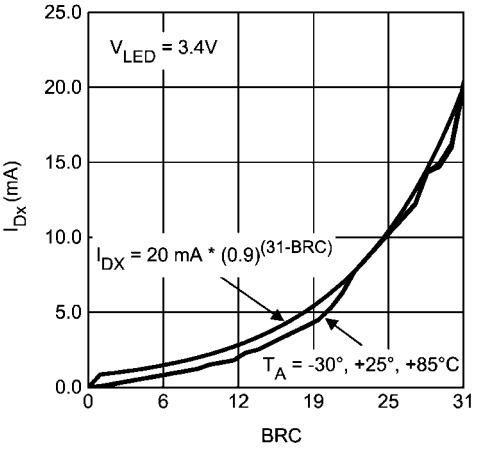
Diode Current vs Brightness Code



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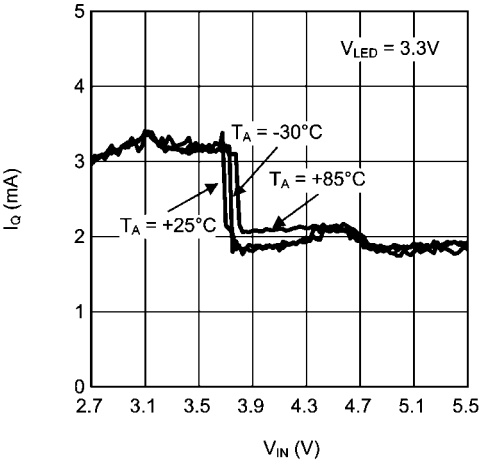
Quiescent Current vs Input Voltage



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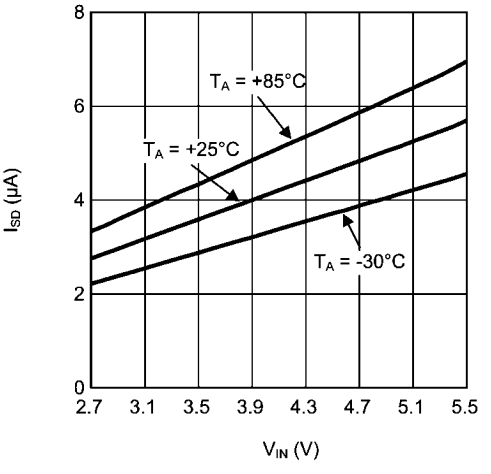
Shutdown Current vs Input Voltage



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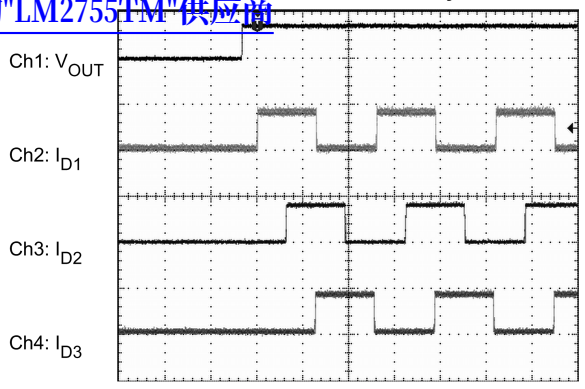
Square Wave Pattern with Delays



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

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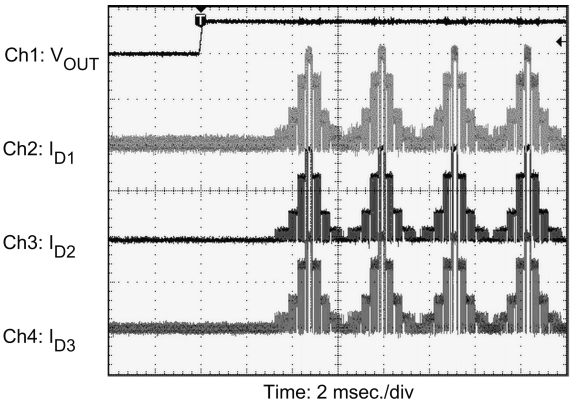
Triangle Wave Pattern



Time: 2 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

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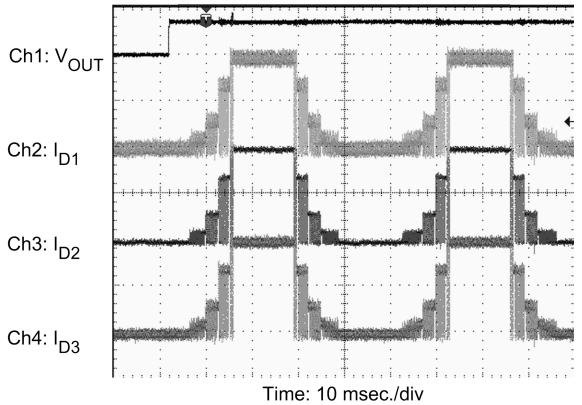
Trapezoid Wave Pattern



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

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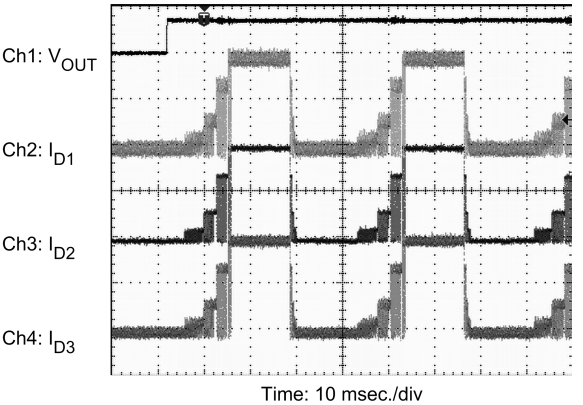
Slow Ramp-Up / Fast Ramp-Down Wave Pattern



Time: 10 msec./div
Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

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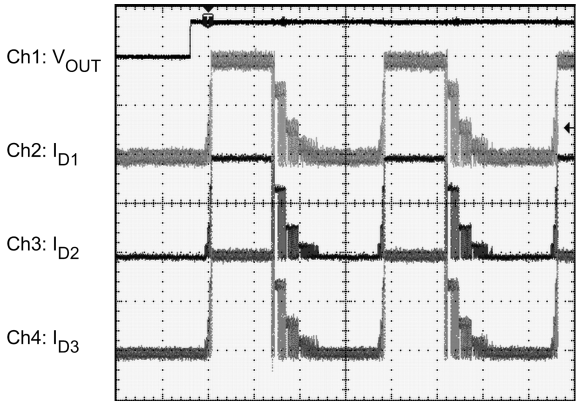
Fast Ramp-Up / Slow Ramp-Down Wave Pattern



Ch1: 5V/div Ch2: 10 mA/div
Ch3: 10 mA/div Ch4: 10 mA/div

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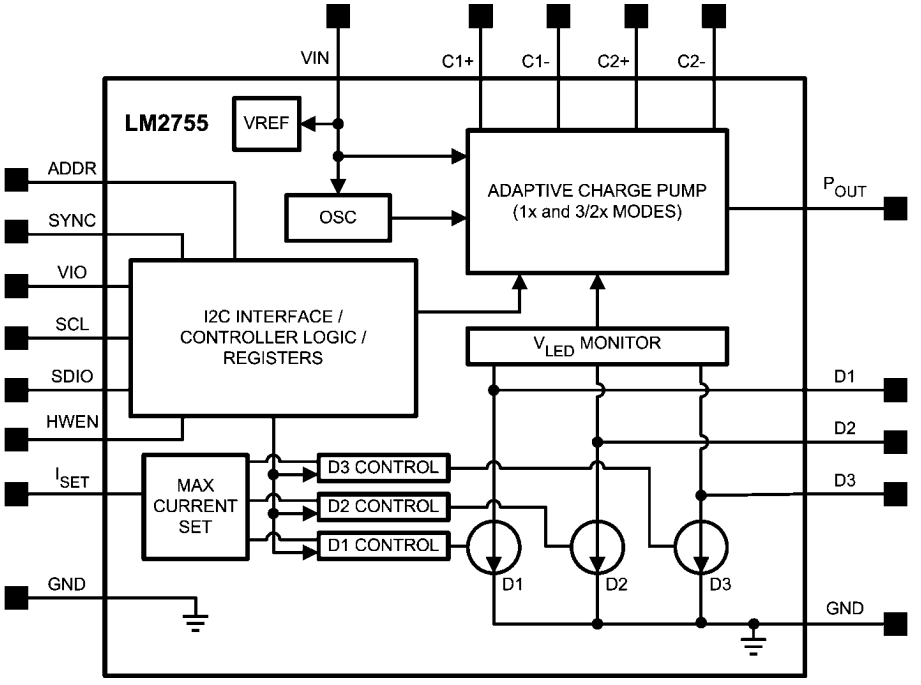
Block Diagram



Circuit Components

CHARGE PUMP

The input to the 3/2× - 1x charge pump is connected to the V_{IN} pin, and the regulated output of the charge pump is connected to the V_{OUT} pin. The recommended input voltage range of the LM2755 is 3.0V to 5.5V. The device's regulated charge pump has both open loop and closed loop modes of operation. When the device is in open loop, the voltage at V_{OUT} is equal to the gain times the voltage at the input. When the device is in closed loop, the voltage at V_{OUT} is regulated to 4.6V (typ.). The charge pump gain transitions are actively selected to maintain regulation based on LED forward voltage and load requirements. This allows the charge pump to stay in the most efficient gain (1x) over as much of the input voltage range as possible, reducing the power consumed from the battery.

LED FORWARD VOLTAGE MONITORING

The LM2755 has the ability to switch converter gains (1x or 3/2x) based on the forward voltage of the LED load. This ability to switch gains maximizes efficiency for a given load. Forward voltage monitoring occurs on all diode pins. At higher input voltages, the LM2755 will operate in pass mode, allowing the POUT voltage to track the input voltage. As the input voltage drops, the voltage on the Dx pins will also drop ($V_{DX} = V_{POUT} - V_{LEDx}$). Once any of the active Dx pins reaches a voltage approximately equal to 350mV, the charge pump will then switch to the gain of 3/2. This switchover ensures that the current through the LEDs never becomes pinched off due to a lack of headroom on the current sources.

Only active Dx pins will be monitored. For example, if only D1 is enabled, the LEDs connected to D2 and D3 will not affect the gain transition point. If all Dx pins are enabled, all diodes will be monitored, and the gain transition will be based upon the diode with the highest forward voltage.

HWEN PIN

The LM2755 has a hardware enable/reset pin (HWEN) that allows the device to be disabled by an external controller without requiring an I²C write command. Under normal operation, the HWEN pin should be held high (logic '1') to prevent an unwanted reset. When the HWEN is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see the *Electrical Characteristics* section of the datasheet for required voltage thresholds.

SYNC PIN

The SYNC pin allows the LM2755 to use an external clock to generate the timing within. This allows the LM2755's current-sinks to pulse-width modulate (PWM) and transition at a user controlled frequency. The PWM frequency and the step-time increment can be set by feeding a clock signal into the sync pin and enabling bit '6' in the general purpose register (See the I2C Compatible Interface section for more details.). The maximum frequency allowed to ensure current level accuracy is 1MHz. This external clock is divided down by 32x to create the minimum time-step and PWM frequency. For a 1MHz external clock, the PWM frequency becomes 31.25KHz and the minimum step time becomes 32 µseconds. If not used, it is recommended that the SYNC pin be tied to ground.

ADDR PIN

The ADDR pin allows the user to chose between two different I2C chip addresses for the LM2755. Tying the ADDR pin high sets the chip address to hex 67 (0x67 or 67h), while tying the ADDR pin low sets the chip address to hex 18(0x18 or 18h). This feature allows multiple LM2755's to be used within a system in addition to providing flexibility in the event another

chip in the system has a chip address similar to the default LM2755 address (0x48).

I²C COMPATIBLE INTERFACE

DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

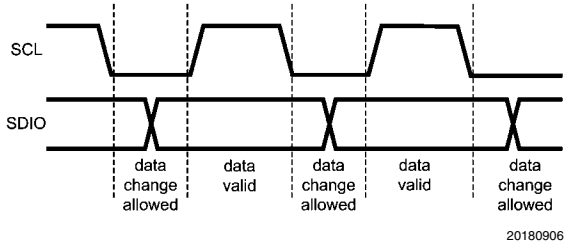


FIGURE 1. Data Validity Diagram

A pull-up resistor between VIO and SDIO must be greater than [**(VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

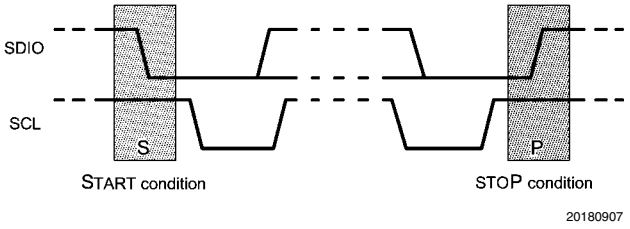


FIGURE 2. Start and Stop Conditions

TRANSFERING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM2755 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM2755 generates an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2755 address is 18h is ADR is tied low and 67h if ADR is tied high . For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

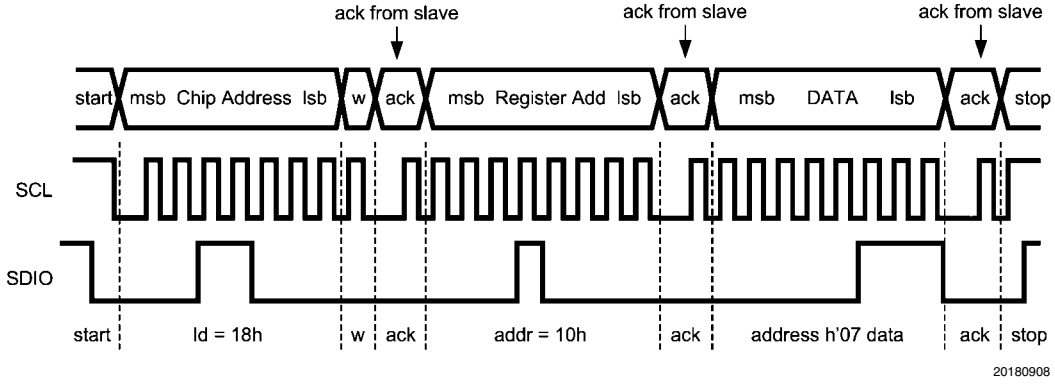


FIGURE 3. Write Cycle
w = write (SDIO = "0")
r = read (SDIO = "1")
ack = acknowledge (SDIO pulled down by either master or slave)
rs = repeated start
id = chip address, 18h if ADR = '0' or 67h if ADR = '1' for LM2755

I²C COMPATIBLE CHIP ADDRESS

The chip address for LM2755 is 0011000 (0x18) when ADR = '0' or 1100111(0x67) when ADR = '1'.

Dimming Waveform

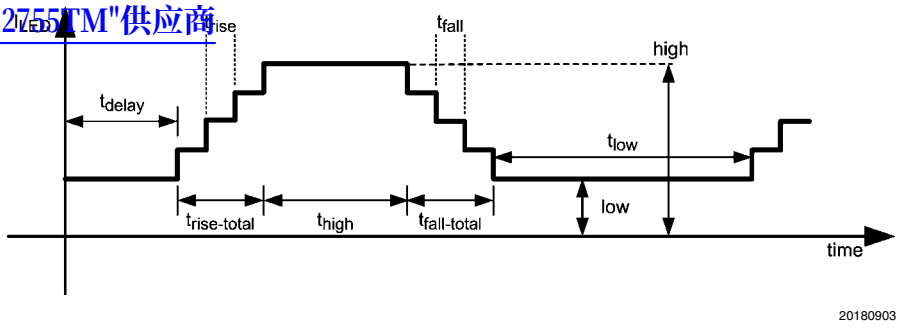


FIGURE 4.

INTERNAL REGISTERS OF LM2755

Register Name	Internal Hex Address	Power On Value
General Purpose	x10	0000 0000
Time Step	x20	1000 1000
D1 High Level	xA9	1110 0000
D1 Low Level	xA8	1110 0000
D1 Delay: t_{delay}	xA1	0000 0000
D1 Ramp-Up Step Time: t_{rise}	xA5	0000 0000
D1 Time High: t_{high}	xA3	0000 0000
D1 Ramp-Down Step Time: t_{fall}	xA4	0000 0000
D1 Timing: t_{low}	xA2	0000 0000
D2 High Level	xB9	1110 0000
D2 Low Level	xB8	1110 0000
D2 Delay: tdelay	xB1	0000 0000
D2 Ramp-Up Step Time: t_{rise}	xB5	0000 0000
D2 Time High: t_{high}	xB3	0000 0000
D2 Ramp-Down Step Time: t_{fall}	xB4	0000 0000
D2 Timing: t_{low}	xB2	0000 0000
D3 High Level	xC9	1110 0000
D3 Low Level	xC8	1110 0000
D3 Delay: tdelay	xC1	0000 0000
D3 Ramp-Up Step Time: t_{rise}	xC5	0000 0000
D3 Time High: t_{high}	xC3	0000 0000
D3 Ramp-Down Step Time: t_{fall}	xC4	0000 0000
D3 Timing: t_{low}	xC2	0000 0000

General Purpose Register Description

- Bit 0: enable output D1 with high current level.
- Bit 1: enable output D2 with high current level.
- Bit 2: enable output D3 with high current level.
- Bit 3: enable dimming waveform on output D1.
- Bit 4: enable dimming waveform on output D2.
- Bit 5: enable dimming waveform on output D3.
- Bit 6: enable external clock. '1' = External Clock Sync, '0' = Internal Clock Used
- Bit 7: If Bit 7 = 0 the charge pump is powered on before any dimming waveform is enabled. If Bit7 = 1 the dimming waveform can be enabled before charge pump is powered on.

Application Information

SETTING FULL-SCALE LED CURRENT

The current through the LEDs connected to D1, D2 and D3 can be set to a desired level simply by connecting an appropriately sized resistor (R_{SET}) between the I_{SET} pin of the LM2755 and GND. The LED currents are proportional to the current that flows through the I_{SET} pin and are a factor of 200 times greater than the I_{SET} currents. The feedback loop of the internal amplifier sets the voltage of the I_{SET} pin to 1.25V (typ.). The statement above is simplified in the equation below:

$$I_{Dx\ (Full\text{-}Scale)} = 200 \times (V_{ISET} / R_{SET})$$

Please refer to the I²C Compatible Interface section of this datasheet for detailed instructions on how to adjust the brightness control registers.

BRIGHTNESS LEVEL CONTROL

Once the desired R_{SET} value has been chosen, the LM2755 has the ability to internally dim the LEDs by modulating the currents with an internally set 20kHz PWM signal. The PWM duty cycle percentage is independently set for each LED through the I²C compatible interface. The 32 brightness levels follow a exponentially increasing pattern rather than a linearly increasing one in order to better match the human eyes response to changing brightness. The brightness level response is modeled in the following equations.:

$$I_{Dx\ LOW} = (0.9)^{(31-n_{LOW})} \times I_{Dx\ Fullscale}$$

$$I_{Dx\ HIGH} = (0.9)^{(31-n_{HIGH})} \times I_{Dx\ Fullscale}$$

n_{HIGH} and n_{LOW} are numbers between 0 and 31 stored in the brightness level registers. When the waveform enable bits are set to '1', n_{HIGH} and n_{LOW} are the brightness level boundries. These equations apply to all Dx outputs and their corresponding registers. A '0' code in the brightness control register sets the current to an "off-state" (0mA).

TIME STEP CONTROL

Bit 0-Bit 2: The value of the 3 bits is equal to N, which is used in the timing control equations. $0 \leq N \leq 7$. The minimum internal time step (N=0) is 50µs. Setting the time-step to N=7 results in a minimum time step of 400µsec. Time step = 50µsec × (N+1)

Bit 3-Bit 7: Not used

DELAY CONTROL

The LM2755 allows the programmed current waveform on each diode pin to independantly start with a delay upon enabling the waveform dimming bits in the general purpose register. There are 256 delay levels available. The delay time is set by the following equation:

$$t_{delay} = N \times n_{delay}$$

n_{delay} is stored in the Dx delay registers and N is stored in the Time Step Control register.

By default, n_{delay} =0 with a range of $0 \leq n_{delay} \leq 255$.

TIMING CONTROL

$T_{PWM\ INTERNAL}$ =50µs, N is a value stored in the Time Step register, and n_{Trise} n_{Tfall}, n_{Thigh}, n_{Tlow} are numbers between 0 and 255, stored in the timing control registers. The durations of the rise, high, fall and low times are given by:

$$t_{rise/fall\ Total} = t_{PWM\ INTERNAL} \times 2^N \times (n_{high}\text{-}n_{low}) \times n_{Trise/fall}$$

where $0 \leq n_{Trise/fall} \leq 255$

$$t_{rise\ or\ fall\ Total} = 50\mu s \times (n_{high}\text{-}n_{low}) \text{ when } n_{Trise/fall} = 0$$

$$t_{high\ or\ low} = t_{PWM\ INTERNAL} \times 2^N \times (n_{high/low} + 1)$$

where $0 \leq n_{Thigh/low} \leq 255$

SYNC PIN TIMING CONTROL

It is possible to replace the internal clock with an external one placed on the external SYNC pin. Writing a '1' to bit6 in the general purpose register switches the system clock from being internally generated to externally generated. The period of the PWM modulating signal becomes:

$$t_{PWM} = t_{SYNC} / 32$$

The maximum recommended SYNC frequency is 1MHz. This frequency yields a PWM frequency of 31.25KHz and the minimum step time of 32 µsec.

MAXIMUM OUTPUT CURRENT, MAXIMUM LED VOLTAGE, MINIMUM INPUT VOLTAGE

The LM2755 can drive 8 LEDs at 22.5mA each (GroupA , GroupB, GroupC) from an input voltage as low as 3.2V, so long as the LEDs have a forward voltage of 3.6V or less (room temperature).

The statement above is a simple example of the LED drive capability of the LM2755. The statement contains the key application parameters that are required to validate an LED-drive design using the LM2755: LED current (I_{LEDx}), number of active LEDs (N_x), LED forward voltage (V_{LED}), and minimum input voltage ($V_{IN\text{-}MIN}$).

The equation below can be used to estimate the maximum output current capability of the LM2755:

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times R_{OUT})] \div [(N_x \times R_{OUT}) + k_{HRx}] \text{ (eq. 1)}$$

$$I_{LED\_MAX} = [(1.5 \times V_{IN}) - V_{LED} - (I_{ADDITIONAL} \times 2.4\Omega)] \div [(N_x \times 2.4\Omega) + k_{HRx}]$$

$I_{ADDITIONAL}$ is the additional current that could be delivered to the other LED Groups.

R_{OUT} – Output resistance. This parameter models the internal losses of the charge pump that result in voltage droop at the pump output V_{OUT}. Since the magnitude of the voltage droop is proportional to the total output current of the charge pump, the loss parameter is modeled as a resistance. The output resistance of the LM2755 is typically 2.4Ω (V_{IN} = 3.6V, T_A = 25°C). In equation form:

$$V_{VOUT} = (1.5 \times V_{IN}) - [(I_{LED1} + I_{LED2} + I_{LED3}) \times R_{OUT}] \quad \text{(eq. 2)}$$

k_{HR} – Headroom constant. This parameter models the minimum voltage required to be present across the current sinks for them to regulate properly. This minimum voltage is proportional to the programmed LED current, so the constant has units of mV/mA. The typical k_{HR} of the LM2755 is 3.25mV/mA. In equation form:

$$(V_{VOUT} - V_{LEDx}) > k_{HRx} \times I_{LEDx} \quad \text{(eq. 3)}$$

Typical Headroom Constant Values

$k_{HR1} = k_{HR2} = k_{HR3}$ = 10 mV/mA

The "$I_{LED\text{-}MAX}$" equation (eq. 1) is obtained from combining the R_{OUT} equation (eq. 2) with the k_{HRx} equation (eq. 3) and solving for I_{LEDx}. Maximum LED current is highly dependent on minimum input voltage and LED forward voltage. Output current capability can be increased by raising the minimum input voltage of the application, or by selecting an LED with a lower forward voltage. Excessive power dissipation may also limit output current capability of an application.

Total Output Current Capability

The maximum total current that can be drawn from the LM2755 is 90mA. Each driver Group has a maximum allotted current per Dx sink that must not be exceeded.

DRIVER TYPE	MAXIMUM Dx CURRENT
Dx	30mA per Dx Pin

The 90mA load can be distributed in many different configurations. Special care must be taken when running the LM2755 at the maximum output current to ensure proper functionality.

POWER EFFICIENCY

Efficiency of LED drivers is commonly taken to be the ratio of power consumed by the LEDs (P_{LED}) to the power drawn at the input of the part (P_{IN}). With a 3/2× - 1× charge pump, the input current is equal to the charge pump gain times the output current (total LED current). The efficiency of the LM2755 can be predicted as follow:

$$P_{LEDTOTAL} = (V_{LEDA} \times N_A \times I_{LEDA}) + (V_{LEDB} \times N_B \times I_{LEDB}) + (V_{LEDC} \times I_{LEDC})$$

$$P_{IN} = V_{IN} \times I_{IN}$$

$$P_{IN} = V_{IN} \times (GAIN \times I_{LEDTOTAL} + I_Q)$$

$$E = (P_{LEDTOTAL} \div P_{IN})$$

The LED voltage is the main contributor to the charge-pump gain selection process. Use of low forward-voltage LEDs (3.0V- to 3.5V) will allow the LM2755 to stay in the gain of 1× for a higher percentage of the lithium-ion battery voltage range when compared to the use of higher forward voltage LEDs (3.5V to 4.0V). See the *LED Forward Voltage Monitoring* section of this datasheet for a more detailed description of the gain selection and transition process.

For an advanced analysis, it is recommended that power consumed by the circuit (V_{IN} x I_{IN}) for a given load be evaluated rather than power efficiency.

POWER DISSIPATION

The power dissipation (P_{DISS}) and junction temperature (T_J) can be approximated with the equations below. P_{IN} is the power generated by the 3/2× - 1× charge pump, P_{LED} is the power consumed by the LEDs, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance for the µSMD 18-bump package. V_{IN} is the input voltage to the LM2755, V_{LED} is the nominal LED forward voltage, N is the number of LEDs and I_{LED} is the programmed LED current.

$$P_{DISS} = P_{IN} - P_{LED1} - P_{LED2} - P_{LED3}$$

$$P_{DISS} = (GAIN \times V_{IN} \times I_{D1 + D2 + D3}) - (V_{LED1} \times I_{LED1}) - (V_{LED2} \times I_{LED2}) - (V_{LED3} \times I_{LED3})$$

$$T_J = T_A + (P_{DISS} \times \theta_{JA})$$

The junction temperature rating takes precedence over the ambient temperature rating. The LM2755 may be operated outside the ambient temperature rating, so long as the junction temperature of the device does not exceed the maximum operating rating of 105°C. The maximum ambient temperature rating must be derated in applications where high power dissipation and/or poor thermal resistance causes the junction temperature to exceed 105°C.

THERMAL PROTECTION

Internal thermal protection circuitry disables the LM2755 when the junction temperature exceeds 160°C (typ.). This feature protects the device from being damaged by high die temperatures that might otherwise result from excessive power dissipation. The device will recover and operate normally when the junction temperature falls below 155°C (typ.). It is important that the board layout provide good thermal conduction to keep the junction temperature within the specified operating ratings.

CAPACITOR SELECTION

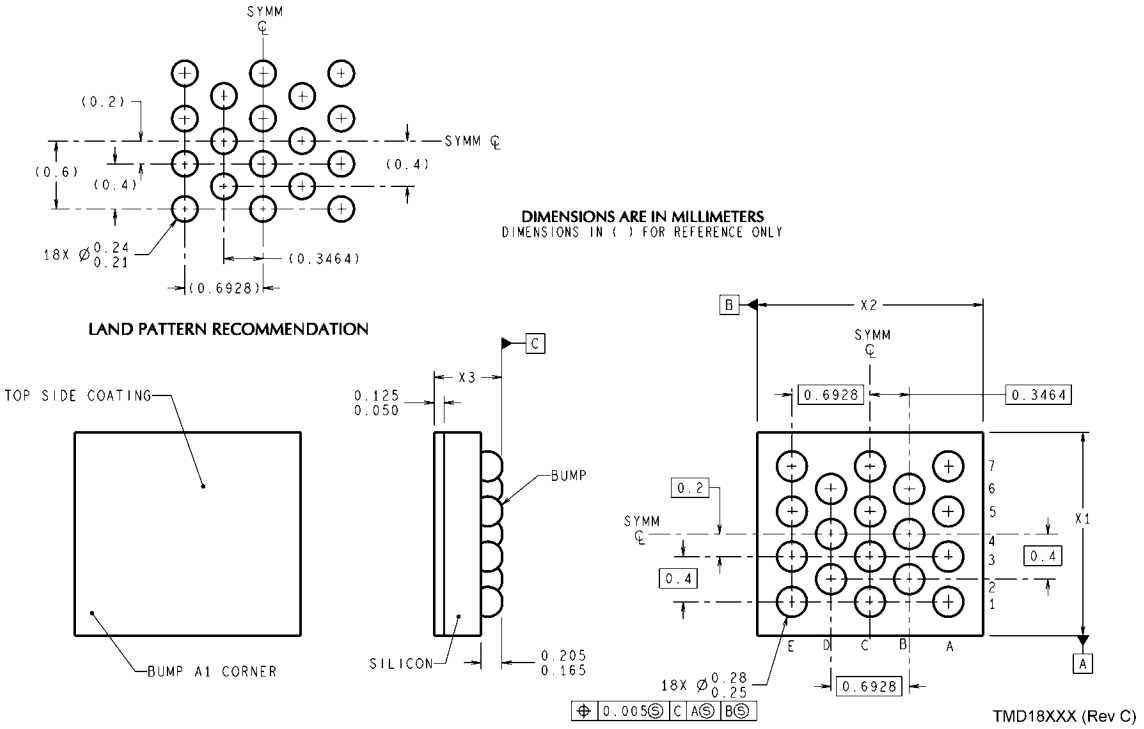
The LM2755 requires 4 external capacitors for proper operation (C_{IN} = C_{OUT} = 1µF, C_1 = C_2 = 0.47µF). Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive and have very low equivalent series resistance (ESR <20mΩ typ.). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors are not recommended for use with the LM2755 due to their high ESR, as compared to ceramic capacitors.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the LM2755. These capacitors have tight capacitance tolerance (as good as ±10%) and hold their value over temperature (X7R: ±15% over -55°C to 125°C; X5R: ±15% over -55°C to 85°C).

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the LM2755. Capacitors with these temperature characteristics typically have wide capacitance tolerance (+80%, -20%) and vary significantly over temperature (Y5V: +22%, -82% over -30°C to +85°C range; Z5U: +22%, -56% over +10°C to +85°C range). Under some conditions, a nominal 1µF Y5V or Z5U capacitor could have a capacitance of only 0.1µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM2755.

The recommended voltage rating for the capacitors is 10V to account for DC bias capacitance losses.

Physical Dimensions inches (millimeters) unless otherwise noted



TMD18AAA: 18 BUMP µSMD
X1 = 1.615mm
X2 = 1.807mm
X3 = 0.6mm

Notes

Notes

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