High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 3ns Delay
- 20ns Rise and Fall Time into 2.2nF
- 8ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for –55°C to +125°C operation. The UC2710 and UC3710 are specified for a temperature range of –40°C to +85°C and 0°C to +70°C respectively and are available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

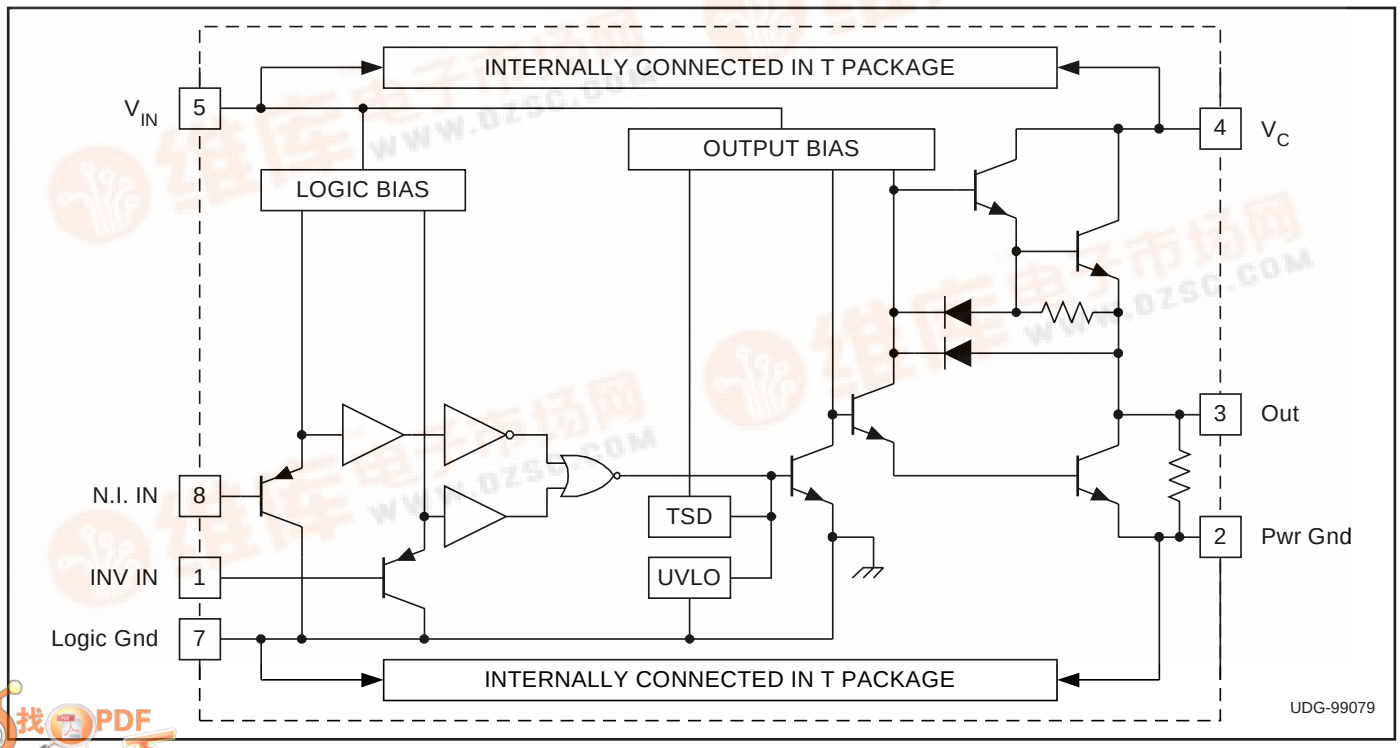
OUT= $\overline{INV}$ and N.I.

$\overline{OUT}$= INV or $\overline{N.I.}$

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1710J	–55°C to +125°C	8 pin CDIP
UC2710DW	–40°C to +85°C	16 pin SOIC-wide
UC2710J		8 pin CDIP
UC2710N		8 pin PDIP
UC2710T		5 pin TO220
UC3710DW	0°C to +70°C	16 pin SOIC-wide
UC3710N		8 pin PDIP
UC3710T		5 pin TO220

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

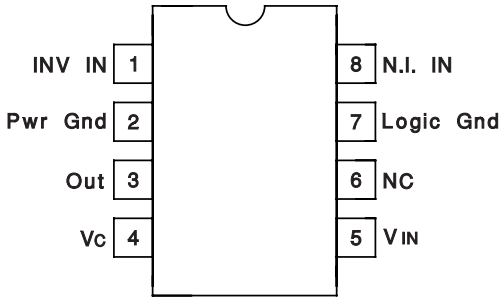
	N-Package	J-Package	T-Package
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, V_C	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	± 500mA	± 500mA	± 1A
Digital Inputs	–0.3V-V_{IN}	–0.3V – V_{IN}	–0.3V – V_{IN}
Power Dissipation at Ta=25°C	1W	1W	3W
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Operating Junction Temperature	–55°C to +150°C	–55°C to +150°C	–55°C to +150°C
Storage Temperature	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note 1: All currents are positive into, negative out of the specified terminal.

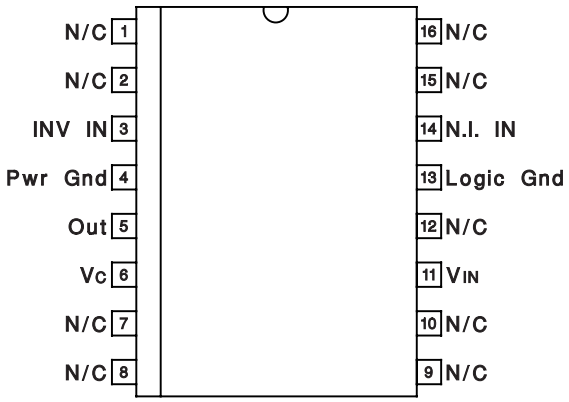
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

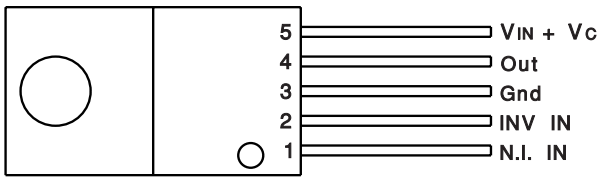
DIL-8 MINIDIP (Top View)
J or N Package



SOIC-16 (Top View)
DW Package



5-Pin TO-220 (Top View)
T Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for V_{IN} = V_C = 15V, No load, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} =18V, V_C =18V, Output Low		26	35	mA
	V_{IN} =18V, V_C =18V, Output High		21	30	mA
V_C Supply Current	V_{IN} =18V, V_C =18V, Output Low		1.5	5.0	mA
	V_{IN} =18V, V_C =18V,Output High		5.0	8	mA
UVLO Threshold	V_{IN} High to Low	3.8	4.1	4.4	V
	V_{IN} Low to High	4.1	4.4	4.8	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $V_{IN} = V_C = 15V$, No load, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V
Digital Input Current	Digital Input = 0.0V	–70	–4.0		µA
Output High Sat., $V_C – V_O$	I_O= –100mA		1.35	2.2	V
	I_O= –6A		3.2	4.5	V
Output Low Sat., V_O	I_O= 100mA		0.25	0.6	V
	I_O= 6A		3.4	4.5	V
Thermal Shutdown			165		°C
From Inv., Input to Output (Note 3, 4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 3,4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns
Total Supply Current at 200kHz Input Switching Frequency	T_A = 25°C (Note 5) CL = 0		30	40	mA

Note: 3. Delay measured from 50% input change to 10% output change.

Note: 4. Those parameters with CL = 30nF are not tested in production.

Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-0152001QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-0152001VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
5962-0152001VXA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1710J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1710J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type
UC1710L883B	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
UC1710SP	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2710N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2710NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2710T	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type
UC2710TG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type
UC3710DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3710DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3710N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3710NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3710T	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type
UC3710TG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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