FAIRCHILD

SEMICONDUCTOR ™

October 1992
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74VHC74
Dual D-Type Flip-Flop with Preset and Clear

General Description

The VHC74 is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D input is transferred to the Q output during the positive going transition of the CK pulse. $\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input LOW.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

■ High Speed: f_{MAX} = 170 MHz (typ) at T_A = 25°C
■ High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
■ Power down protection is provided on all inputs
■ Low power dissipation: I_{CC} = 2 μA (max) at T_A = 25°C
■ Pin and function compatible with 74HC74

Ordering Code:

Order Number	Package Number	Package Description
74VHC74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74VHC74SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
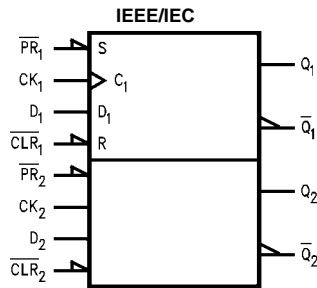
Connection Diagram
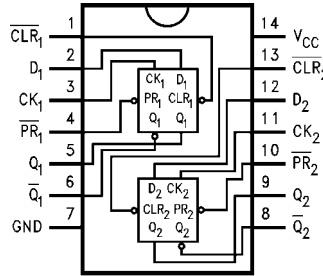
Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Output

Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H (Note 1)	H (Note 1)	
H	H	L	╱	L	H	
H	H	H	╱	H	L	
H	H	X	╲	Q_n	Q_n	No Change

Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) state.

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Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading varaibles. Fairchild does not recommend operation outside databook specifications.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	2.0	1.50			1.50		V		
		3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	2.0			0.50		0.50	V		
		3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −50 µA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 50 µA
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	µA	$V_{IN} = V_{CC}$ or GND	

AC Electrical Characteristics

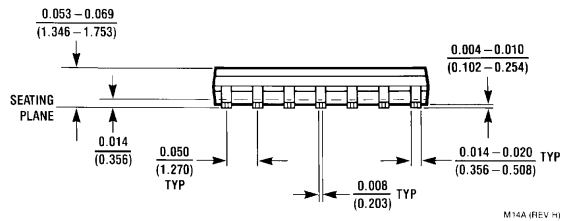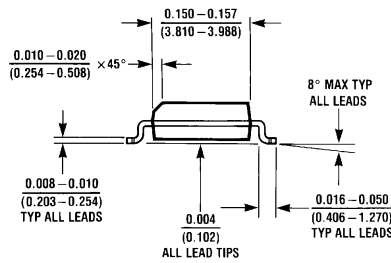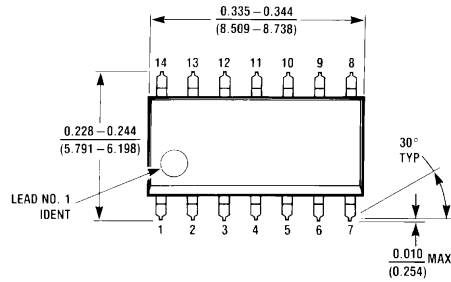| Symbol	Parameter	V_CC (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
f_MAX	Maximum Clock	3.3 ± 0.3	80	125		70		MHz	C_L = 15 pF
	Frequency		50	75		45			C_L = 50 pF
		5.0 ± 0.5	130	170		110		MHz	C_L = 15 pF
			90	115		75			C_L = 50 pF
t_PLH	Propagation Delay	3.3 ± 0.3		6.7	11.9	1.0	14.0	ns	C_L = 15 pF
t_PHL	Time (CK-Q, $\overline{Q}$)			9.2	15.4	1.0	17.5		C_L = 50 pF
		5.0 ± 0.5		4.6	7.3	1.0	8.5	ns	C_L = 15 pF
				6.1	9.3	1.0	10.5		C_L = 50 pF
t_PLH	Propagation Delay Time	3.3 ± 0.3		7.6	12.3	1.0	14.5	ns	C_L = 15 pF
t_PHL	($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)			10.1	15.8	1.0	18.0		C_L = 50 pF
		5.0 ± 0.5		4.8	7.7	1.0	9.0	ns	C_L = 15 pF
				6.3	9.7	1.0	11.0		C_L = 50 pF
C_IN	Input Capacitance			4	10		10	pF	V_CC = Open
C_PD	Power Dissipation Capacitance			25				pF	(Note 4)

Note 4: C_PD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/2$ (per F/F).

AC Operating Requirements

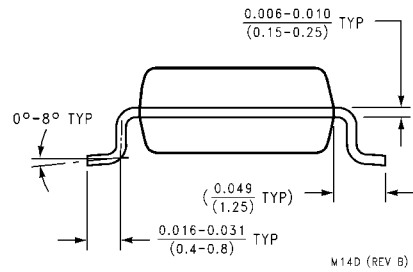| Symbol	Parameter	V_CC (V) (Note 5)	T_A = 25°C	T_A = −40°C to +85°C	Units
			Typ	Guaranteed Minimum	
t_W(L)	Minimum Pulse Width (CK)	3.3		6.0	7.0	ns
t_W(H)		5.0		5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_H	Minimum Hold Time	3.3		0.5	0.5	ns
		5.0		0.5	0.5	
t_REC	Minimum Recovery Time ($\overline{CLR}$, $\overline{PR}$)	3.3		5.0	5.0	ns
		5.0		3.0	3.0	

Note 5: V_CC is 3.3 ± 0.3V or 5.0 ± 0.5V

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Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A

14   8

0.295 − 0.319
(7.5 − 8.1)

0.205 − 0.213
(5.2 − 5.4)

1   7

0.394 − 0.402
(10.0 − 10.2)

(0.71
(1.8))

0.067 − 0.083
(1.7 − 2.1)

0.006 − 0.010
(0.15 − 0.25) TYP

⬓ 0.006 (0.15)

SEATING PLANE

0.050
(1.27) TYP

0.014 − 0.020
(0.35 − 0.50) TYP

0.000 − 0.010
(0 − 0.25)

0° − 8° TYP

(0.049
(1.25) TYP)

0.016 − 0.031
(0.4 − 0.8) TYP
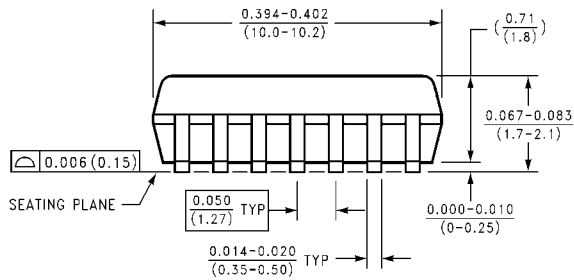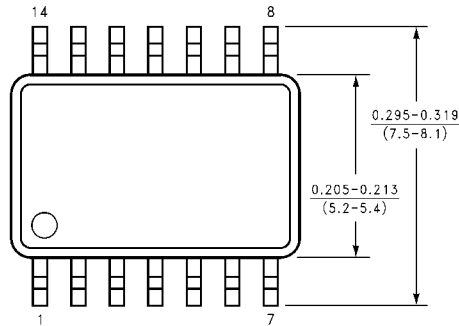
M14D (REV B)

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

74VHC74 Dual D-Type Flip-Flop with Preset and Clear

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

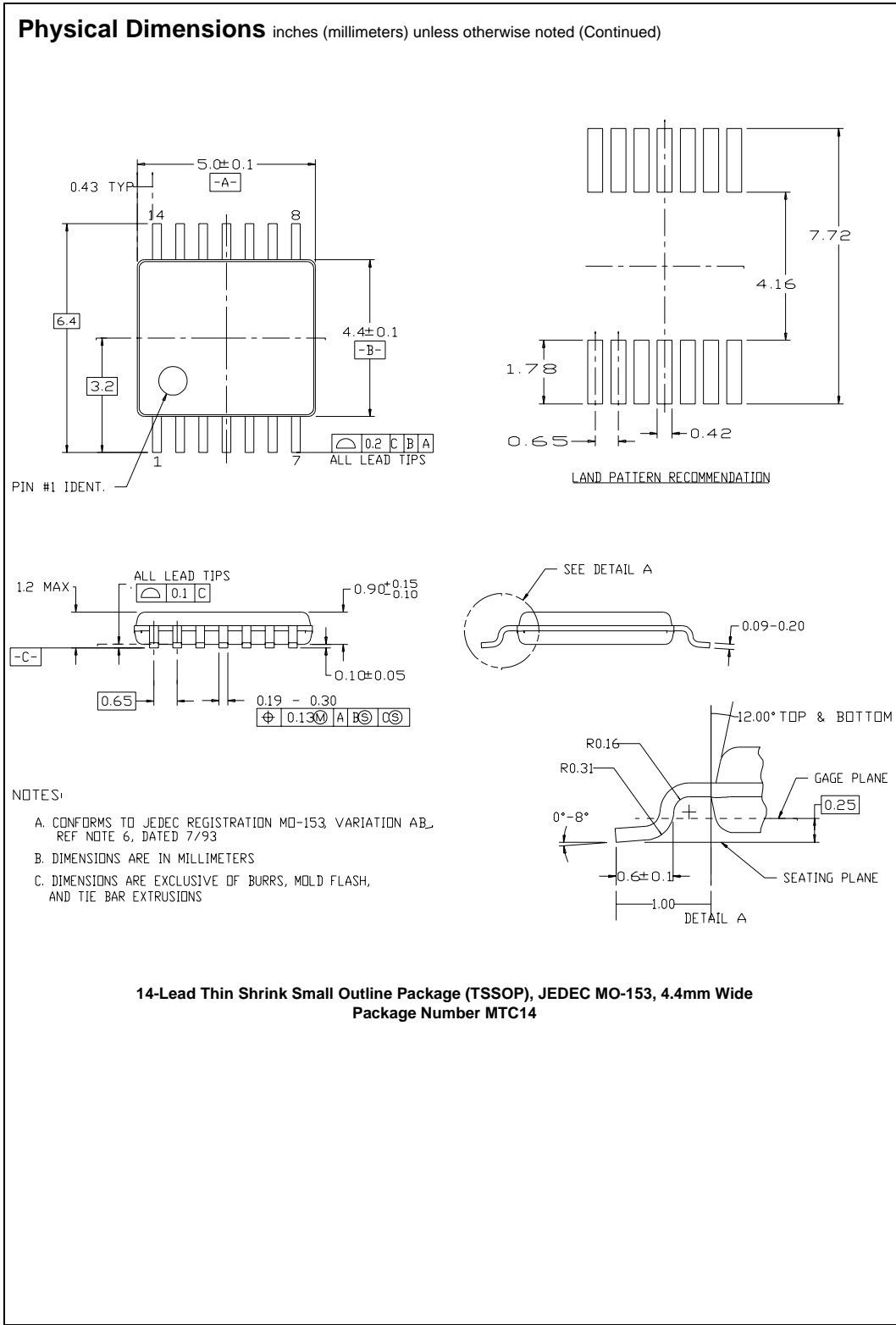0.740 − 0.770
(18.80 − 19.56)

0.090
(2.286)

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

0.092 DIA
(2.337)

0.030 MAX
(0.762) DEPTH

OPTION 1

INDEX
AREA

PIN NO. 1
IDENT

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060 TYP
(1.524)

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 − 0.023 TYP
(0.356 − 0.584)

0.100 ± 0.010 TYP
(2.540 ± 0.254)

0.050 ± 0.010 TYP
(1.270 − 0.254)

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016 TYP
(0.203 − 0.406)

0.280
(7.112)
MIN

0.325 +0.040 −0.015

(8.255 +1.016 −0.381)

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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