NIPPON PRECISION CIRCUITS LTD.

SM5834AG

General-purpose High-speed FIR Digital Filter

OVERVIEW

The SM5834AG is an FIR digital filter fabricated in Molygate® CMOS for video signal processors.

The SM5834AG processes 10-bit signal data using mathematical blocks set by 10-bit coefficient data. It comprises six 10 × 10-bit multipliers and eleven 16-bit adders, enabling it to be configured as a single-chip, asymmetrical 6-tap filter or a symmetrical 11-tap filter. Several devices can be cascaded to realize longer filters.

The filter coefficients are stored in six programmable registers which can be updated during normal operation. The maximum signal sampling frequency is 25 MHz.

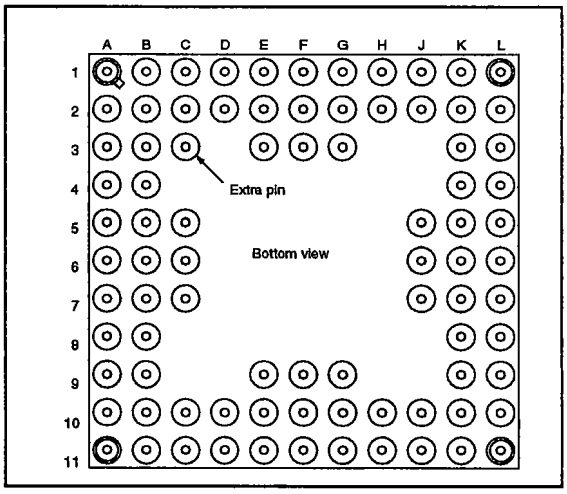
FEATURES

- Filter configuration
  - Asymmetrical 6-tap FIR filter (Mode I)
  - Symmetrical 11-tap FIR filter (Mode II)
  - Devices can be cascaded for longer filters
- Data format
  - 10-bit 2s-complement input data
  - 10-bit 2s-complement coefficient data
  - 16-bit 2s-complement internal processing
- 25 MHz maximum sampling rate
- Arithmetic blocks
  - Six 10 × 10-bit → 16-bit multipliers
  - Six 10-bit coefficient buffers
  - Six 10-bit coefficient registers
  - Eleven 16 + 16-bit → 16-bit adders
- 25 MHz throughput rate with fixed coefficients, and 20 MHz with adaptive coefficients
- Coefficient registers can be read.
- Two-tier coefficient registers for synchronized update
- Support for 8-bit bus interface
- Overflow detect function
- TTL-compatible input/outputs
- 5 ±0.5 V supply
- 84-pin PGA (pin-grid array)
- Molygate® CMOS process

APPLICATIONS

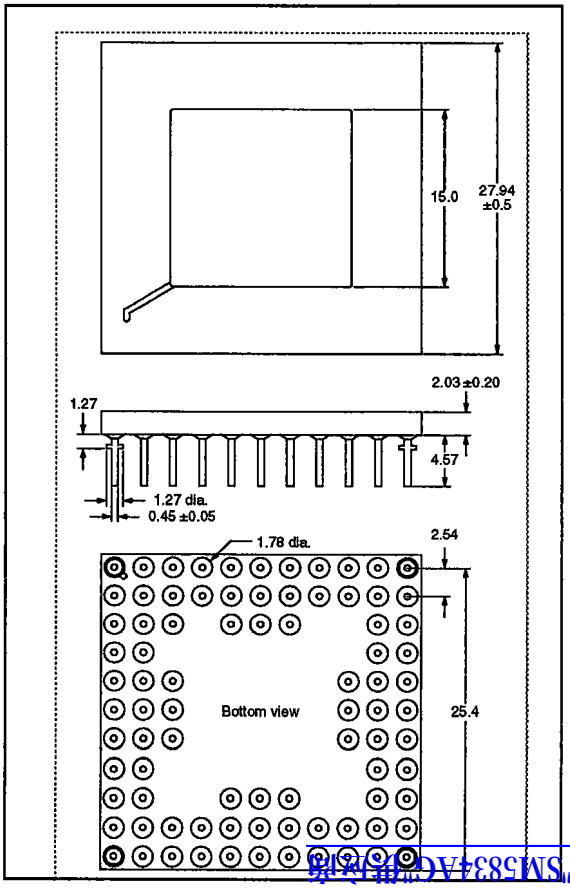
- Digital VCR filters

PINOUT

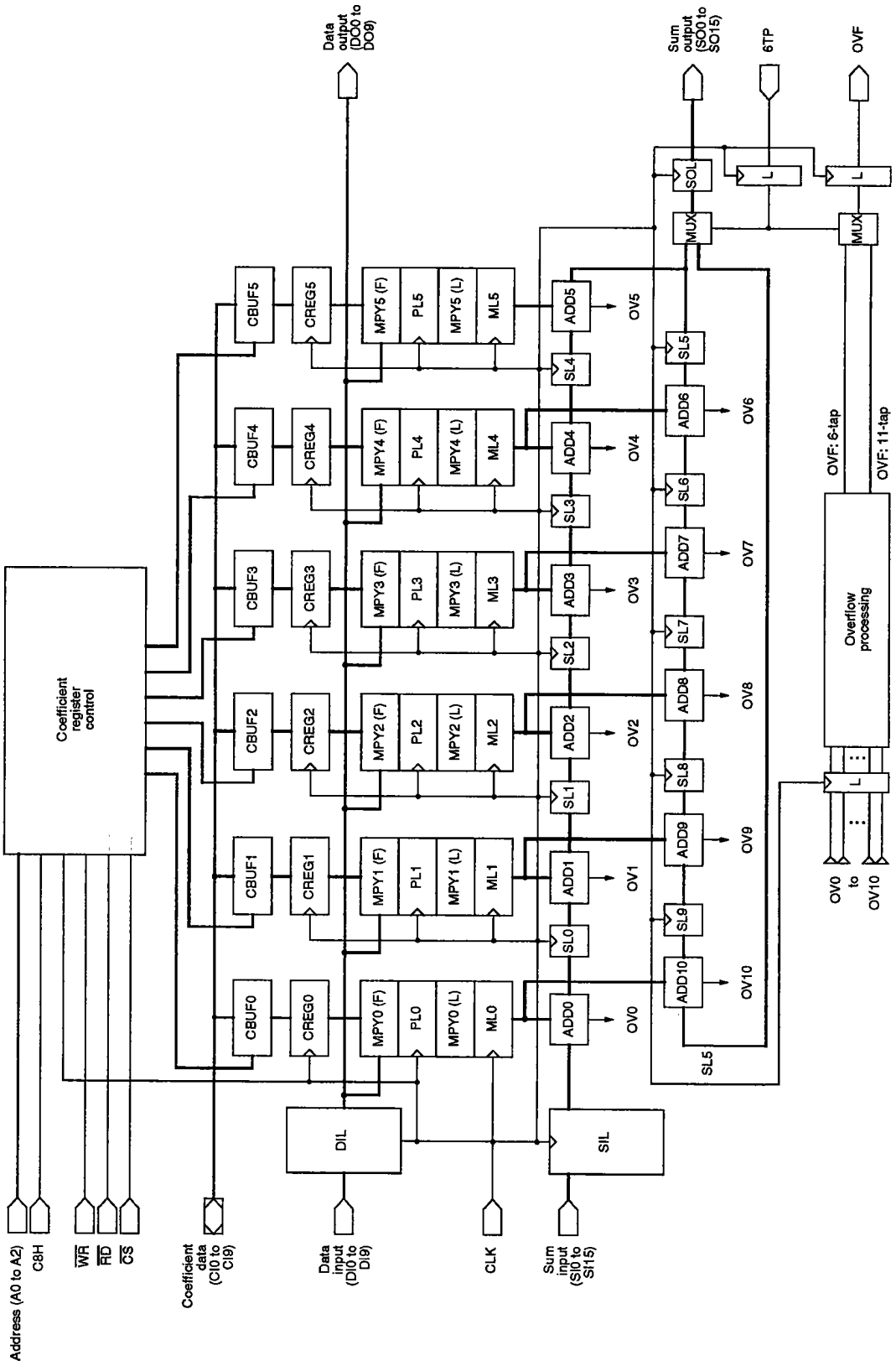


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Pin Number	Name	I/O	Description
1	B2	DI0	ip	Signal data input bit 0 (LSB)
2	C2	DI1	ip	Signal data input bit 1
3	B1	DI2	ip	Signal data input bit 2
4	C1	DI3	ip	Signal data input bit 3
5	D2	DI4	ip	Signal data input bit 4
6	D1	DI5	ip	Signal data input bit 5
7	E3	DI6	ip	Signal data input bit 6
8	E2	DI7	ip	Signal data input bit 7
9	E1	DI8	ip	Signal data input bit 8
10	F2	DI9	ip	Signal data input bit 9 (MSB)
11	F3	VSS1		Ground
12	G3	VDD1		5 V supply
13	G1	DO9	o	Signal data output bit 9 (MSB)
14	G2	DO8	o	Signal data output bit 8
15	F1	DO7	o	Signal data output bit 7
16	H1	DO6	o	Signal data output bit 6
17	H2	DO5	o	Signal data output bit 5
18	J1	DO4	o	Signal data output bit 4
19	K1	DO3	o	Signal data output bit 3
20	J2	DO2	o	Signal data output bit 2
21	L1	NC		No connection
22	K2	NC		No connection
23	K3	NC		No connection
24	L2	DO1	o	Signal data output bit 1
25	L3	DO0	o	Signal data output bit 0 (LSB)
26	K4	SO15	o	Sum output bit 15 (MSB)
27	L4	SO14	o	Sum output bit 14
28	J5	SO13	o	Sum output bit 13
29	K5	SO12	o	Sum output bit 12
30	L5	SO11	o	Sum output bit 11
31	K6	SO10	o	Sum output bit 10
32	J6	VSS2		Ground
33	J7	VDD2		5 V supply
34	L7	SO9	o	Sum output bit 9
35	K7	SO8	o	Sum output bit 8
36	L6	SO7	o	Sum output bit 7

Number	Pin Number	Name	I/O	Description
37	L8	SO6	o	Sum output bit 6
38	K8	SO5	o	Sum output bit 5
39	L9	SO4	o	Sum output bit 4
40	L10	SO3	o	Sum output bit 3
41	K9	SO2	o	Sum output bit 2
42	L11	NC		No connection
43	K10	SO1	o	Sum output bit 1
44	J10	SO0	o	Sum output bit 0 (LSB)
45	K11	OVF	o	Overflow detect (active-HIGH)
46	J11	SI0	ip	Cascade sum input bit 0 (LSB)
47	H10	SI1	ip	Cascade sum input bit 1
48	H11	SI2	ip	Cascade sum input bit 2
49	F10	SI3	ip	Cascade sum input bit 3
50	G10	SI4	ip	Cascade sum input bit 4
51	G11	SI5	ip	Cascade sum input bit 5
52	G9	SI6	ip	Cascade sum input bit 6
53	F9	SI7	ip	Cascade sum input bit 7
54	F11	VSS3		Ground
55	E11	VDD3		5 V supply
56	E10	SI8	ip	Cascade sum input bit 8
57	E9	SI9	ip	Cascade sum input bit 9
58	D11	SI10	ip	Cascade sum input bit 10
59	D10	SI11	ip	Cascade sum input bit 11
60	C11	SI12	ip	Cascade sum input bit 12
61	B11	SI13	ip	Cascade sum input bit 13
62	C10	SI14	ip	Cascade sum input bit 14
63	A11	SI15	ip	Cascade sum input bit 15
64	B10	6TP	ip	Filter tap number select. 6-tap asymmetrical mode when HIGH and 11-tap symmetrical mode when LOW
65	B9	VSS4		Ground
66	A10	$\overline{CS}$	i	Chip select
67	A9	$\overline{RD}$	i	Coefficient read signal
68	B8	$\overline{WR}$	i	Coefficient write signal
69	A8	C8H	ip	Coefficient high-order byte select. High byte when C8H = HIGH
70	B6	A2	ip	Coefficient register address bit 2
71	B7	A1	ip	Coefficient register address bit 1
72	A7	A0	ip	Coefficient register address bit 0

Number	Pin Number	Name	I/O	Description
73	C7	CLK	i	Clock input
74	C6	CI9	io	Coefficient data input/output bit 9 (MSB)
75	A6	CI8	io	Coefficient data input/output bit 8
76	A5	CI7	io	Coefficient data input/output bit 7
77	B5	CI6	io	Coefficient data input/output bit 6
78	C5	CI5	io	Coefficient data input/output bit 5
79	A4	CI4	io	Coefficient data input/output bit 4
80	B4	CI3	io	Coefficient data input/output bit 3
81	A3	CI2	io	Coefficient data input/output bit 2
82	A2	CI1	io	Coefficient data input/output bit 1
83	B3	CI0	io	Coefficient data input/output bit 0 (LSB)
84	A1	VDD4		5 V supply

Note

i = input, ip = input with pull-down resistance, o = output, io = input/output

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_W	1.2	W
Storage temperature range	T_{stg}	–40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.75 to 5.25	V
Operating temperature range	T_{opr}	–20 to 70	deg. C

DC Electrical Characteristics

V_{DD} = 4.75 to 5.25 V, T_a = –20 to 70 deg. C, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby current consumption	I_S	V_{IN} = V_{DD} or 0 V	–	–	10.0	µA
Operating current consumption	I_{DD}	V_{DD} = 5 V, f = 25 MHz, all outputs open	–	–	200	mA
HIGH-level input voltage	V_{IH}	See notes 1 and 2.	2.4	–	–	V
LOW-level input voltage	V_{IL}	See note 3.	–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –0.4 mA. See note 3.	2.5	–	–	V
		I_{OH} = –1.0 mA. See note 4.	2.5	–	–	
LOW-level output voltage	V_{OL}	I_{OL} = 1.6 mA. See note 3.	–	–	0.4	V
		I_{OL} = 4.0 mA. See note 4.	–	–	0.4	
HIGH-level input current	I_{IH}	V_{IN} = V_{DD}. See note 2.	–	10	20	µA
HIGH-Level input leakage current	I_{LH}	V_{IN} = V_{DD}. See note 1.	–	–	1.0	µA
LOW-level input leakage current	I_{LL}	V_{IN} = 0 V. See notes 1 and 2.	–	–	1.0	µA
High-impedance HIGH-level output leakage current	I_{ZH}	$V_{\overline{RD}}$ = V_{IH}, V_{OUT} = V_{DD}	–	–	5.0	µA
High-impedance LOW-level output leakage current	I_{ZL}	$V_{\overline{RD}}$ = V_{IH}, V_{OUT} = 0 V	–	–	5.0	µA

Notes

1. Pins CLK, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ are TTL-level inputs.
2. Pins SI0 to SI15, DI0 to DI9, 6TP, C8H and A0 to A2 are TTL-level inputs with pull-down resistances.
3. Pins CI0 to CI9 are TTL-level input/outputs.
4. Pins SO0 to SO15, DO0 to DO9, and OVF are TTL-level outputs.

AC Electrical Characteristics

V_{DD} = 4.75 to 5.25 V, T_a = –20 to 70 deg. C, V_{SS} = 0 V unless otherwise noted

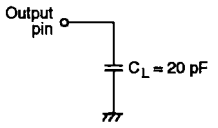
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{CLK}	Fixed coefficients	1	–	25	MHz
		Adaptive coefficients	1	–	20	
Clock LOW-level pulsewidth	t_{PWL}	See figure 1.	15	–	–	ns
Clock HIGH-level pulsewidth	t_{PWH}		15	–	–	ns
Clock rise time	t_r		–	–	100	ns
Clock fall time	t_f		–	–	100	ns
DI0 to DI9 data input setup time	t_{S1}	See figure 2.	10	–	–	ns
DI0 to DI9 data input hold time	t_{H1}		5	–	–	ns

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
SI0 to SI15 sum input setup time	t_{S2}	See figure 3.	10	–	–	ns
SI0 to SI15 sum input hold time	t_{H2}		3	–	–	ns
CLK to DO*n* data output delay time	t_{PD1}	See figure 4. See note 5.	–	–	25	ns
CLK to DO*n* data output hold time	t_{OH1}		8	–	–	ns
CLK to SO*n* sum output delay time	t_{PD2}	See figure 5. See note 5.	–	–	27	ns
CLK to SO*n* sum output hold time	t_{OH2}		8	–	–	ns
CLK to OVF overflow output delay time	t_{PD3}	See figure 6. See note 5.	–	–	25	ns
CLK to OVF overflow output hold time	t_{OH3}		8	–	–	ns
Write cycle time	t_{WC}	See figure 7.	50	–	–	ns
$\overline{WR}$ write clock pulsewidth	t_{PW2}		25	–	–	ns
CI0 to CI9 coefficient data setup time	t_{S3}		5	–	–	ns
CI0 to CI9 coefficient data hold time	t_{H3}		15	–	–	ns
A0 to A2 and $\overline{CS}$ address setup time	t_{S4}		5	–	–	ns
A0 to A2 and $\overline{CS}$ address hold time	t_{H4}		5	–	–	ns
C8H high-byte setup time	t_{S5}		15	–	–	ns
C8H high-byte hold time	t_{H5}		15	–	–	ns
Read cycle time	t_{RC}	See figure 8. See note 6.	100	–	–	ns
A0 to A2 address access time	t_{AA}		–	–	80	ns
$\overline{CS}$ chip select access time	t_{ACS}		–	–	80	ns
C8H high-byte access time	t_{AC8H}		–	–	80	ns
A0 to A2 coefficient output hold time	t_{OH4}		8	–	–	ns
C8H coefficient output hold time	t_{OH5}		8	–	–	ns
$\overline{RD}$ coefficient output enable, output delay time (low impedance)	t_{OLZ}	See figure 8. See note 6.	8	–	–	ns
$\overline{CS}$ coefficient output enable, output delay time (low impedance)	t_{CLZ}		8	–	–	ns
$\overline{RD}$ to CI*n* coefficient output enable, output delay time	t_{OE}		–	–	90	ns
$\overline{RD}$ coefficient output disable, output delay time	t_{OHZ}	See figure 8. See note 6.	–	–	30	ns
$\overline{CS}$ coefficient output disable, output delay time	t_{CHZ}		–	–	35	ns

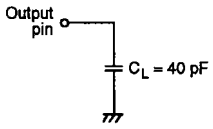
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Input capacitance	C_{IN}	f = 1 MHz. See notes 1 and 2.	–	–	10	pF
Input/output capacitance	C_{IO}	f = 1 MHz, $V_{\overline{RD}} = V_{IH}$	–	–	20	pF

Notes

1. Pins CLK, $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ are TTL-level inputs.
2. Pins SI0 to SI15, DI0 to DI9, 6TP, C8H and A0 to A2 are TTL-level inputs with pull-down resistances.
3. Pins CI0 to CI9 are TTL-level input/outputs.
4. Typical values are measured at V_{DD} = 5 V and T_a = 25 deg. C
5. Measurement circuit 1



6. Measurement circuit 2



Timing Diagrams

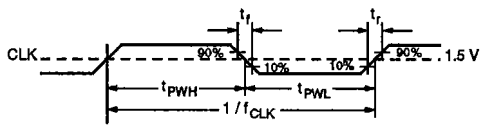


Figure 1. Clock input waveform

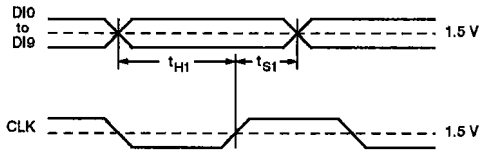


Figure 2. Data input timing

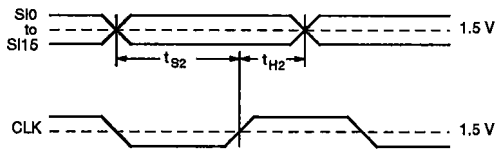


Figure 3. Sum input timing

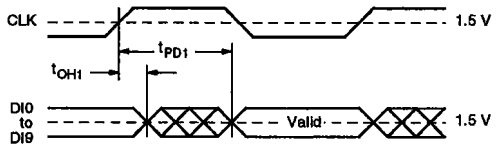


Figure 4. Data output timing

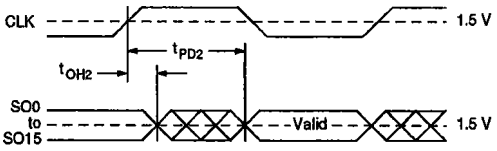


Figure 5. Sum output timing

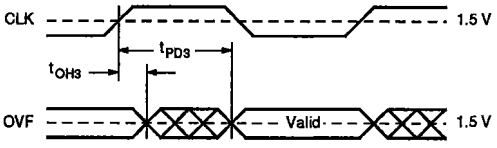


Figure 6. Overflow output timing

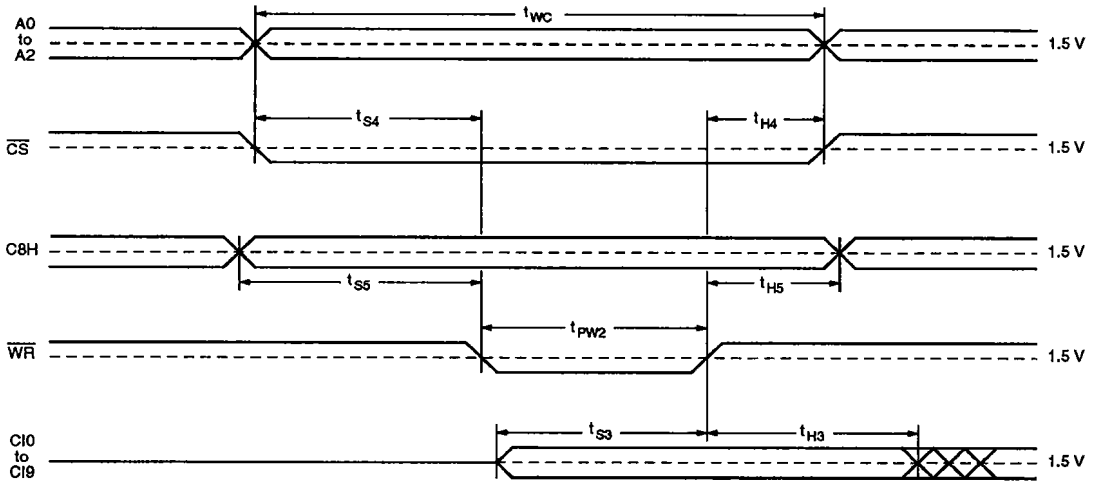


Figure 7. Coefficient write timing

Note
$\overline{RD}$ should be held HIGH during the write cycle.

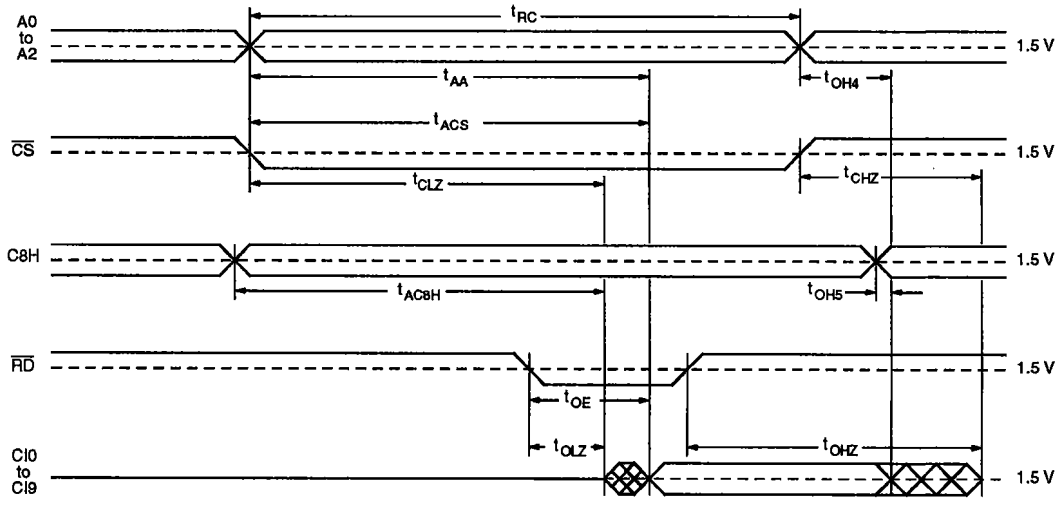


Figure 8. Coefficient read timing

Note
$\overline{WR}$ should be held HIGH during the read cycle.

FUNCTIONAL DESCRIPTION

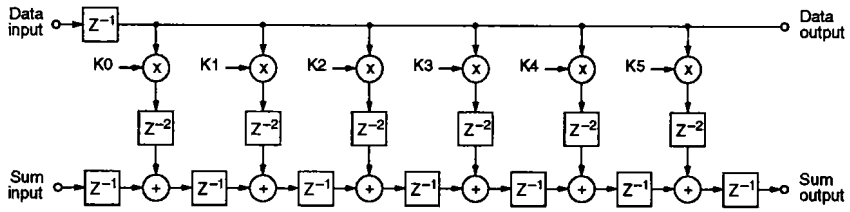
Filter Type Select

The SM5834AG can be configured as a symmetrical filter—with filter coefficients symmetrical about the center tap—or an asymmetrical filter as shown in the following table.

Mode	6TP	Filter configuration
I	HIGH	Asymmetrical 6-tap FIR filter
II	LOW	Symmetrical 11-tap FIR filter

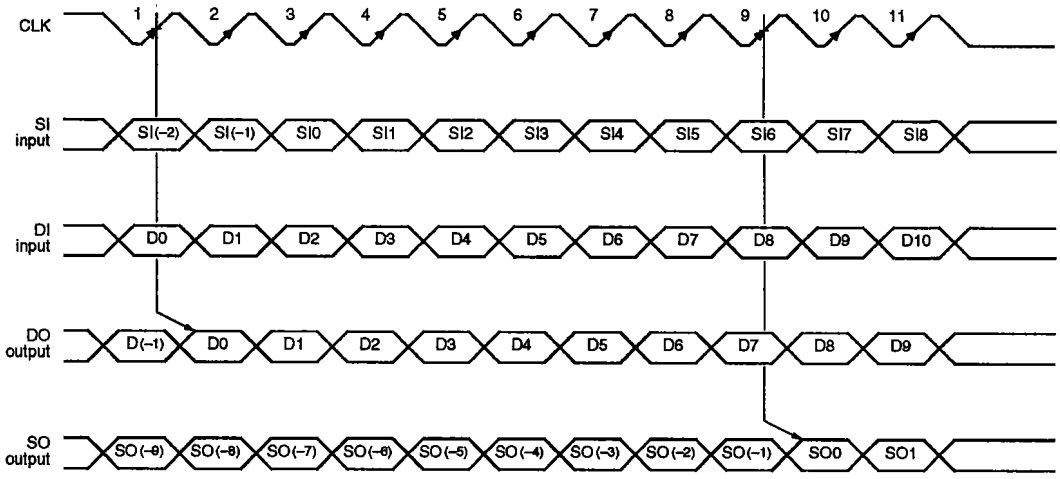
Mode I

Flow diagram



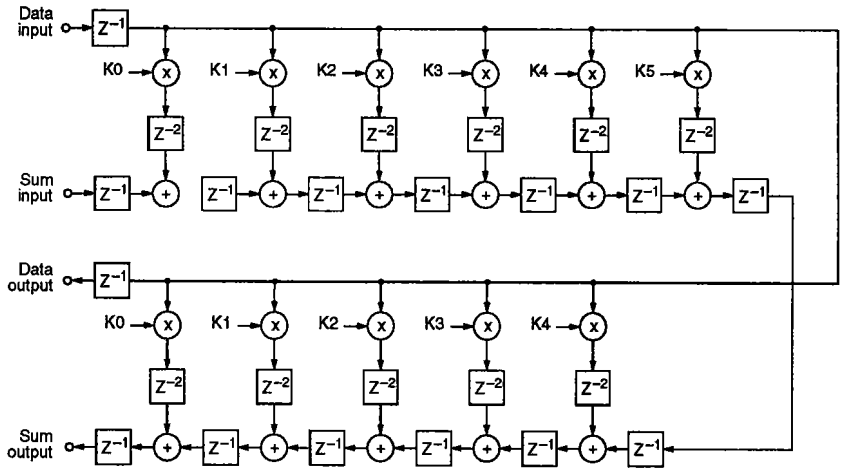
$$SO(n) = SI(n) + \sum_{m=0}^{5} [Km \times D(n + m)]$$

Timing diagram



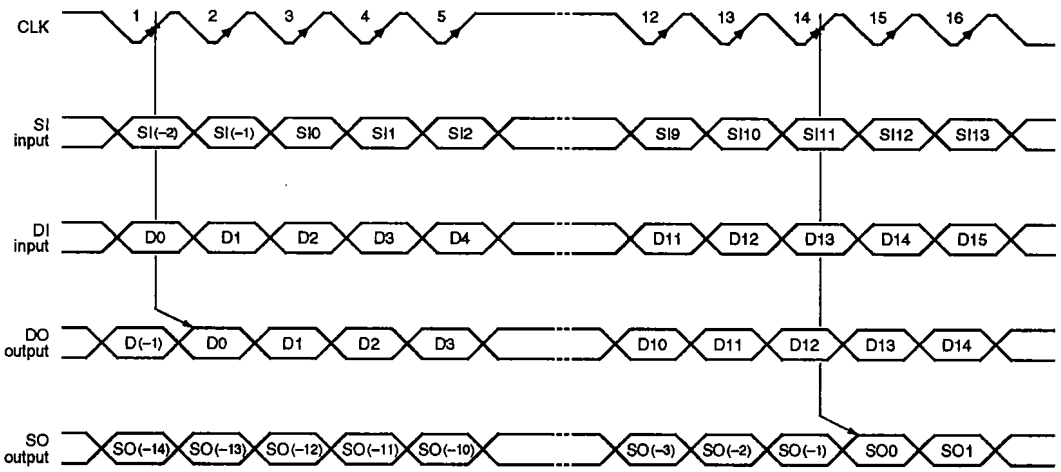
Mode II

Flow diagram



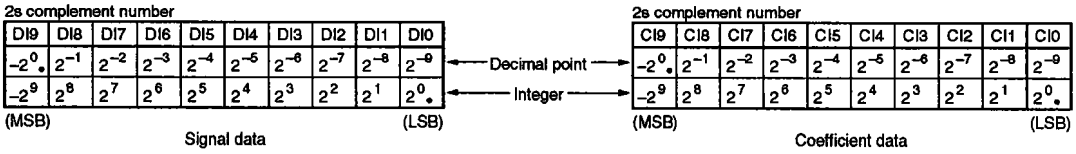
$$SO(n) = SI(n) + \sum_{m=0}^{5} [Km \times D(n + m)] + \sum_{m=4}^{0} [Km \times D(n + 10 - m)]$$

Timing diagram



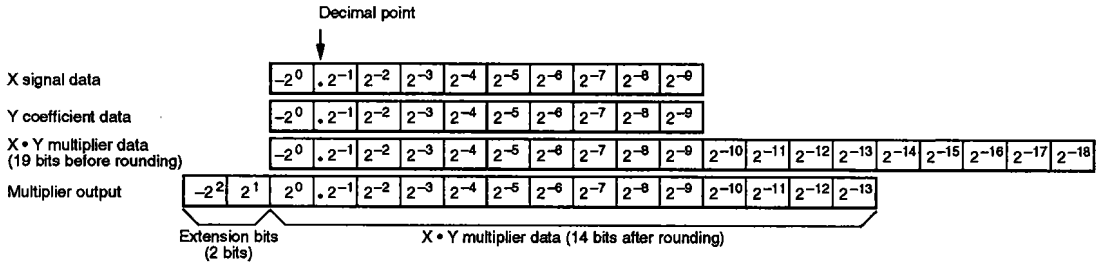
Signal Data and Coefficient Data Format

The filter input data, signal data output and coefficient input/output data all use the same 10-bit 2s-complement format.



Multiplier Input/Output Data

The multipliers multiply 10-bit signal data by 10-bit coefficient data to produce a 16-bit internal result. The following figures show the relationship between the input data, coefficient data and output data.



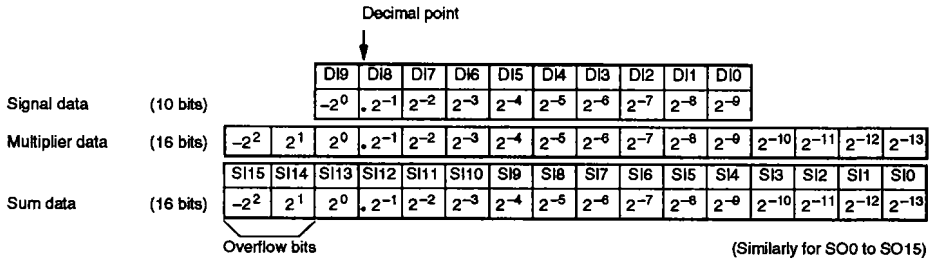
The five least-significant bits from the multiplier output are rounded off. The multiplier output sign bit is extended into the extended-precision bits.

Note

If both the signal data and coefficient data are set to –1 (the maximum negative value), then an overflow will occur and an incorrect result will be produced. Accordingly, do not set any coefficients to –1.

Adder Arithmetic Data Format

All internal arithmetic operations are performed using 16-bit 2s-complement format.



The range of the sum result before overflow is ($-4 < SUM < 4 - 2^{-13}$)

Overflow Detect Function (OVF)

If an overflow occurs in any of the adders, the OVF output flag goes HIGH. All adder overflow outputs are ORed synchronously, so the OVF flag does not necessarily go HIGH at the same time as the sum output resulting from the erroneous data. The corresponding sum output can be any of the six (in asymmetric filter mode) or eleven (in symmetric filter mode) outputs, starting from the one that was output immediately before OVF went HIGH. The shaded regions indicate the outputs that could be in error.

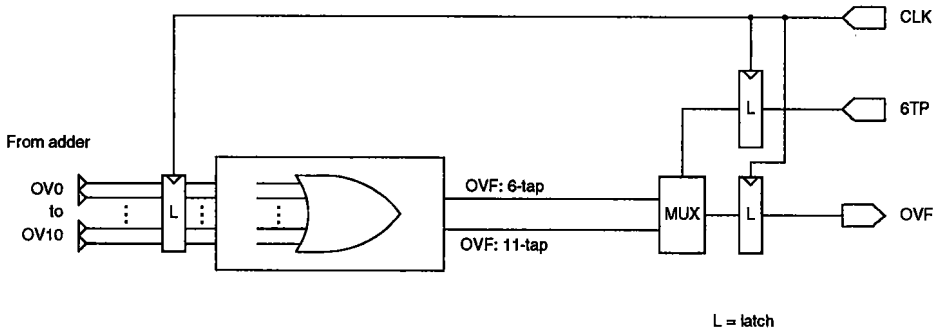


Figure 9. Overflow processor block diagram

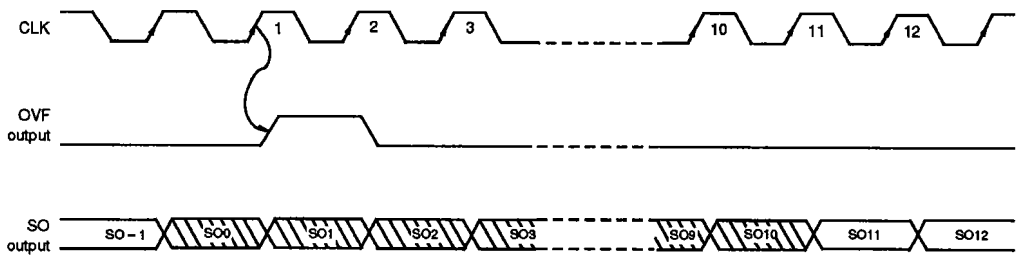


Figure 10. OVF and sum output relation

Programming Coefficient Data

The SM5834AG employs a buffered coefficient register architecture to enable simultaneous update of all coefficients. This enables smooth frequency response changes in applications such as adaptive filters. Changing the filter coefficients thus involves two steps: writing to the coefficient buffers, and updating the coefficient registers with the buffer contents.

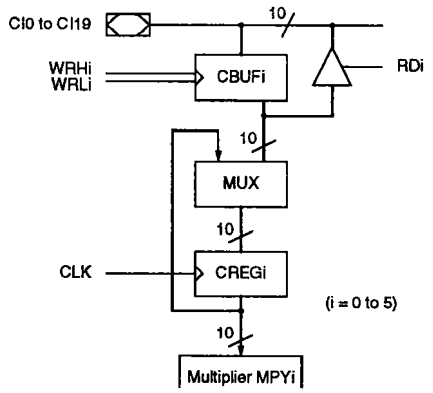


Figure 11. Coefficient bus interface

Writing to the coefficient buffer

To write to the coefficient buffers, the address lines A0 to A2 are first used to select one of the six buffers, CBUF0 to CBUF5. The $\overline{CS}$ and $\overline{WR}$ strobes are then used to write the data on C0 to C9 into the selected buffer. C8H should be kept LOW during this time.

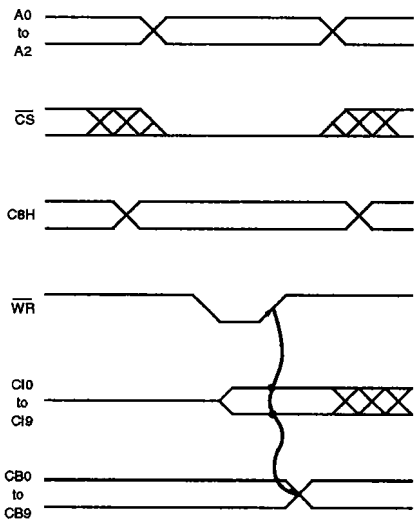


Figure 12. Coefficient write

Reading from the coefficient buffer

To read from the coefficient buffers, A0 to A2 are used to select one of the six buffers, then the $\overline{CS}$ and $\overline{WR}$ strobes are used to read data from the selected buffer. C8H should be kept LOW during this time.

Note that it is the coefficient buffers which are read, not the coefficient registers.

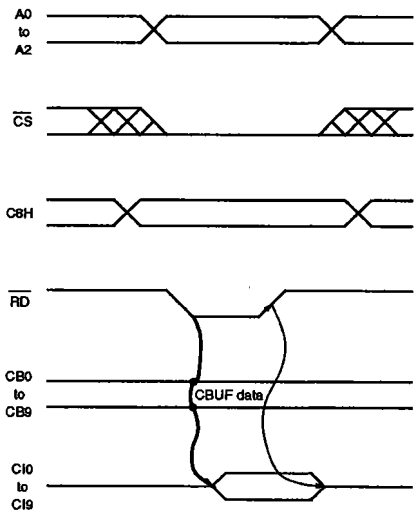


Figure 13. Coefficient read

Updating Coefficient registers

To update a register, A0 to A2 are all set HIGH and then a coefficient write cycle is performed. This simultaneously updates all coefficient registers with the values in the corresponding buffers. At least two clock cycles must elapse before the registers can be updated again.

Table 1. Coefficient buffer addresses

A2	A1	A0	Selected registor or operation
LOW	LOW	LOW	CBUF0
LOW	LOW	HIGH	CBUF1
LOW	HIGH	LOW	CBUF2
LOW	HIGH	HIGH	CBUF3
HIGH	LOW	LOW	CBUF4
HIGH	LOW	HIGH	CBUF5
HIGH	HIGH	HIGH	Update coefficient registers

Coefficient high-byte select function

The C8H pin allows the SM5834AG to be connected to an 8-bit bus. When C8H is HIGH, the two least-significant bits of the coefficient input/output bus (CI0 and CI1) correspond to the top two bits of the buffer data (CB8 and CB9). Note that on a buffer read, CB9 is extended into bits 2 through 7 of the output data (CI2 to CI7).

Table 2. Writing to the coefficient buffer high-order byte (C8H = HIGH)

CBUF bit	CBUF data
CB9	CI1
CB8	CI0
CB7 to CB0	Can't write

Table 3. Reading from the coefficient buffer high-order byte (C8H = HIGH)

CI bit	CI output data
CI9	CB9
CI8	CB8
CI7 to CI2	CB9
CI1	CB9
CI0	CB8

8-bit bus read/write

Writing to (or reading from) the coefficient buffer when connected to an 8-bit bus is simply a matter of performing two consecutive writes (or reads), changing the level on the C8H pin between read or write strobes. Figures 14 and 15 illustrate the timing of this process.

In this example, the data read or written is 3FCH. Note the output value of FFH when the high byte is read, due to extension of bit 9 into the output word.

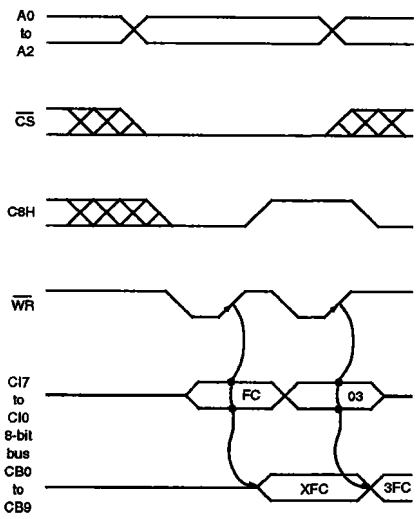


Figure 14. Coefficient write to 8-bit bus

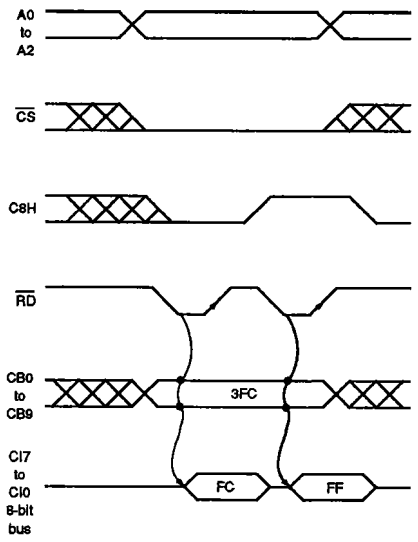


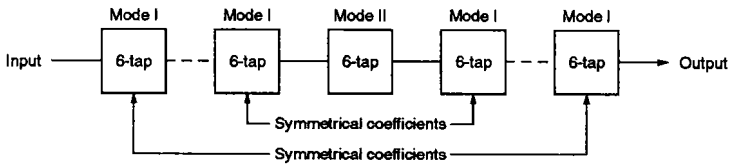
Figure 15. Coefficient read from 8-bit bus

Casade Connection

Two or more SM5834AGs can be cascaded to realize longer filters. For cascade connection, the sum outputs (SO0 to SO15) of each device are connected to the sum inputs (SI0 to SI15) of the next device. Similarly, the data outputs (DO0 to DO9) of each device are connected to the data inputs (DI0 to DI9) of the next device. The coefficients of each device are programmed by connecting each $\overline{CS}$ input to individual chip select lines.

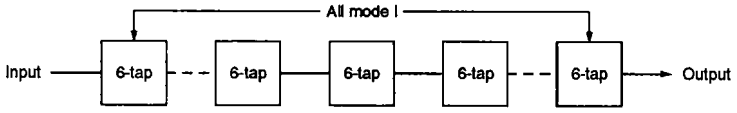
Symmetrical filter configuration

The center device in the chain in configured as a symmetrical 11-tap filter, and the remainder as asymmetrical 6-tap filters.



Asymmetrical filter configuration

All devices are configured as asymmetrical 6-tap filters.



Filter Coefficient Limitations

Although each adder has two extended-precision bits to allow for an increase in gain, the possibility of overflow in the adders increases for longer filters.

The range of permissible filter coefficients is

$$-1 \leq Ci \leq 1 - 2^{-9} \quad (0 \leq i \leq N - 1)$$

where N is the number of filter taps.

The sum result range before overflow is

$$D_{max} \times \sum_{i=0}^{N-1} |Ci| \leq 4 - 2^{-13}$$

assuming that the magnitude of the input data is

$$|D_k| \leq D_{max} \text{ (where } D_{max} \leq 1)$$

Filter coefficients should be determined so that no overflow can occur at the frequency at which the filter gain is maximum. Overflow may still occur on rare occasions, but these can be detected by monitoring the OVF pin.

Filter Tap Number Limitations

Multiplier output is rounded to 16 bits in each stage, which generates quantization noise that accumulates in the final stage. The quantization noise generated by each multiplier stage is

$$N_{QM} = \frac{(2^{-13})^2}{12}$$

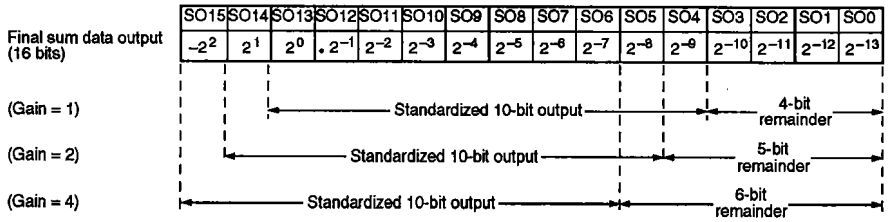
and the quantization noise caused at the output by rounding at the *m*th bit is

$$N_{QO} = \frac{(2^{-m})^2}{12}$$

Therefore, the maximum number of taps a filter can have, N_F, before the internal quantization noise exceeds the output noise is given by

$$N_F \leq \frac{N_{QO}}{N_{QM}}$$

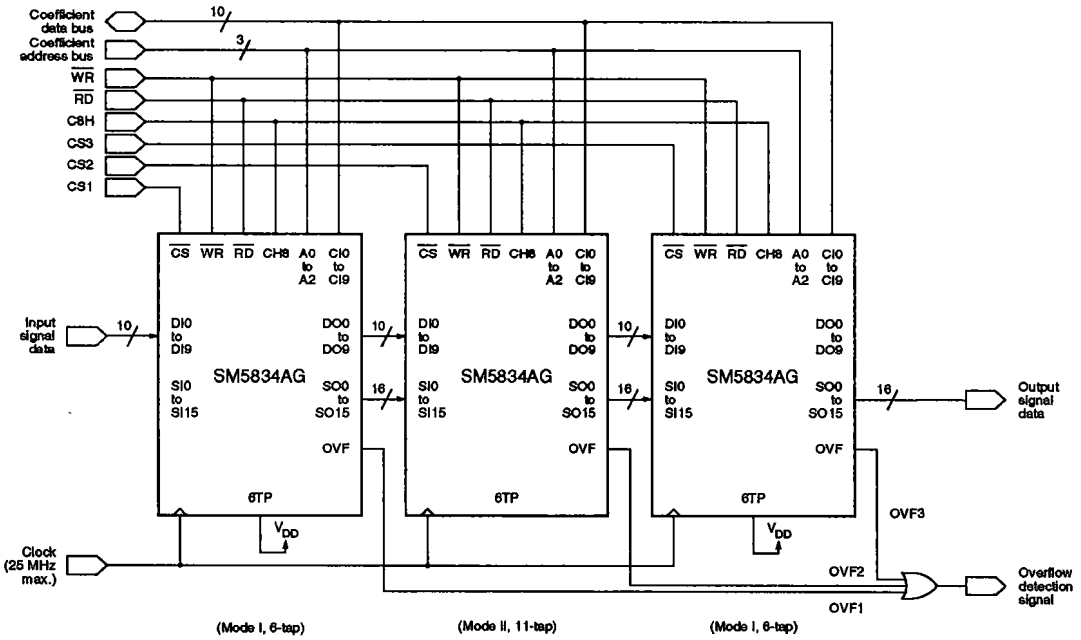
The range of bits of the sum output word depends on the gain of the filter. The output signal, therefore, should not exceed the maximum value represented by the selected bits.



Maximum gain	Maximum number of taps
1	256
2	1024
4	4096

TYPICAL APPLICATION

23-tap Linear Phase Filter



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