REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY

CHECKED BY

APPROVED BY

DRAWING APPROVAL DATE
92-08-05

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, 16-BIT, MICROPROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90678
A	67268	

SHEET 1

DESC FORM 193
JUL 91

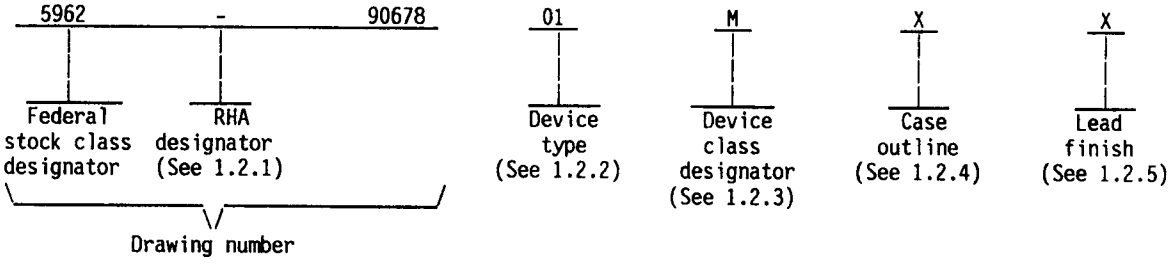
5962-E060

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	f_{CLK}
01	80C286-10	16-bit CMOS microprocessor	10 MHz
02	80C286-12	16-bit CMOS microprocessor	12.5 MHz

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). For device classes M, B, and S, case outline(s) shall meet the requirements in appendix C of MIL-M-38510 and as listed below. For device classes Q and V, case outline(s) shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	P-AC (68-pin 1.180" x 1.180" x .345"), pin grid array package
Y	See figure 1 (68-terminal, .970" x .970" x .115"), quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage	+7.0 V dc
Input, output or I/O voltage applied range	-1.0 V dc to V_{CC} +1.0 V dc
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	275°C
Power dissipation (P_D)	1.1 W
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-M-38510, appendix C
Case Y	9.5°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input rise and fall time (from 0.8 V to 2.0 V):	
Device type 01	10 ns maximum
Device type 02	8.0 ns maximum
Case operating temperature range	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 4.5 V f = 2 MHz	1,2,3	All	-0.5	0.8	V
Input high voltage	V_{IH}	V_{CC} = 5.5 V f = 2 MHz			2.0	V_{CC}+ 0.5 V	
CLK input low voltage	V_{ILC}	V_{CC} = 4.5 V f = 2 MHz			-0.5	1.0	
CLK input high voltage	V_{IHC}	V_{CC} = 5.5 V f = 2 MHz			3.6	V_{CC}+ 0.5 V	
Output low voltage	V_{OL}	I_{OL} = 2.0 mA 2/ V_{CC} = 4.5 V				0.45	
Output high voltage	V_{OH}	I_{OH} = -2.0 mA 2/ V_{CC} = 4.5 V			3.0		
		I_{OH} = -100 µA 2/ V_{CC} = 4.5 V			V_{CC}- 0.5 V		
Input leakage current	I_{IL}	V_{CC} = 5.5 V, 2/ measured on pins: 29, 31, 57, 59, 61, 63, and 64			-10	+10	µA
Input sustaining current (bus hold low)	I_{BHL}	V_{IN} = 1.0 V 3/			35	200	
Input sustaining current (bus hold high)	I_{BHH}	V_{IN} = 3.0 V 4/			-50	-400	
Input sustaining current on BUSY and ERROR pins	I_{SL}	V_{IN} = 0.0 V 5/			-30	-500	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Bus hold low overdrive	I_{BHLO}	V_{CC} = 5.5 V 6/ V_{IN} = 5.5 V or 0.0 V	1,2,3	All	250		µA
Bus hold high overdrive	I_{BHHO}				-420		
Output leakage current	I_{LO}	V_{OUT} = 0.0 V or 5.5 V, V_{CC} = 5.5 V, measured on pins 1, 7, 8, 10 through 28, 32, 33 and 34			-10	+10	
Active power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 2.4 V or 0.40 V, outputs unloaded, C_L = 100 pF; f = 10 MHz		01		200	mA
		f = 12.5 MHz		02		220	
Standby power supply current	I_{CCS}	V_{CC} = 5.5 V, V_{IN} = 0.0 V or 5.5 V, outputs unloaded 7/		All		5.0	
Clk input capacitance	C_{CLK}	f_{CLK} = 1.0 MHz, see 4.4.1c	4			20	pF
Other input capacitance	C_{IN}					10	
Input/output capacitance	C_O					20	
Functional tests		See 4.4.1d	7, 8				
System clock period	t_1	See figure 3	9,10,11	01	50		ns
				02	40		
System clock low time	t_2	Measured between the 1.0 V reference points on the clock input, see figure 3		01	12		
				02	11		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
System clock high time	t_3	Measured between the 3.6 V reference points on the clock input, see figure 3	9,10,11	01	16		ns
				02	13		
Asynchronous input setup time 8/	t_4	See figure 3		01	20		
				02	15		
Asynchronous input hold time 8/	t_5			01	20		
				02	15		
RESET setup time	t_6			01	23		
				02	10		
RESET hold time	t_7			All	5		
Read data setup time	t_8			01	8		
				02	5		
Read data hold time	t_9			01	8		
				02	4		
READY setup time	t_{10}			01	26		
				02	20		
READY hold time	t_{11}			01	25		
				02	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Status/PEACK active delay 9/	t_{12a}	C_L = 100 pF, I_L = 2.0 mA, See figure 3	9,10,11	01	5 13/	22	ns
				02	1	21	
Status/PEACK inactive delay 10/	t_{12b}			01	3 13/	30	
				02	1	24	
Address valid delay 11/	t_{13}			01	4 13/	35	
				02	1	32	
Write data valid delay 11/	t_{14}			01	3 13/	40	
				02	0	31	
Address/status/data float delay 12/ 13/	t_{15}	See figure 3, I_L = -6.0 mA (V_{OH} to float), I_L = 8.0 mA (V_{OL} to float), C_L = 100 pF		01	2 13/	47	
				02	0	32	
HLDA valid delay 14/	t_{16}	C_L = 100 pF, I_L = 2.0 mA, See figure 3		01	3 13/	47	
				02	0	25	
System CLK rise time	t_{17}	1.0 V to 3.6 V 6/ 13/		All		8	
System CLK fall time	t_{18}	3.6 V to 1.0 V 6/ 13/		All		8	
Address valid to status setup time 13/ 15/	t_{19}	C_L = 100 pF, I_L = 2.0 mA, See figure 3		01	27		
				02	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ The following pins are active low: $\overline{BHE}$, $\overline{BUSY}$, $\overline{ERROR}$, $\overline{INTA}$ of COD/$\overline{INTA}$, $\overline{LOCK}$, $\overline{PEACK}$, $\overline{SO}$, $\overline{SI}$, $\overline{READY}$. Unless otherwise specified all test conditions shall be at worst case condition.

2/ V_{IN} = 0.8 V, 2.0 V. Relaxed input levels for V_{OL} and V_{OH} may be used if separate V_{IL} and V_{IH} tests (guaranteeing threshold voltage transmission) are performed.

3/ I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0 V on the following pins: 36 through 51, 66 and 67.

4/ I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0 V on the following pins: 4, 5, 6, 36 through 51, 66, 67 and 68.

5/ I_{IL} should be measured after raising V_{IN} to V_{CC} and then lowering to 0.0 V on pins 53 and 54.

6/ If not tested then guaranteed to the limits specified in table I.

7/ I_{CCS} should be tested with the clock stopped in phase two of the processor clock cycle.

8/ Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR and BUSY. This specification is given only for testing purposes to assure recognition of a specific CLK edge.

9/ Delay from 1.0 V on the CLK to 1.5 V for minimum (HOLD time) and to 1.5 V for maximum (active delay).

10/ Delay from 1.0 V on the CLK to 1.5 V for minimum (HOLD time) and to 1.5 V for maximum (inactive delay).

11/ Delay from 1.0 V on the CLK to 1.5 V.

12/ Delay from 1.0 V on the CLK to float (no current drive) condition.

13/ Tested initially and at process and design changes. Thereafter guaranteed, if not tested, to the limits specified in table I.

14/ Delay from 1.0 V on the CLK to 1.5 V.

15/ Delay measured from address either reaching 1.5 V (valid) to status going active reaching 0.8 V or status going inactive reaching 1.5 V.

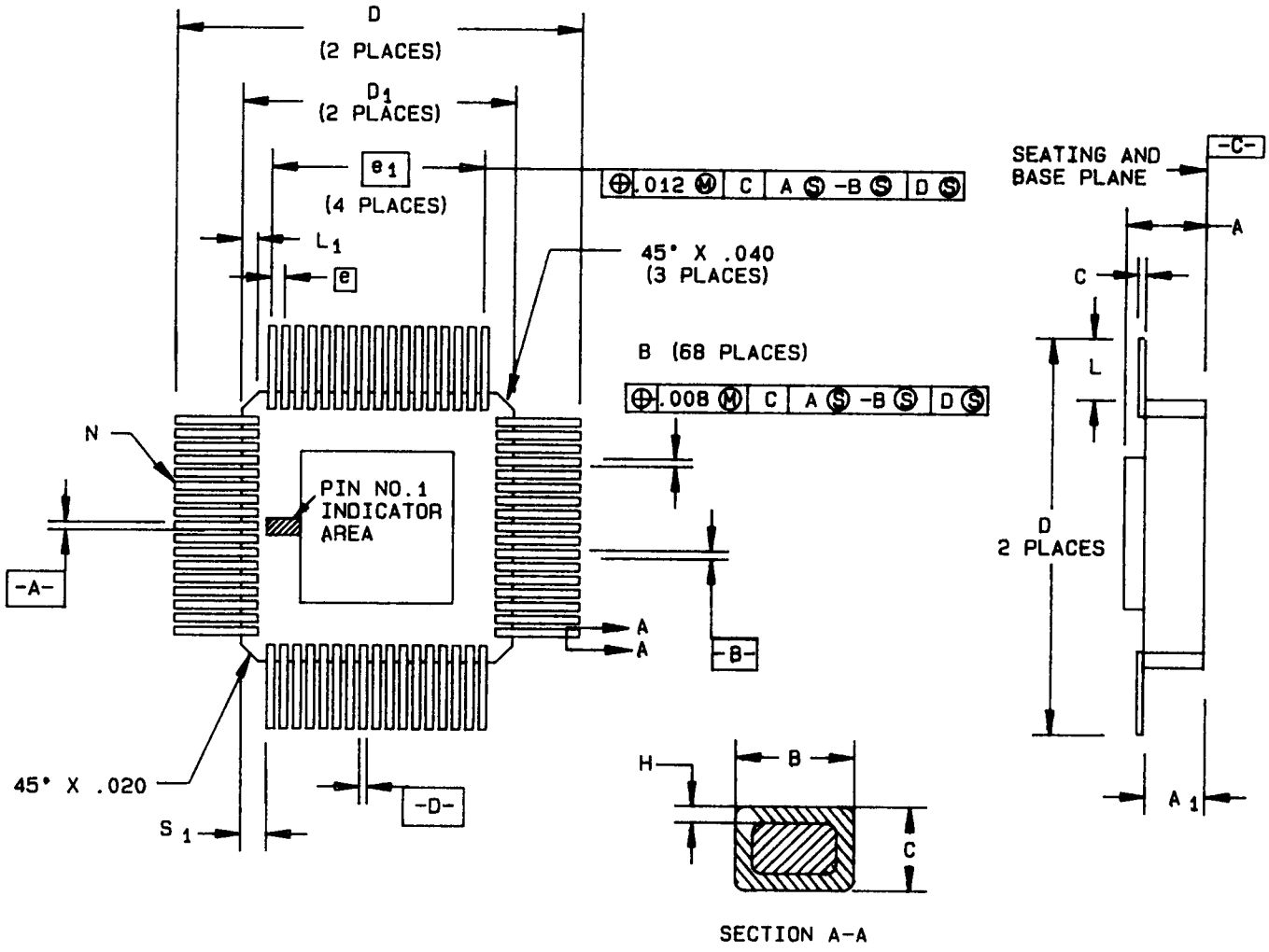


FIGURE 1. Case outline Y.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90678
		REVISION LEVEL	SHEET 10

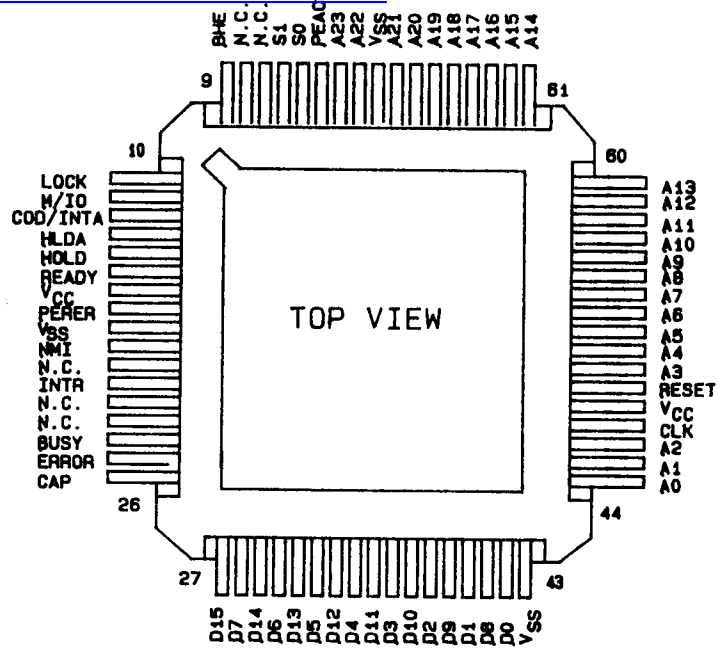
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.080	.115	2.03	2.92
A_1	.070	.094	1.78	2.39
B	.016	.021	0.41	1.53
C	.008	.012	0.20	0.31
D_1	.926	.970	23.52	24.64
e	.050 BSC		1.27 BSC	
e_1	.800 BSC		20.32 BSC	
D	1.640	1.870	41.66	47.50
L	.350	.450	8.89	11.43
L_1	.040	.060	1.02	1.52
M	---	.0015	---	0.038
N	68			
N_D/N_E	17			
S_1	.050	---	1.27	---

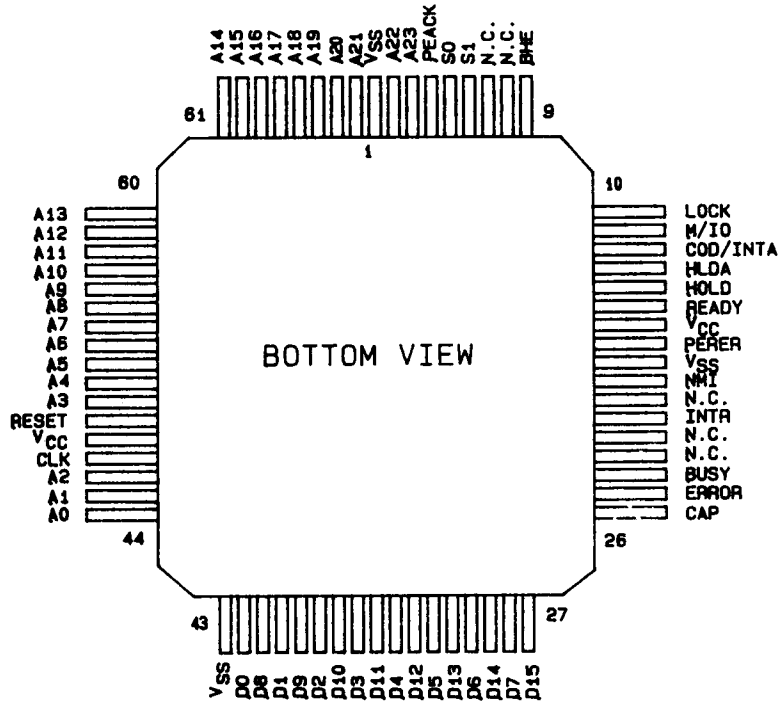
NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance for three place decimals is ±.005.
4. The index feature for terminal 1 identification, optical orientation, or handling purposes shall be within the shaded areas shown on planes 1 and 2. Terminal 1 identification is optional on the surface closet to the seating plane.
5. Corner shapes (square notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
6. Dimension N: Number of terminals per package edge.
7. Dimensioning is in accordance with ANSI Y14.5M 1982.
8. Lead coplanarity shall be within .004 inch (0.10 mm) .050 inch (1.27 mm) from package body.
9. No overhang of the lead on the braze pad is allowed.
10. Dimensions B and C apply to base metal only. Dimension M applies to plating thickness.
11. The leads on this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars, carriers, etc.) are not shown on the drawing; however, when microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline Y - Continued.

Device types	All	Device types	All
Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	$\overline{BHE}$	F10	A4
A3	NC	F11	A5
A4	S0	G1	NC
A5	A23	G2	NMI
A6	V_{SS}	G10	RESET
A7	A20	G11	A3
A8	A18	H1	NC
A9	A16	H2	INTR
A10	A14	H10	CLK
B1	LOCK	H11	V_{CC}
B2	NC	J1	BUSY
B3	S1	J2	NC
B4	PEACK	J10	A1
B5	A22	J11	A2
B6	A21	K1	NC
B7	A19	K2	ERROR
B8	A17	K3	D7
B9	A15	K4	D6
B10	A12	K5	D5
B11	A13	K6	D4
C1	COD/INTA	K7	D3
C2	M/IO	K8	D2
C10	A10	K9	D1
C11	A11	K10	D0
D1	HOLD	K11	A0
D2	HLDA	L2	D15
D10	A8	L3	D14
D11	A9	L4	D13
E1	V_{CC}	L5	D12
E2	READY	L6	D11
E10	A6	L7	D10
E11	A7	L8	D9
F1	V_{SS}	L9	D8
F2	PEREQ	L10	V_{SS}

FIGURE 2. Terminal connections.





Case Y

FIGURE 2. Terminal connections - Continued.

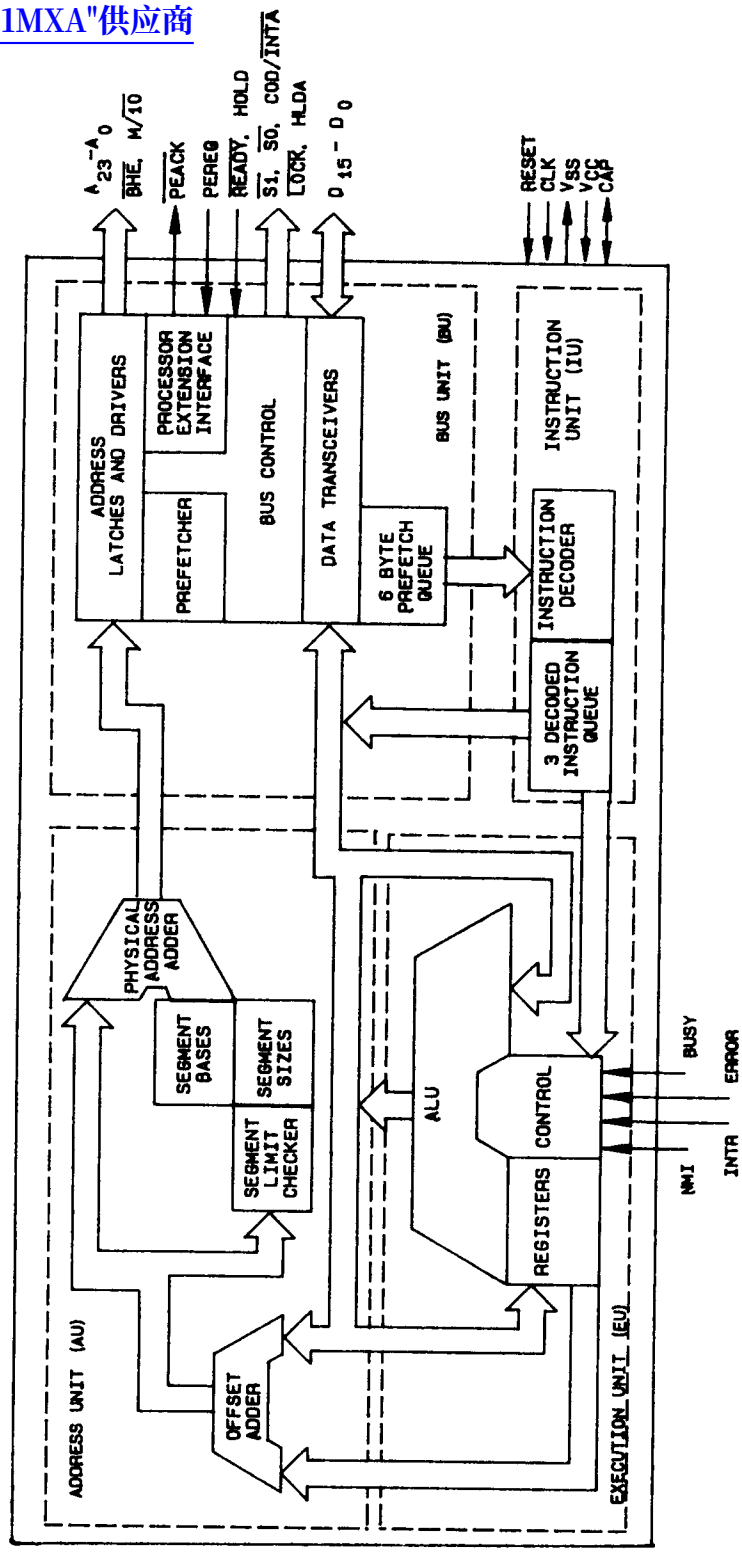


FIGURE 3. Functional block diagram.

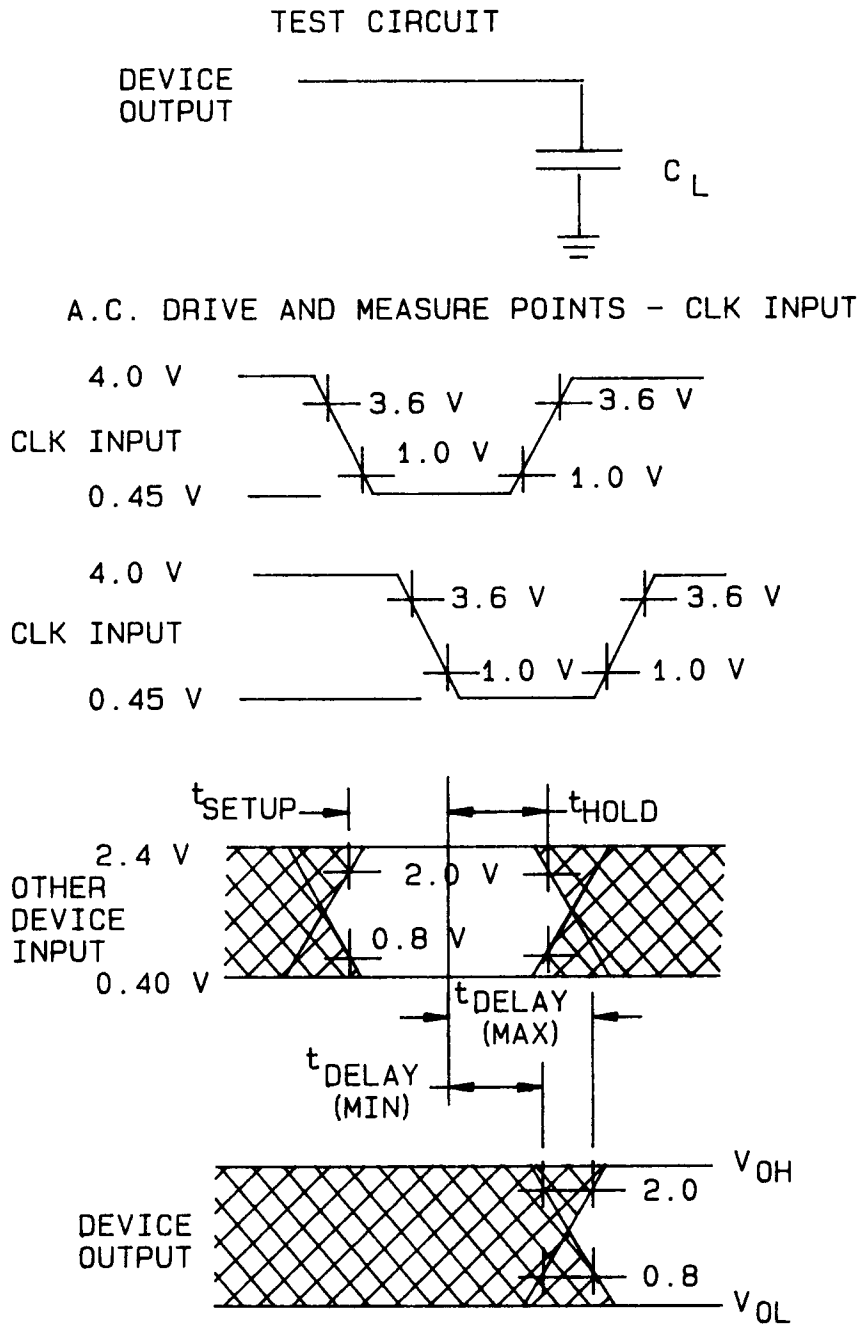
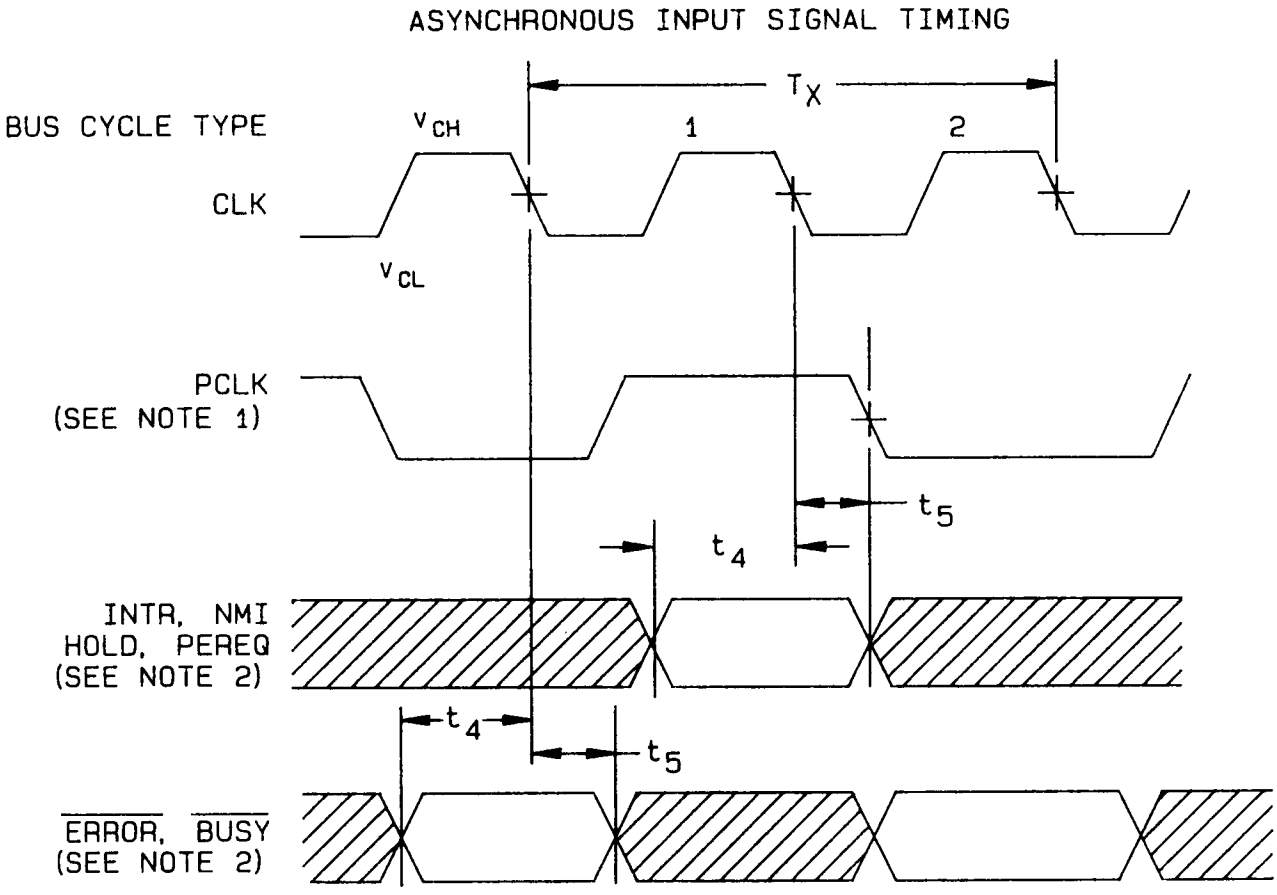


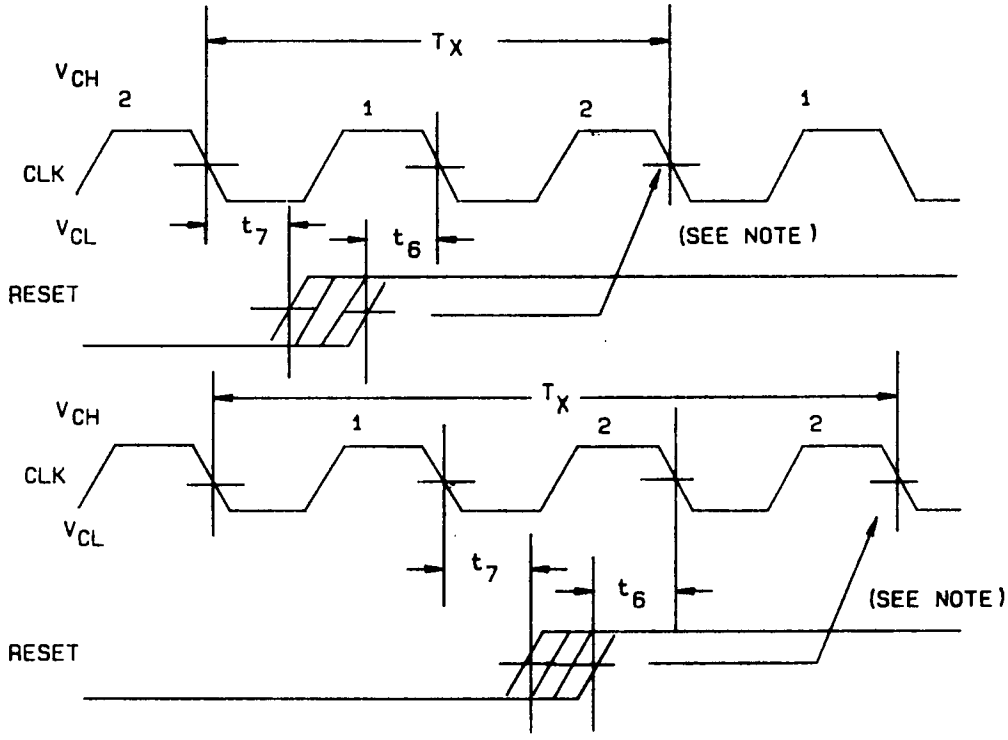
FIGURE 4. Switching waveforms and test circuit.



NOTES:
1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

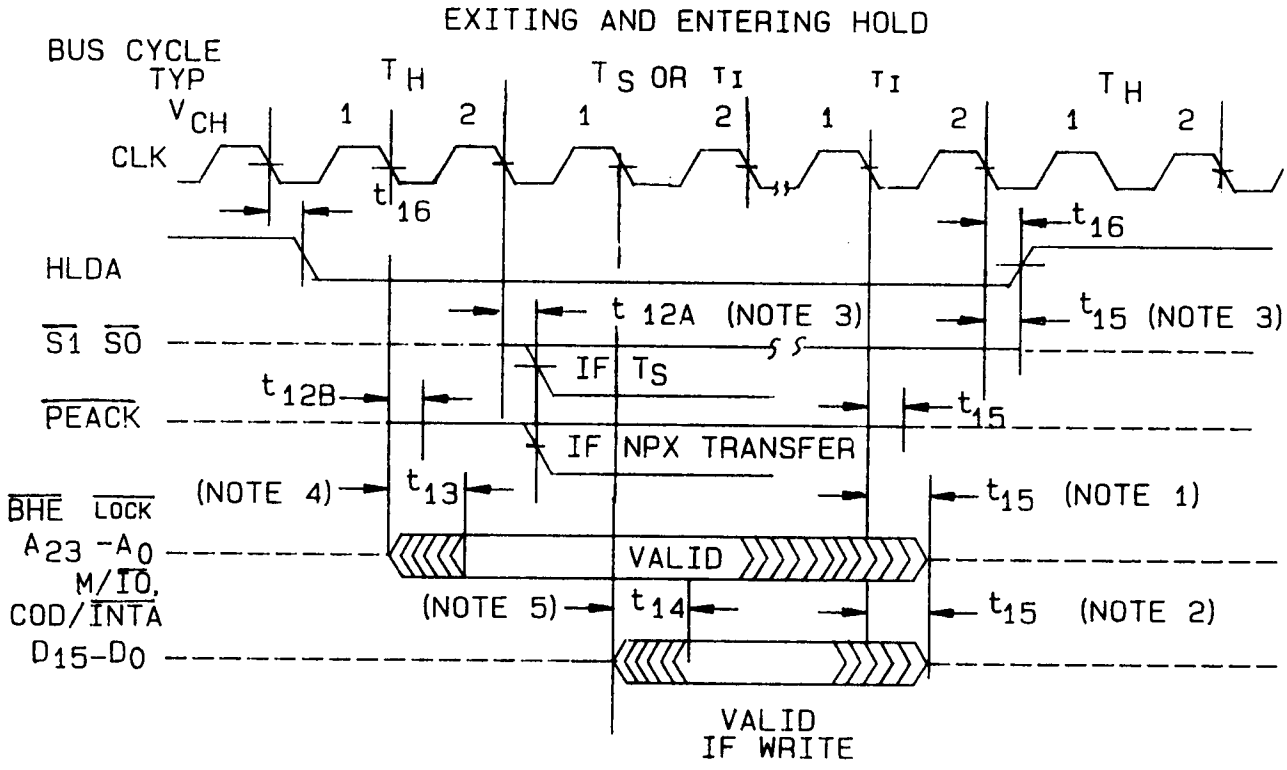
FIGURE 4. Switching waveforms and test circuit - Continued.

RESET INPUT TIMING AND
SUBSEQUENT PROCESSOR CYCLE PHASE



NOTE: When RESET meets the setup time shown, the CLK will start or repeat cycle 2 of a processor cycle.

FIGURE 4. Switching waveforms and test circuit - Continued.



NOTES:
1. These signals may not be driven by the device during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_I in the diagram was a write T_C.
3. The device puts its status pins in a high impedance logic one state during T_H.
4. BHE and LOCK are driven at this time but will not become valid until T_S.
5. The data bus will remain in a high impedance state if a read cycle is performed.

FIGURE 4. Switching waveforms and test circuit - Continued.

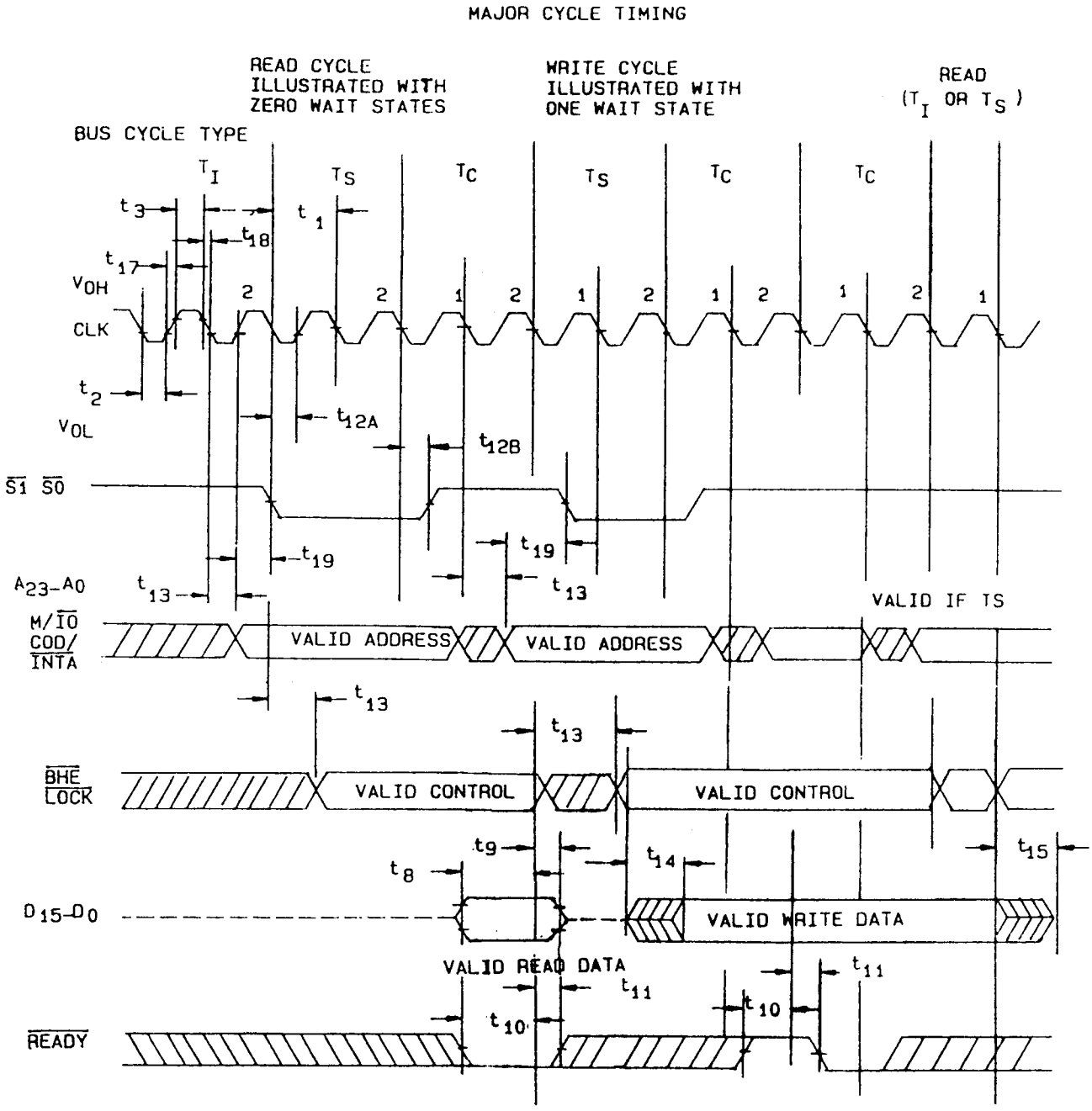
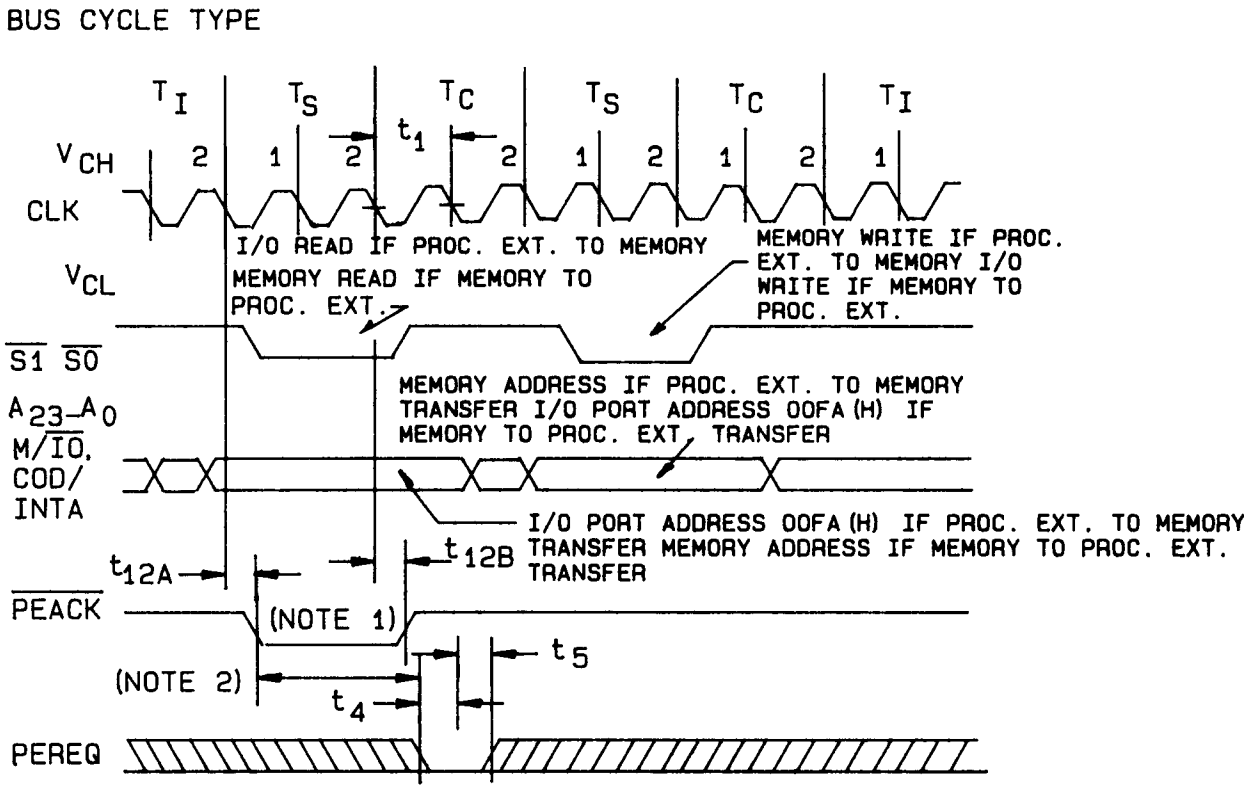


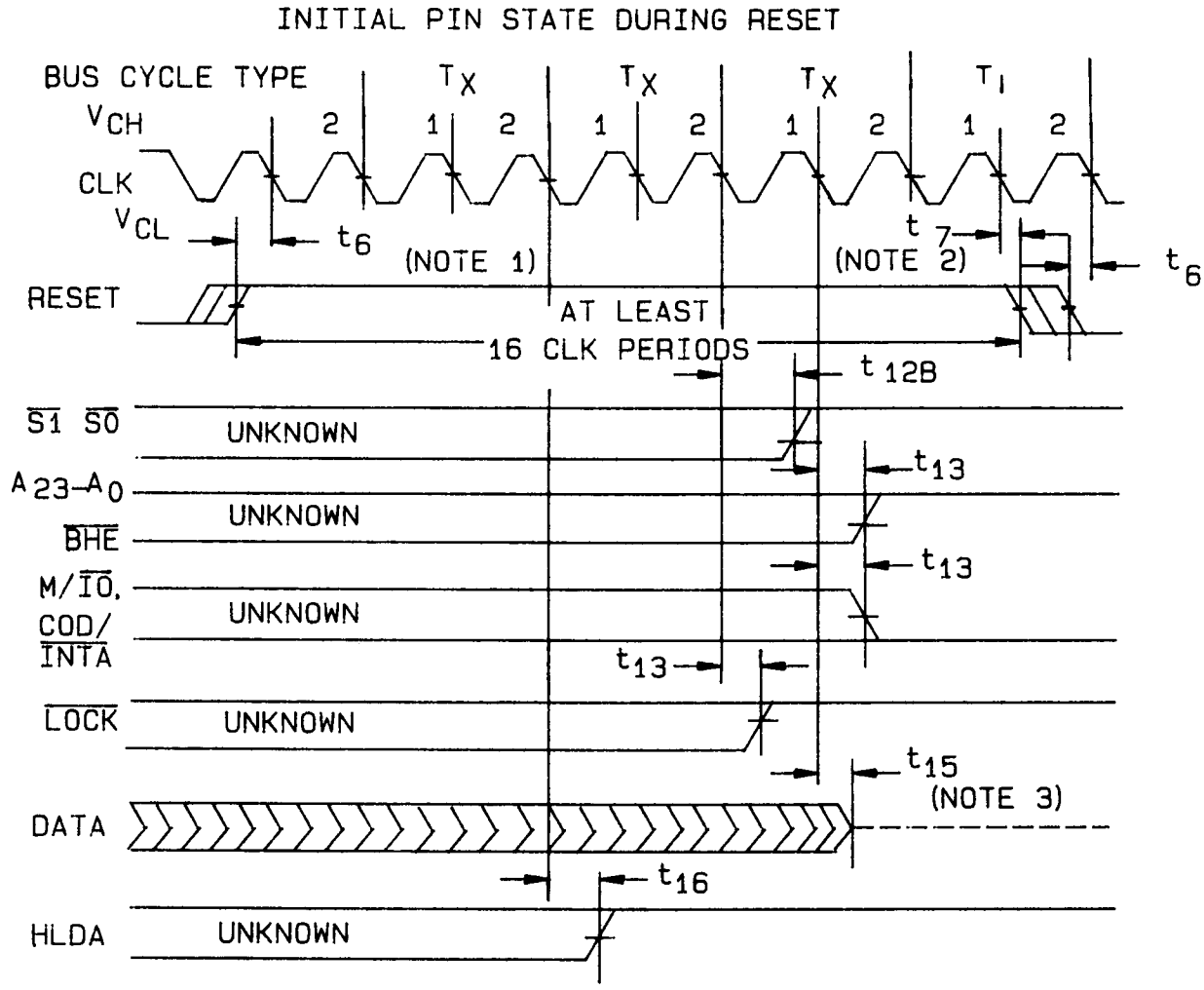
FIGURE 4. Switching waveforms and test circuit - Continued.

PEREQ/PEACK TIMING FOR ONE TRANSFER ONLY



NOTES:
1. PEACK always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is 3 x t1 - t12A(max) - t4(min). The actual, configuration dependent, maximum time is: 3 x t1 = t12A(max) - t4(min) + N x 2 x t1. N is the number of extra TC states added to either the first or second bus operation of the processor extension data operand transfer sequence.

FIGURE 4. Switching waveforms and test circuit - Continued.



NOTES:
1. Setup time for RESET (rising) may be violated with the consideration that cycle 1 of the processor clock may begin one system CLK period later.
2. Setup and hold times for RESET (falling) must be met for proper operation, but RESET (falling) may occur during CLK cycle 1 or 2.
3. The data bus is only guaranteed to be in a high impedance state at the time shown.

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{CLK}, C_{IN} and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

d. For device class M, subgroups 7 and 8 tests shall consist of verifying the instruction set and functionality of the device. These test form a part of the vendors test tape and shall be maintained and available from approved sources of supply. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device and these test shall be approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1,7		1,7
Final electrical parameters (see 4.2)	1/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	2/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11	1/ 1,2,3,7, 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			3/ 2,7,8,10		3/ 1,2,3
Group C end-point electrical parameters (see 4.4)	3/ 2,8A,10	3/ 2,8A,10		3/ 2,8,10	
Group D end-point electrical parameters (see 4.4)	3/ 2,8A,10	3/ 2,8A,10	3/ 2,7,8,10	3/ 2,8,10	
Group E end-point electrical parameters (see 4.4)	3/ 2,8,10	3/ 2,8,10	3/ 2,8,10	3/ 2,8,10	3/ 2,8,10

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Subgroups 1, 7, and 9 may be substituted.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

6.5 Symbols, definitions, and functional descriptions.

CLK	System clock: This input pin provides the fundamental timing for the device system. It is divided by two inside the device to generate the processor clock. The internal device-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D15-D0	Data bus: This input/output pin inputs data during memory, I/O and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and is held at high impedance to the last valid logic level during bus hold acknowledge.
A23-A0	Address bus: This output pin outputs physical memory and I/O port addresses. A23-A16 are LOW during I/O transfers. A0 is LOW when data is to be transferred on pins D7-D0. The address bus in active high and floats to three-state off during bus hold acknowledge.
$\overline{BHE}$	Bus high enable: This output pin indicates transfer of data on the upper byte of the data bus D15-D8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to three-state OFF during bus hold acknowledge.

BHE and A0 encodings

BHE value	A0 value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus(D15-D8)
1	0	Byte transfer on lower half of data bus(D7-D0)
1	1	Reserved

6.5 Symbols, definitions, and functional descriptions - Continued.

$\overline{S1}$, $\overline{S0}$ — Bus cycle status: This output pin indicates initiation of a bus cycle and along with M/IO and COD/INTA defines the type of bus cycle. The bus is in a TS state whenever one or both are LOW. S1 and S0 are active LOW and are held at a high impedance logic one during bus hold acknowledge.

Bus cycle status definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	If A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None, not a status cycle

M/$\overline{IO}$ — Memory I/O select: This output pin distinguishes memory access from I/O access. If HIGH during TS, a memory cycle or a halt shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/IO is held at high impedance to the last valid logic state during bus hold acknowledge.

COD/$\overline{INTA}$ — Code/interrupt acknowledge: This output pin distinguishes instruction fetch cycles from memory data read cycle. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/INTA is held at high impedance to the last valid logic state during bus hold acknowledge. Its timing is the same as M/IO.

$\overline{LOCK}$ — Bus lock: This output pin indicates that other system bus masters are not to gain control of the system bus for the current and following bus cycles. The LOCK signal may be activated explicitly by the "LOCK" instructions, interrupt acknowledge, or descriptor table access. LOCK is active LOW and is held at a high impedance logic one during bus hold acknowledge

$\overline{READY}$ — Bus ready: This input pin terminates a bus cycle. Bus cycles are extended without limit until terminated by READY LOW. READY is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. READY is ignored during bus hold acknowledge.

HOLD, HLDA — Bus hold request and hold acknowledge: This I/O pin controls ownership of the device local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the device will float its bus drivers and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the device deactivating HLDA and regaining control of the local bus. This terminates the bus acknowledge condition. HOLD may be asynchronous to the system clock. These signals are active HIGH. Note that HLDA never floats.

6.5 Symbols, definitions, and functional descriptions - Continued.

INTR — Interrupt request: This input pin requires the device to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the device responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To ensure program interruption, INTR must remain active until an interrupt acknowledge bus cycle is initiated. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.

NMI — Non-maskable interrupt request: This input pin interrupts the device with an internally supplied vector value of two. No interrupt acknowledge cycles are performed. The interrupt enable bit in the device flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles.

PEREQ, PEACK — Processor extension operand request and acknowledge: This I/O pin extends the memory management and protection capabilities of the device to processor extensions. The PEREQ input requests the device to perform a data operand transfer for a processor extension. The PEACK output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH. PEACK is active LOW and is held at a high impedance logic one during bus hold acknowledge. PEREQ may be asynchronous to the system clock.

$\overline{BUSY}$, $\overline{ERROR}$ — Processor extension $\overline{BUSY}$ and $\overline{ERROR}$: This input pin indicates the operating condition of a processor extension to the device. An active BUSY input stops device program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The device may be interrupted while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the device to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.

RESET — System reset: This input pin clears the internal logic of the device and is active HIGH. The device may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the device enter the state shown below.

Pin state during reset

Pin value	Pin names
1(high)	$\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23-A0, $\overline{BHE}$, $\overline{LOCK}$
0(low)	M/IO, COD/INTA, HLDA
High impedance	D15-D0

Operation of the device begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the device for internal initializations before the first bus cycles are to fetch code from the power-on execution address is performed. A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock: however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.

V_{SS} — System ground: These input ground pins must all be connected to system ground.

V_{CC} — System power: These are the input +5.0 volt power supply pins (a 0.1 μF capacitor between pins E1 and F1 is recommended).

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.