

# Memory FRAM

CMOS

## 2 M Bit (128 K × 16)

# MB85R2002

### ■ DESCRIPTIONS

The MB85R2002 is an FRAM (Ferroelectric Random Access Memory) chip consisting of 131,072 words × 16 bits of non-volatile memory cells created using ferroelectric process and silicon gate CMOS process technologies.

The MB85R2002 is able to retain data without using a back-up battery, as is needed for SRAM.

The memory cells used in the MB85R2002 can be used for at least  $10^{10}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

The MB85R2002 uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

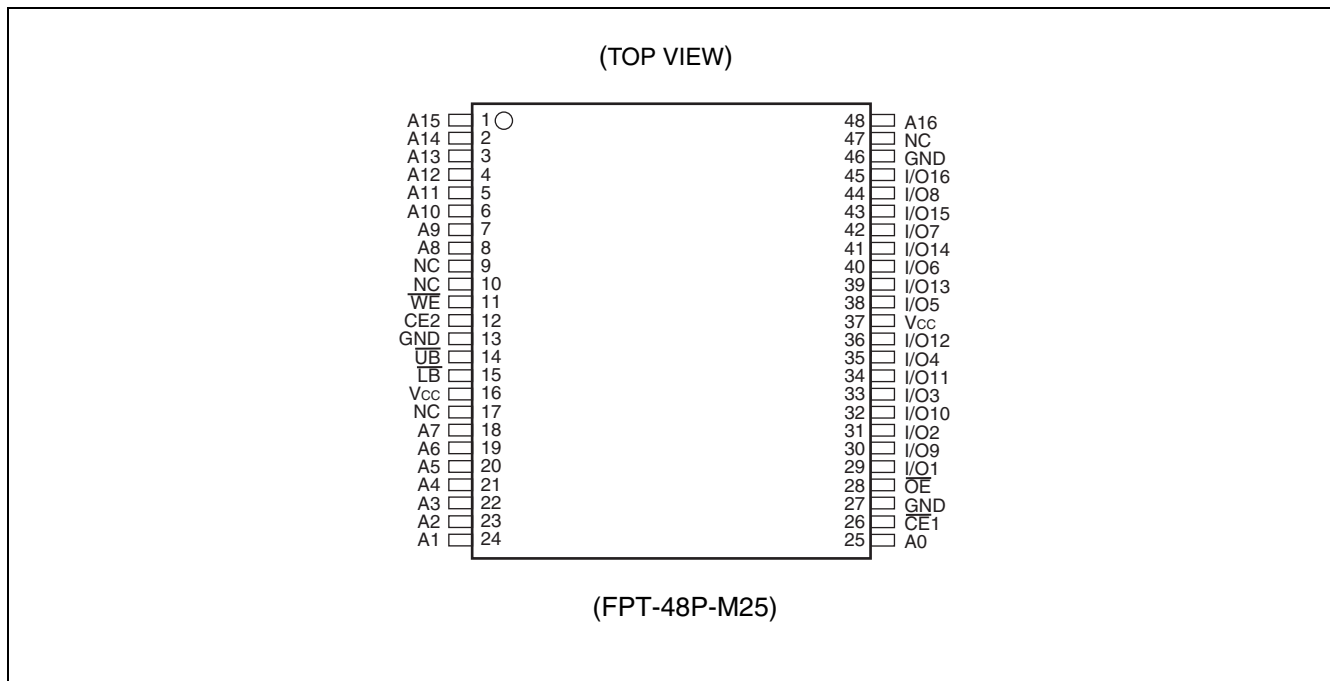
### ■ FEATURES

- Bit configuration : 131,072 words × 16 bits
- Read/write endurance :  $10^{10}$  times/bit (Min)
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : -20 °C to +85 °C
- Data retention : 10 years (+55 °C)
- $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  data byte control
- Package : 48-pin plastic TSOP (1)

# MB85R2002

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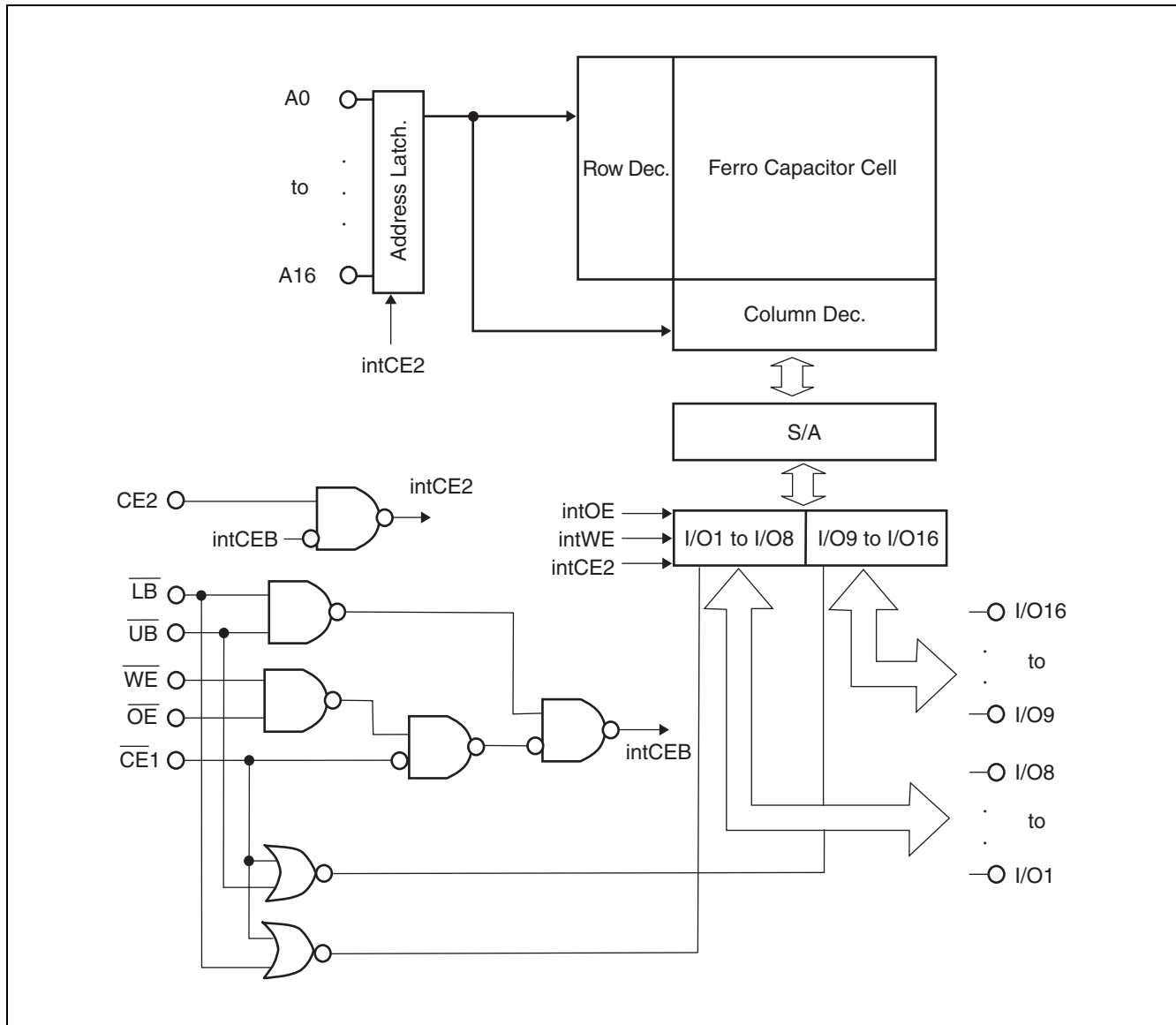
## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Pin name	Function
A0 to A16	Address Input
I/O1 to I/O16	Data Input/Output
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$ , $\overline{UB}$	Data Byte Control Input
V <sub>CC</sub>	Power Supply
GND	Ground
NC	No Connection

## ■ BLOCK DIAGRAM



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## ■ FUNCTION TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Pre-charge	H	X	X	X	X	X	High-Z	High-Z	Standby ( $I_{SB}$ )
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	$\overline{\downarrow}$ L	H $\uparrow$	H	L	L	L	Dout	Dout	Operation ( $I_{CC}$ )
					L	H	Dout	High-Z	
					H	L	High-Z	Dout	
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	$\overline{\downarrow}$	L	L	Dout	Dout	
					L	H	Dout	High-Z	
					H	L	High-Z	Dout	
Write	$\overline{\downarrow}$ L	H $\uparrow$	L	X	L	L	Din	Din	
					L	H	Din	High-Z	
					H	L	High-Z	Din	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	$\overline{\downarrow}$	H	L	L	Din	Din	
					L	H	Din	High-Z	
					H	L	High-Z	Din	

L =  $V_{IL}$ , H =  $V_{IH}$ , X can be either  $V_{IL}$  or  $V_{IH}$ , High-Z = High Impedance

$\overline{\downarrow}$  : Latch address and latch data at falling edge,  $\uparrow$  : Latch address and latch data at rising edge

\*1 :  $\overline{OE}$  control of the Pseudo-SRAM means the valid address at the falling edge of  $\overline{OE}$  to read.

\*2 :  $\overline{WE}$  control of the Pseudo-SRAM means the valid address and data at the falling edge of  $\overline{WE}$  to write.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage*	$V_{CC}$	-0.5	+4.0	V
Input Voltage*	$V_{IN}$	-0.5	$V_{CC} + 0.5$	V
Output Voltage*	$V_{OUT}$	-0.5	$V_{CC} + 0.5$	V
Ambient Operating Temperature	$T_A$	-20	+85	°C
Storage Temperature	$T_{stg}$	-40	+125	°C

\* : All voltages are referenced to GND = 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage*	$V_{CC}$	3.0	3.3	3.6	V
Input Voltage (high)*	$V_{IH}$	$V_{CC} \times 0.8$	—	$V_{CC} + 0.5$	V
Input Voltage (low)*	$V_{IL}$	-0.5	—	+0.6	V
Ambient Operating Temperature	$T_A$	- 20	—	+85	°C

\* : All voltages are referenced to GND = 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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## ■ ELECTRICAL CHARACTERISTICS

### 1. DC CHARACTERISTICS

(within recommended operating conditions)

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$I_{LIL}$	$V_{IN} = 0\text{ V to }V_{CC}$	—	—	10	$\mu\text{A}$
Output Leakage Current	$I_{LOL}$	$V_{OUT} = 0\text{ V to }V_{CC}$ , $\overline{CE1} = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	$\mu\text{A}$
Supply Current	$I_{CC}$	$\overline{CE1} = 0.2\text{ V}$ , $CE2 = V_{CC}-0.2\text{ V}$ , $I_{OUT} = 0\text{ mA}^{*1}$	—	10	15	mA
Standby Current	$I_{SB}$	$\overline{CE1} \geq V_{CC}-0.2\text{ V}$	—	10	50	$\mu\text{A}$
		$CE2 \leq 0.2\text{ V}^{*2}$				
		$\overline{OE} \geq V_{CC}-0.2\text{ V}$ , $\overline{WE} \geq V_{CC}-0.2\text{ V}^{*2}$				
		$LB \geq V_{CC}-0.2\text{ V}$ , $UB \geq V_{CC}-0.2\text{ V}^{*2}$				
Output Voltage (high)	$V_{OH}$	$I_{OH} = -0.1\text{ mA}$	$V_{CC} \times 0.8$	—	—	V
Output Voltage (low)	$V_{OL}$	$I_{OL} = 2.0\text{ mA}$	—	—	0.4	V

\*1 : During the measurement of  $I_{CC}$ , the Address, Data In were taken to only change once per active cycle.  
 $I_{OUT}$  : output current

\*2 : All pins other than setting pins should be input at the CMOS level voltages such as  $H \geq V_{CC} - 0.2\text{ V}$ ,  $L \leq 0.2\text{ V}$ .

### 2. AC CHARACTERISTICS

#### • AC TEST CONDITIONS

Supply Voltage : 3.0 V to 3.6 V

Operating Temperature :  $-20\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

Input Voltage Amplitude : 0.3 V to 2.7 V

Input Rising Time : 5 ns

Input Falling Time : 5 ns

Input Evaluation Level : 2.0 V / 0.8 V

Output Evaluation Level : 2.0 V / 0.8 V

Output Impedance : 50 pF

#### (1) Read Operation

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	$t_{RC}$	150	—	ns
$\overline{CE1}$ Active Time	$t_{CA1}$	120	—	ns
$CE2$ Active Time	$t_{CA2}$	120	—	ns
$\overline{OE}$ Active Time	$t_{RP}$	120	—	ns
$LB$ , $UB$ Active Time	$t_{BP}$	120	—	ns
Pre-charge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	5	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
$\overline{OE}$ Setup Time	$t_{ES}$	5	—	ns
$LB$ , $UB$ Setup Time	$t_{BS}$	5	—	ns
Output Data Hold time	$t_{OH}$	0	—	ns
Output Set Time	$t_{LZ}$	30	—	ns
$\overline{CE1}$ Access Time	$t_{CE1}$	—	100	ns
$CE2$ Access Time	$t_{CE2}$	—	100	ns
$\overline{OE}$ Access Time	$t_{OE}$	—	100	ns
Output Floating Time	$t_{OHZ}$	—	20	ns

## (2) Write Operation

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	$t_{WC}$	150	—	ns
CE1 Active Time	$t_{CA1}$	120	—	ns
CE2 Active Time	$t_{CA2}$	120	—	ns
LB, UB Active Time	$t_{BP}$	120	—	ns
Pre-Charge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	5	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
LB, UB Setup Time	$t_{BS}$	5	—	ns
Write Pulse Width	$t_{WP}$	120	—	ns
Data Setup Time	$t_{DS}$	0	—	ns
Data Hold Time	$t_{DH}$	50	—	ns
Write Setup Time	$t_{WS}$	5	—	ns

## (3) Power ON/OFF Sequence

(within recommended operating conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ LEVEL hold time for Power OFF	$t_{pd}$	85	—	—	ns
$\overline{CE1}$ LEVEL hold time for Power ON	$t_{pu}$	85	—	—	ns

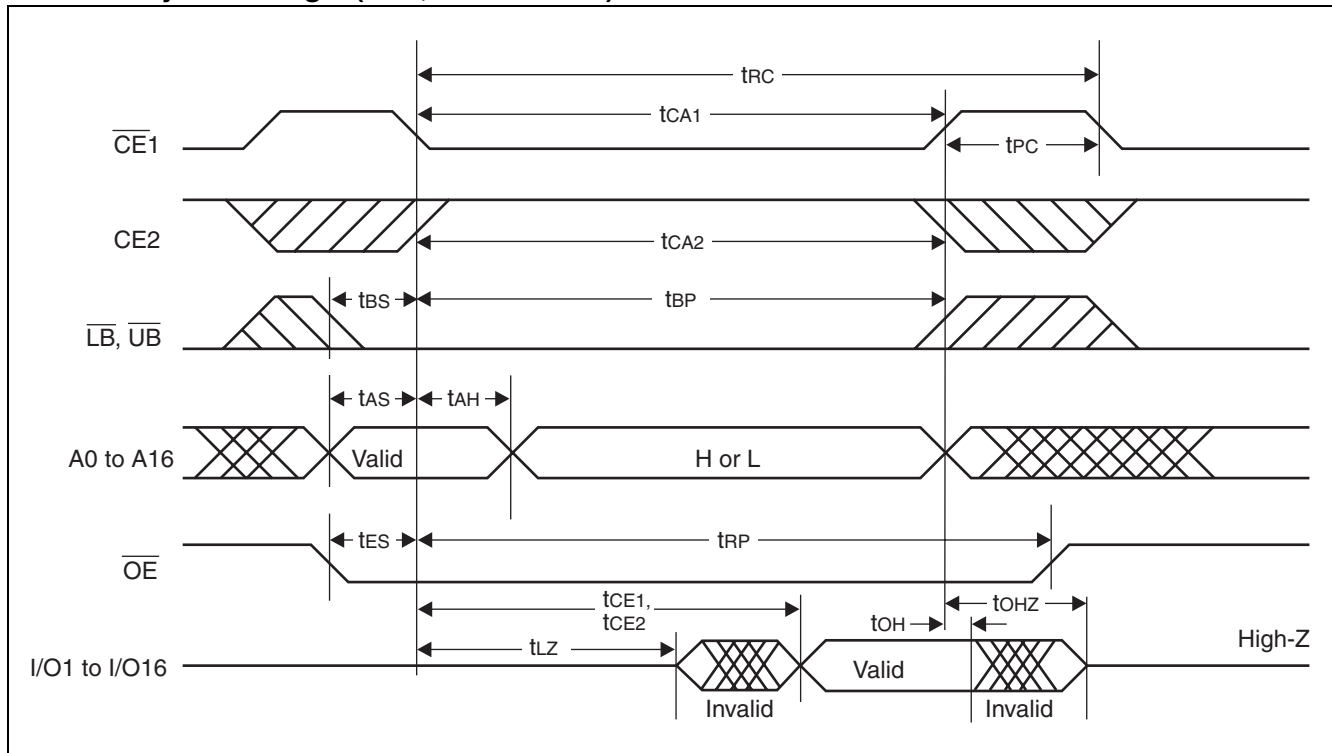
## 3. Pin Capacitance

(f = 1 MHz,  $T_A = +25\text{ }^{\circ}\text{C}$ )

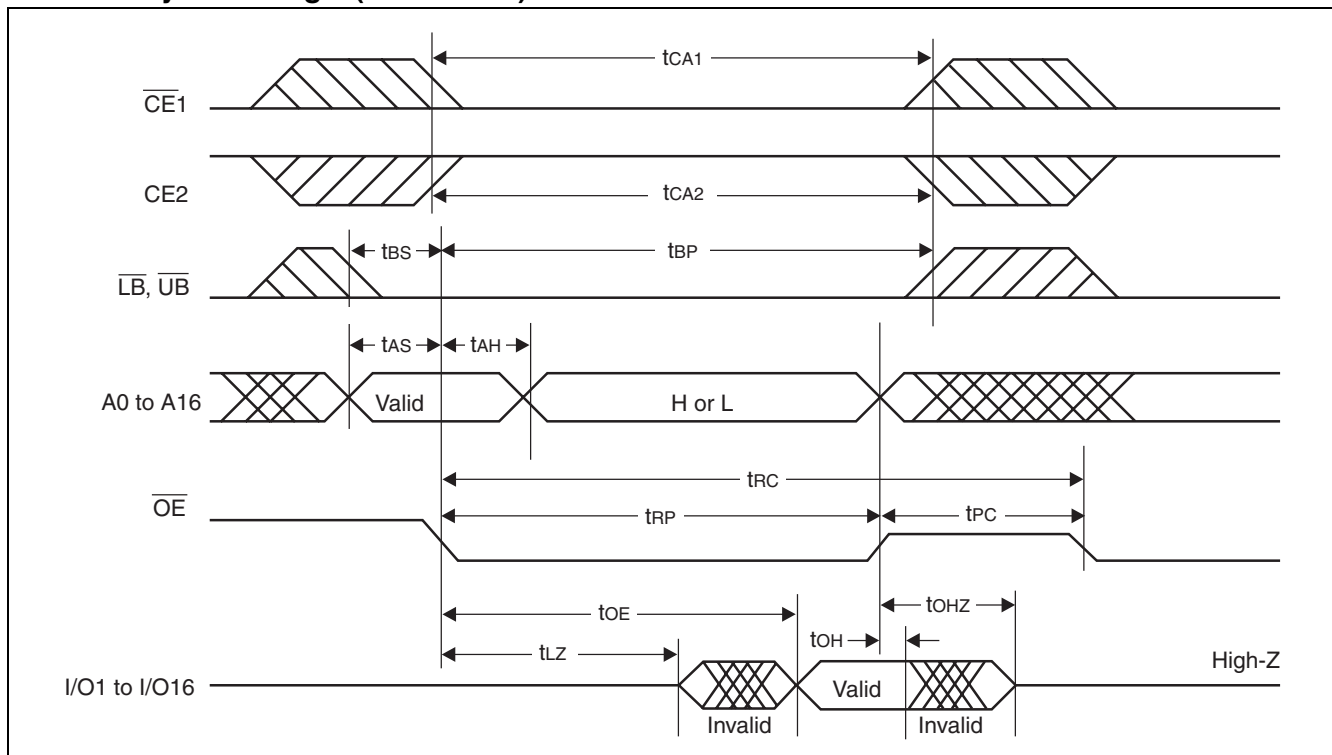
Parameter	Symbol	Test Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	$C_{IN}$	$V_{IN} = GND$	—	—	10	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = GND$	—	—	10	pF

## ■ TIMING DIAGRAMS

### 1. Read Cycle Timing 1 ( $\overline{\text{CE}}1$ , CE2 Control)

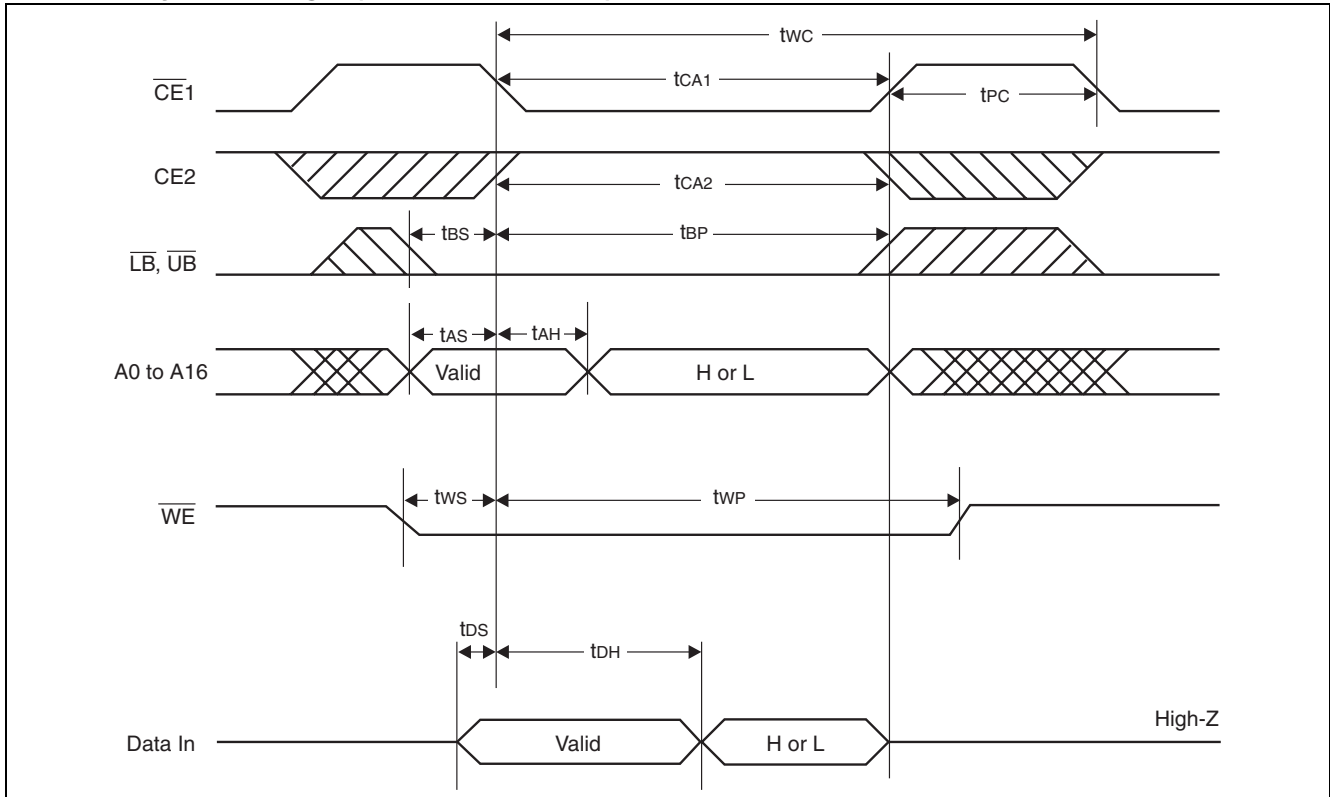


### 2. Read Cycle Timing 2 ( $\overline{\text{OE}}$ Control)

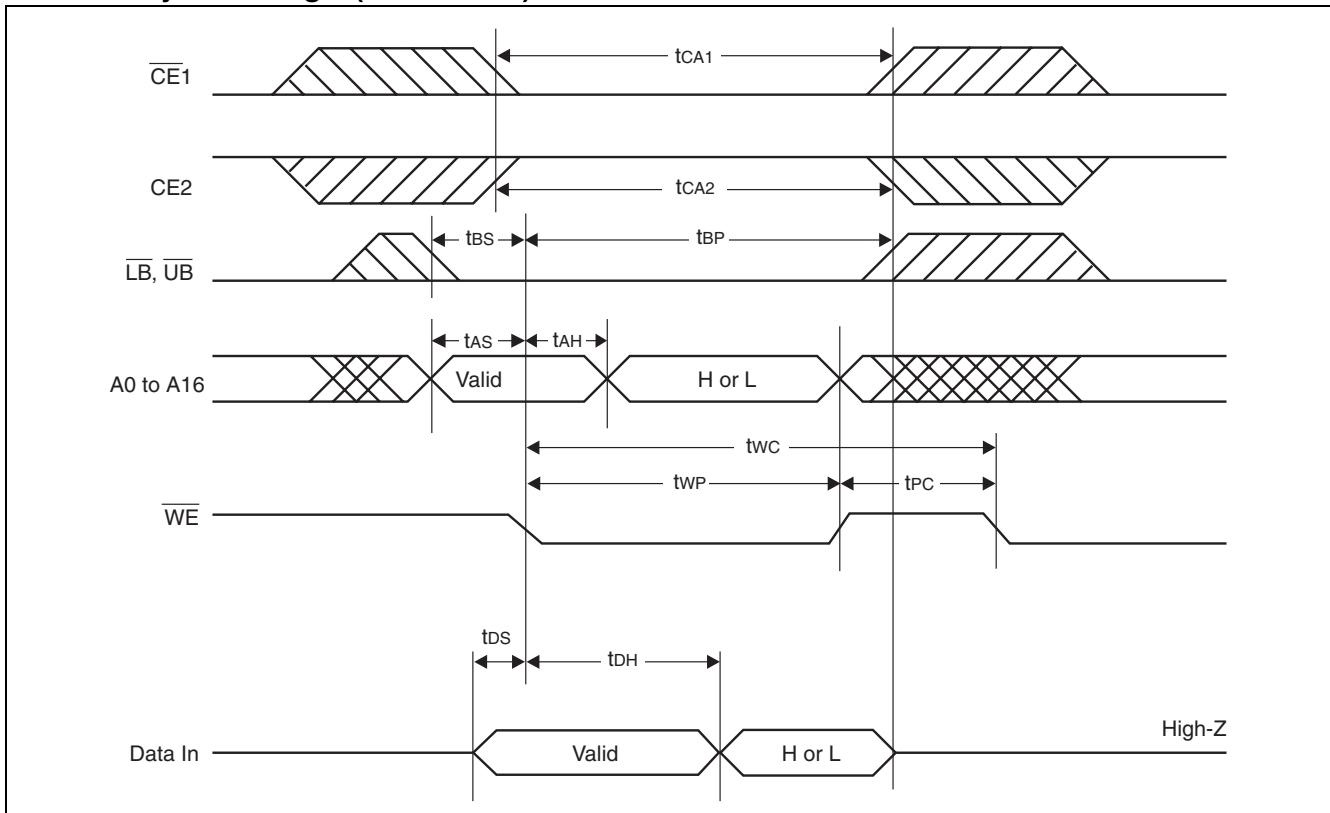




### 3. Write Cycle Timing 1 ( $\overline{\text{CE1}}$ , CE2 Control)



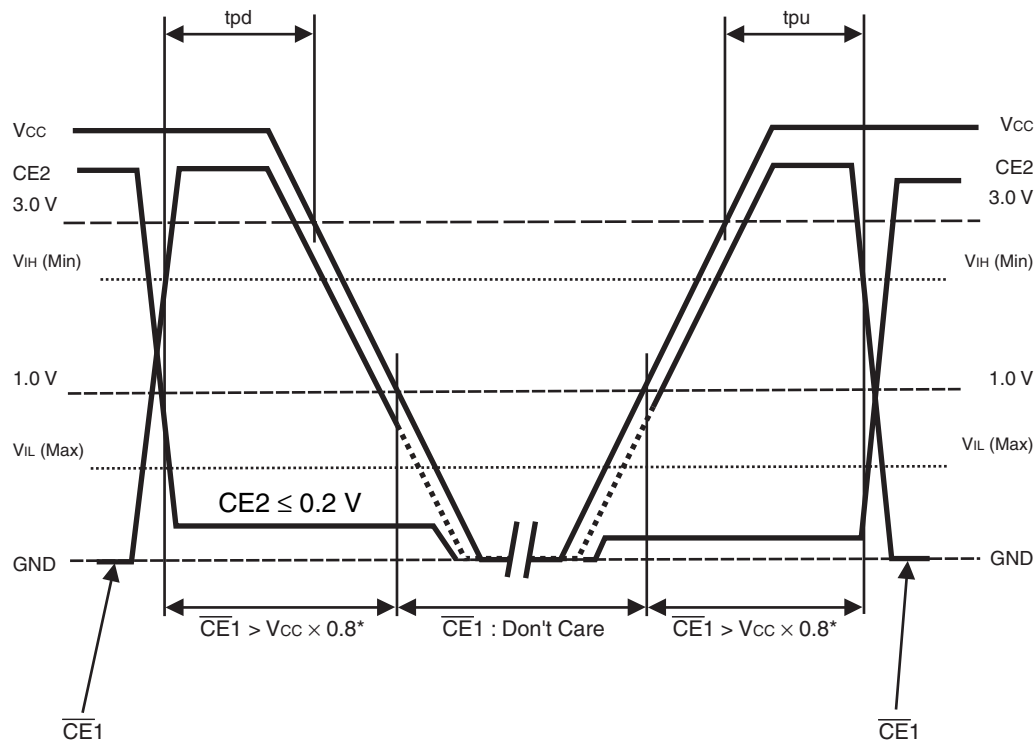
### 4. Write Cycle Timing 2 ( $\overline{\text{WE}}$ Control)



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## ■ POWER ON/OFF SEQUENCE



\* :  $\overline{CE1} (Max) < V_{CC} + 0.5 V$

Note : You can choose either of  $\overline{CE1}$  or  $CE2$ , or both for disenable control of the device.

## ■ NOTES ON USE

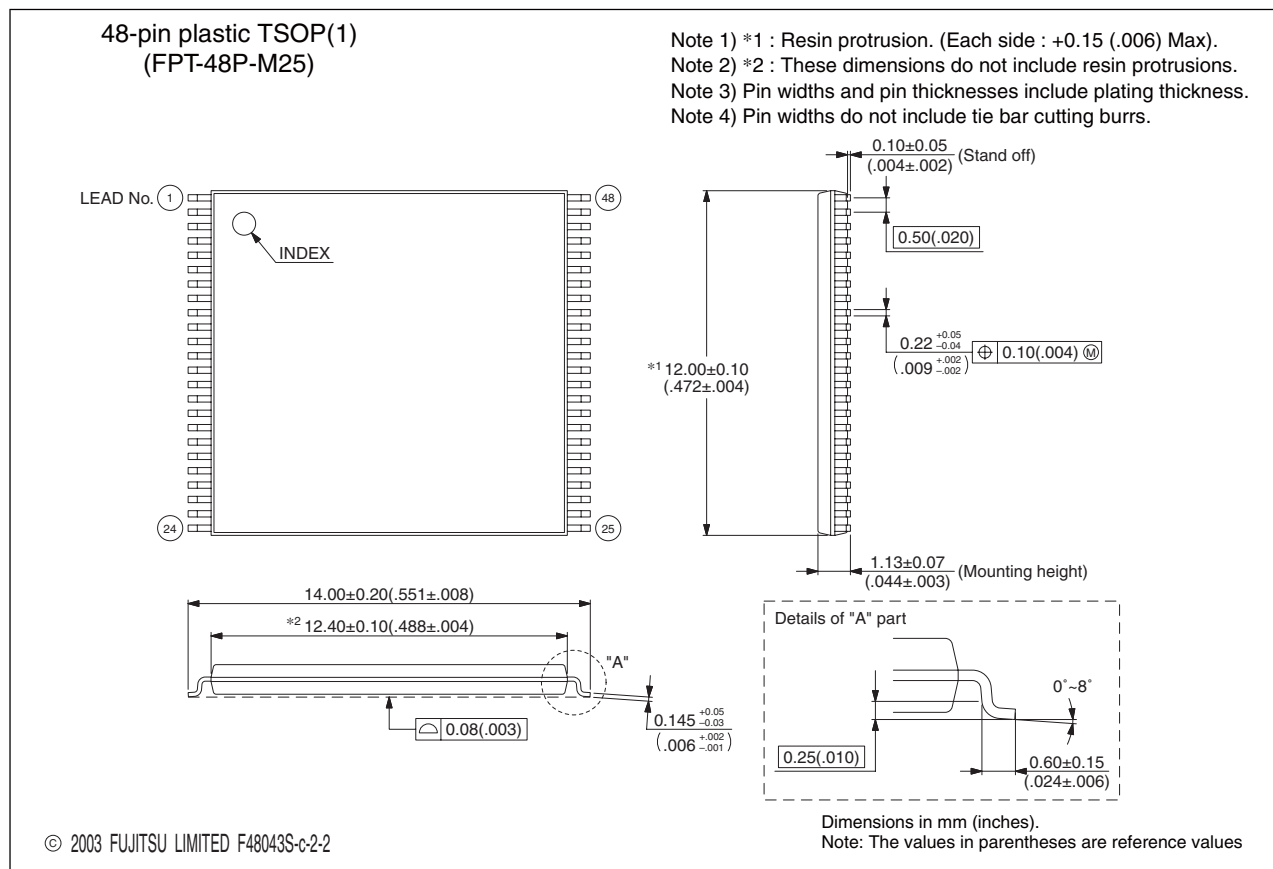
Data that is written prior to IR reflow is not guaranteed to be retained after IR reflow.

## ■ ORDERING INFORMATION

Part number	Package
MB85R2002PFTN-GE1	48-pin plastic TSOP(1) (FPT-48P-M25)

## ■ PACKAGE DIMENSIONS

<p>48-pin plastic TSOP(1)</p> <p>(FPT-48P-M25)</p>	Lead pitch	0.50 mm
	Package width × package length	12.00 × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.37 g
	Code (Reference)	P-TSOP(1)48-12×12.4-0.50



Please confirm the latest Package dimension by following URL.  
<http://edevic.fujitsu.com/fj/DATASHEET/ef-ovpkiv.html>

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