REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to 1.3 and I_{CC} test in table I. In accordance with N.O.R. 5962-R132-93.	93-05-05	M. A. FRYE
B	Make changes to V_{OUT} and C_{IN} tests in table I. In accordance with N.O.R. 5962-R141-94.	94-03-31	M. A. FRYE
C	Make change to CMRR test in table I. In accordance with N.O.R. 5962-R026-95.	94-10-28	M. A. FRYE
D	Make change final electrical parameters in table II. In accordance with N.O.R. 5962-R192-95.	95-08-25	M. A. FRYE
E	Make changes to $+I_{IN}$, $-I_{IN}$, V_{IO}, I_{CC}, PSRR, CMRR, SSBW, GFPL, GFPH, GFR, HD2, HD3, and SR tests in table I. Redrawn.	96-11-13	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	E	E	E																
SHEET	15	16	17																

REV STATUS OF SHEETS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
RICK OFFICER

CHECKED BY
RAJESH PITHADIA

APPROVED BY
RAYMOND MONNIN

DRAWING APPROVAL DATE
91-11-04

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, LINEAR, OPERATIONAL AMPLIFIER, HIGH SPEED, PROGRAMMABLE SUPPLY CURRENT, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90993

SHEET 1 OF 17

DESC FORM 193
JUL 94

9004708 0025354 888

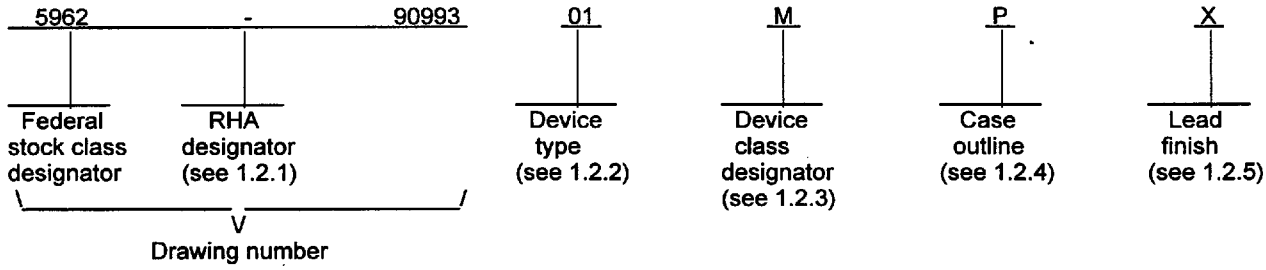
5962-E031-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	CLC505	High-speed programmable supply current operational amplifier

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage (V_S)	±7 V dc
Output current (I_{OUT})	70 mA
Common mode input voltage (V_{CM})	±7 V dc
Differential input voltage (V_{ID})	10 V dc
Power dissipation (P_D)	1.2 W
Junction temperature	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-ambient (Θ_{JA})	100°C/W
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_S)	±5 V dc
Gain range (A_V)	+2 to +21 and -1 to -20
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input bias current (noninverting)	$+I_{IN}$	I_{CC} = 9 mA, 2/ R_P = 33 kΩ, R_L = 250 Ω	1,2	01	-18	+18	µA
			3		-36	+36	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1,2		-6	+6	
			3		-12	+12	
		I_{CC} = 1 mA, 2/ R_P = 300 kΩ, R_L = 1 kΩ	1		-2.5	+2.5	
			2		-3.0	+3.0	
			3		-5	+5	
Input bias current (inverting)	$-I_{IN}$	I_{CC} = 9 mA, 2/ R_P = 33 kΩ, R_L = 250 Ω	1	01	-38	+38	µA
			2		-40	+40	
			3		-60	+60	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1		-14	+14	
			2		-15	+15	
			3		-22	+22	
		I_{CC} = 1 mA, 2/ R_P = 300 kΩ, R_L = 1 kΩ	1		-7	+7	
			2		-11	+11	
			3		-10	+10	
Input offset voltage	V_{IO}	I_{CC} = 9 mA, 2/ R_P = 33 kΩ, R_L = 250 Ω, R_S = 50 Ω	1	01	-8.0	+8.0	mV
			2		-14.0	+14.0	
			3		-12.8	+12.8	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω, R_S = 50 Ω	1		-7.0	+7.0	
			2		-13.0	+13.0	
			3		-12.8	+12.8	
		I_{CC} = 1 mA, 2/ R_P = 300 kΩ, R_L = 1 kΩ, R_S = 50 Ω	1		-7.0	+7.0	
			2		-14.5	+14.5	
			3		-13.0	+13.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Average +input bias 2/ current drift	T_C ($+I_{IN}$)	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	2	01	-100	+100	nA/°C
			3		-225	+225	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	2		-50	+50	
			3		-75	+75	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	2		-30	+30	
			3		-32	+32	
Average -input bias 2/ current drift	T_C ($-I_{IN}$)	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	2	01	-125	+125	nA/°C
			3		-275	+275	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	2		-60	+60	
			3		-100	+100	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	2		-35	+35	
			3		-38	+38	
Average offset voltage 2/ drift	T_C (V_{IO})	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	2,3	01	-50	+50	µV/°C
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω			-60	+60	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ			-75	+75	
Supply current	I_{CC}	R_P = 33 kΩ, no load 2/	1,3	01		11	mA
			2			12	
		R_P = 100 kΩ, no load	1,3			3.8	
			2			4.2	
		R_P = 300 kΩ, no load 2/	1			1.3	
			2,3			1.4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply rejection 3/ ratio	PSRR	I_{CC} = 9 mA, 2/ R_P = 33 kΩ, R_L = 250 Ω	1	01	48		dB
			2,3		45		
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1		48		
			2,3		45		
		I_{CC} = 1 mA, 2/ R_P = 300 kΩ, R_L = 1 kΩ	1		48		
			2,3		45		
Common mode rejection 2/ ratio	CMRR	I_{CC} = 9 mA, V_{CM} = ±1 V, R_P = 33 kΩ, R_L = 250 Ω	4	01	48		dB
			5,6		45		
		I_{CC} = 3.4 mA, V_{CM} = ±1 V, R_P = 100 kΩ, R_L = 500 Ω	4		48		
			5,6		45		
		I_{CC} = 1 mA, V_{CM} = ±1 V, R_P = 300 kΩ, R_L = 1 kΩ	4		48		
			5,6		45		
Input resistance 2/	$+R_{IN}$	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	1	01	800		kΩ
			2		1600		
			3		400		
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1		2		MΩ
			2		4		
			3		1		
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	1		5		
			2		10		
			3		2.5		
Output impedance at dc 2/	R_{OUT}	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	1	01		0.3	Ω
			2			0.2	
			3			1.2	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1			0.5	
			2			0.2	
			3			1.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output impedance at dc 2/	R_{OUT}	I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	1	01		1.0	Ω
			2			0.5	
			3			3.0	
Input capacitance 2/	C_{IN}	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω, See 4.4.1c, T_A = +25°C	4	01		2	pF
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω, See 4.4.1c, T_A = +25°C				2	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ, See 4.4.1c, T_A = +25°C				2	
Output voltage swing 4/	V_{OUT}	I_{CC} = 9 mA, 2/ R_P = 33 kΩ, R_L = 250 Ω	4,5	01	2.7		V
			6		2.5		
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4,5		2.7		
			6		2.5		
		I_{CC} = 1 mA, 2/ R_P = 300 kΩ, R_L = 1 kΩ	4,5		2.5		
			6		1.2		
Output current 2/	I_{OUT}	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	1	01	36		mA
			2		36		
			3		18		
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1		18		
			2		18		
			3		9		
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	1		5		
			2		5		
			3		2.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Common mode input 2/ voltage range	CMIR	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	1	01	-1.8	+1.8	V
			2		-2.0	+2.0	
			3		-1.5	+1.5	
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	1		-1.8	+1.8	
			2		-2.0	+2.0	
			3		-1.5	+1.5	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	1		-1.8	+1.8	
			2		-2.0	+2.0	
			3		-1.5	+1.5	
Small signal bandwidth	SSBW	-3 dB bandwidth, 2/ $V_{OUT} < 2\ V_{PP}$, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4	01	115		MHz
			5		100		
			6		115		
		-3 dB bandwidth, $V_{OUT} < 2\ V_{PP}$, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4		80		
			5 2/		65		
			6 2/		80		
		-3 dB bandwidth, 2/ $V_{OUT} < 2\ V_{PP}$, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4		35		
			5,6		30		
Large signal bandwidth 2/	LSBW	-3 dB bandwidth, $V_{OUT} < 5\ V_{PP}$, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,6	01	95		MHz
			5		80		
		-3 dB bandwidth, $V_{OUT} < 5\ V_{PP}$, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4,6		50		
			5		40		
		-3 dB bandwidth, $V_{OUT} < 5\ V_{PP}$, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4		20		
			5		18		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain flatness peaking low	GFPL	0.1 MHz to 25 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 9$ mA, $R_P = 33$ kΩ, $R_L = 250$ Ω	4	01		0.3	dB
			5,6			0.4	
		0.1 MHz to 20 MHz, $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 3.4$ mA, $R_P = 100$ kΩ, $R_L = 500$ Ω	4			0.2	
			5,6 2/			0.3	
		0.1 MHz to 10 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 1$ mA, $R_P = 300$ kΩ, $R_L = 1$ kΩ	4			0.1	
			5,6			0.2	
Gain flatness peaking high	GFPH	> 25 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 9$ mA, $R_P = 33$ kΩ, $R_L = 250$ Ω	4	01		0.5	dB
			5,6			0.6	
		> 20 MHz, $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 3.4$ mA, $R_P = 100$ kΩ, $R_L = 500$ Ω	4			0.4	
			5,6 2/			0.5	
		> 10 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 1$ mA, $R_P = 300$ kΩ, $R_L = 1$ kΩ	4			0.2	
			5,6			0.3	
Gain flatness rolloff	GFR	0.1 MHz to 50 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 9$ mA, $R_P = 33$ kΩ, $R_L = 250$ Ω	4,6	01		1.0	dB
			5			1.3	
		0.1 MHz to 40 MHz, $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 3.4$ mA, $R_P = 100$ kΩ, $R_L = 500$ Ω	4			1.0	
			5 2/			1.3	
			6 2/			1.0	
		0.1 MHz to 20 MHz, 2/ $V_{OUT} < 2\ V_{PP}$, $I_{CC} = 1$ mA, $R_P = 300$ kΩ, $R_L = 1$ kΩ	4,6			1.0	
			5			1.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Linear phase deviation 2/	LPD	< 50 MHz, V_{OUT} = 2 V_{PP}, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,6	01	1.0		Degree
			5		1.2		
		< 40 MHz, V_{OUT} = 2 V_{PP}, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4,6		1.0		
			5		1.2		
		< 20 MHz, V_{OUT} = 2 V_{PP}, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4,6		0.8		
			5		1.0		
2nd harmonic distortion	HD2	2 V_{PP} at 20 MHz, 2/ V_{OUT} = 2 V_{PP}, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,5	01		-45	dBc
			6			-40	
		2 V_{PP} at 10 MHz, V_{OUT} = 2 V_{PP}, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4			-45	
			5 2/			-45	
			6 2/			-40	
		2 VPP at 5 MHz, 2/ V_{OUT} = 2 V_{PP}, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4,5			-45	
			6			-40	
3rd harmonic distortion	HD3	2 V_{PP} at 20 MHz, 2/ V_{OUT} = 2 V_{PP}, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,5,6	01		-55	dBc
		2 V_{PP} at 10 MHz, V_{OUT} = 2 V_{PP}, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4			-55	
			5,6 2/			-55	
		2 VPP at 5 MHz, 2/ V_{OUT} = 2 V_{PP}, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4,5,6			-55	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Noise floor 2/ 5/	NF	> 1 MHz, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,6	01		-154	dBm (1 Hz)
			5			-153	
		> 1 MHz, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4,6			-153	
			5			-152	
		>1 MHz, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4,6			-150	
			5			-149	
Integrated noise 2/ 5/	INV	1 MHz to 200 MHz, I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω	4,6	01		65	µV
			5			70	
		1 MHz to 200 MHz, I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω	4,6			70	
			5			80	
		1 MHz to 100 MHz, I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ	4,6			70	
			5			80	
Slew rate 2/	SR	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω, A_V = +2, V_{OUT} = 3 V, measured at ±1 V	9,10	01	1200		V/µs
			11		1000		
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω, A_V = +2, V_{OUT} = 3 V, measured at ±1 V	9,10		800		
			11		700		
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ, A_V = +2, V_{OUT} = 3 V, measured at ±1 V	9,10		600		
			11		500		
Settling time 2/	t_S	I_{CC} = 9 mA, R_P = 33 kΩ, R_L = 250 Ω, 2 V step at ±0.1% of the fixed value	9,10,11	01		16	ns
		I_{CC} = 3.4 mA, R_P = 100 kΩ, R_L = 500 Ω, 2 V step at ±0.05% of the fixed value	9,10,11			22	
		I_{CC} = 1 mA, R_P = 300 kΩ, R_L = 1 kΩ, 2 V step at ±0.05% of the fixed value	9,10			60	
			11			70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Rise and fall time 2/	t_F	I_{CC} = 9 mA, 2 V step, R_P = 33 kΩ, R_L = 250 Ω	9,11	01		3.0	ns
			10			3.5	
	t_R	I_{CC} = 9 mA, 5 V step, R_P = 33 kΩ, R_L = 250 Ω	9,11			3.7	
			10			4.4	
	t_F	I_{CC} = 3.4 mA, 2 V step, R_P = 100 kΩ, R_L = 500 Ω	9,11			4.4	
			10			5.4	
	t_R	I_{CC} = 3.4 mA, 5 V step, R_P = 100 kΩ, R_L = 500 Ω	9,11			7.0	
			10			8.8	
	t_F	I_{CC} = 1 mA, 2 V step, R_P = 300 kΩ, R_L = 1 kΩ	9			10	
			10,11			12	
	t_R	I_{CC} = 1 mA, 5 V step, R_P = 300 kΩ, R_L = 1 kΩ	9			18	
			10,11			20	
Overshoot 2/	OS	I_{CC} = 9 mA, 2 V step, R_P = 33 kΩ, R_L = 250 Ω	9	01		12	%
			10,11			15	
		I_{CC} = 3.4 mA, 2 V step, R_P = 100 kΩ, R_L = 500 Ω	9			10	
			10,11			12	
		I_{CC} = 1 mA, 2 V step, R_P = 300 kΩ, R_L = 1 kΩ	9			5	
			10,11			8	

1/ Unless otherwise specified, V_S = ±5 V dc, R_L is load resistance, R_P is programming resistance, feedback resistance (R_F) = 1000 Ω, peak capacitance (C_P) = 100 pF, and A_V = +6.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

3/ -V = -4.5 V to -5.0 V and +V = +4.5 V to +5.0 V.

4/ Group A tested only.

5/ Noise tests are performed from 1 MHz to 200 MHz for I_{CC} = 9 mA, 1 MHz to 200 MHz for I_{CC} = 3.4 mA, and 1 MHz to 100 MHz for I_{CC} = 1 mA.

Device type	01
Case outline	P
Terminal number	Terminal symbol
1	NC
2	-INPUT
3	+INPUT
4	$-V_S$
5	NC
6	V_{OUT}
7	$+V_S$
8	R_P

NC = No connection

FIGURE 1. Terminal connections.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3 1/	1,2,3 1/	1,2,3 1/
Group A test requirements (see 4.4)	1,2,3,4,5,6, 2/ 9,10,11	1,2,3,4,5,6,9, 10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.
2/ Subgroups 9, 10, and 11, if not tested, shall be guaranteed to the limits specified in table I.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 96-11-13

Approved sources of supply for SMD 5962-90993 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9099301MPC	62839	CLC505A8D

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
62839	Comlinear Corporation 4800 Wheaton Drive Fort Collins, CO 80525

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.