

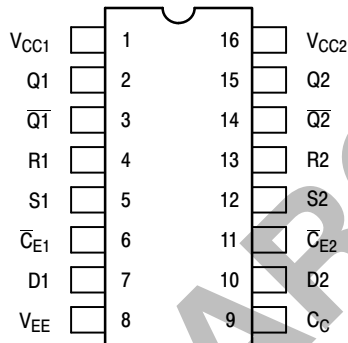
Dual Type D Master-Slave Flip-Flop

The MC10131 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

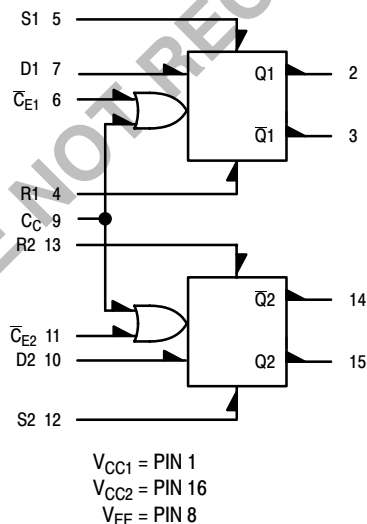
The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

- $P_D = 235 \text{ mW typ/pkg (No Load)}$
- $F_{Tog} = 160 \text{ MHz typ}$
- $t_{pd} = 3.0 \text{ ns typ}$
- $t_r, t_f = 2.5 \text{ ns typ (20\%–80\%)}$

DIP PIN ASSIGNMENT



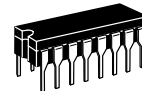
LOGIC DIAGRAM



ON Semiconductor

<http://onsemi.com>

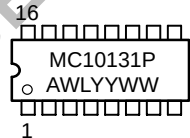
MARKING DIAGRAMS



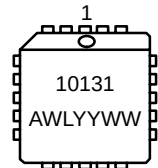
CDIP-16
L SUFFIX
CASE 620



PDIP-16
P SUFFIX
CASE 648



PLCC-20
FN SUFFIX
CASE 775



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	X	Q_n
H	L	L
H	H	H

$C = C_E + C_C$. A clock H is a clock transition from a low to a high state.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

ORDERING INFORMATION

Device	Package	Shipping
MC10131L	CDIP-16	25 Units / Rail
MC10131P	PDIP-16	25 Units / Rail
MC10131FN	PLCC-20	46 Units / Rail

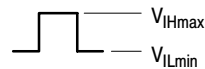
MC10131

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			−30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I _E	8		62		45	56		62	mAdc
Input Current	I _{inH}	4		525			330		330	μAdc
		5		525			330		330	
		6		350			220		220	
		7		390			245		245	
		9		425			265		265	
	I _{inL}	4, 5* 6, 7, 9*	0.5 0.5		0.5 0.5			0.3 0.3		μAdc
Output Voltage Logic 1	V _{OH}	2 2†	−1.060 −1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc
Output Voltage Logic 0	V _{OL}	2 3†	−1.890 −1.890	−1.675 −1.675	−1.850 −1.850		−1.650 −1.650	−1.825 −1.825	−1.615 −1.615	Vdc
Threshold Voltage Logic 1	V _{OHA}	2 2†	−1.080 −1.080		−0.980 −0.980			−0.910 −0.910		Vdc
Threshold Voltage Logic 0	V _{OLA}	2 3†		−1.655 −1.655			−1.630 −1.630		−1.595 −1.595	Vdc
Switching Times (50Ω Load) Clock Input										ns
Propagation Delay	t _{9+2−}	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	
	t ₉₊₂₊	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	
	t ₆₊₂₊	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	
	t _{6+2−}	2	1.7	4.6	1.8	3.0	4.5	1.8	5.0	
Rise Time (20 to 80%)	t ₂₊	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Fall Time (20 to 80%)	t _{2−}	2	1.0	4.6	1.1	2.5	4.5	1.1	4.9	
Set Input										ns
Propagation Delay	t ₅₊₂₊	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t ₁₂₊₁₅₊	15	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t _{5+3−}	3	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t _{12+14−}	14	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
Reset Input										ns
Propagation Delay	t _{4+2−}	2	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t _{13+15−}	15	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t _{4+3−}	3	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
	t ₁₃₊₁₄₊	14	1.7	4.4	1.8	2.8	4.3	1.8	4.8	
Setup Time	t _{setup}	7	2.5		2.5			2.5		ns
Hold Time	t _{hold}	7	1.5		1.5			1.5		ns
Toggle Frequency (Max)	f _{tog}	2	125		125	160		125		MHz

* Individually test each input applying V_{IH} or V_{IL} to input under test.

† Output level to be measured after a clock pulse has been applied to the $\overline{C}_E$ Input (Pin 6)



ELECTRICAL CHARACTERISTICS (continued)

* Individually test each input applying V_{IH} or V_{IL} to input under test.

A timing diagram for the input signal V_I . It shows a square wave signal that transitions between a high level labeled V_{IHmax} and a low level labeled V_{ILmin} . The signal is high for a duration t_{1H} and low for a duration t_{1L} .

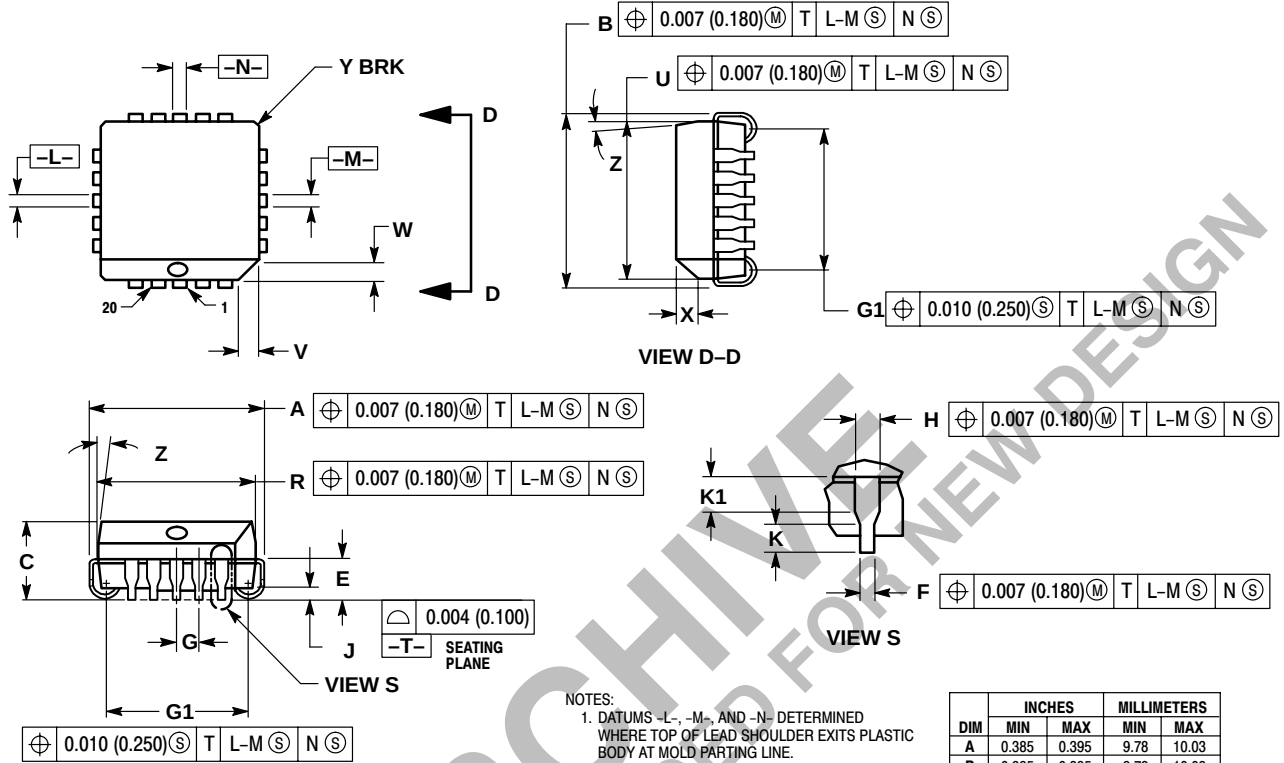
<http://onsemi.com>

MC10131

查询"MC10131-D"供应商

PACKAGE DIMENSIONS

PLCC-20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C

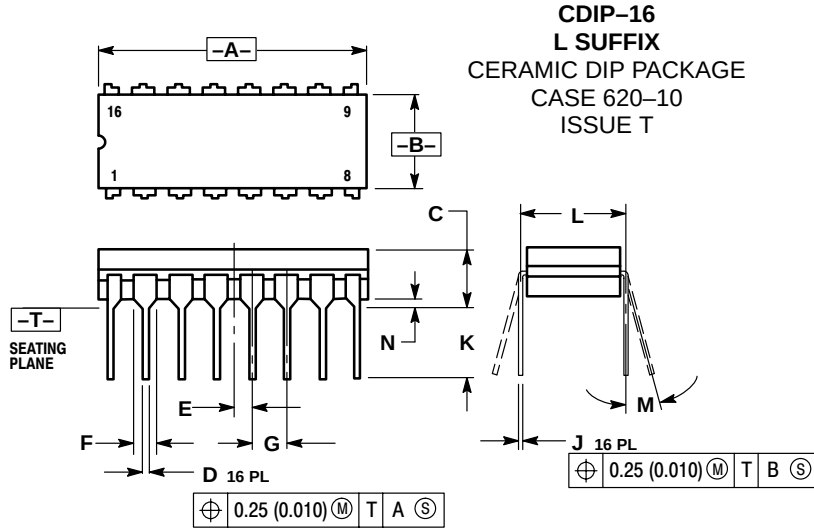


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

MC10131

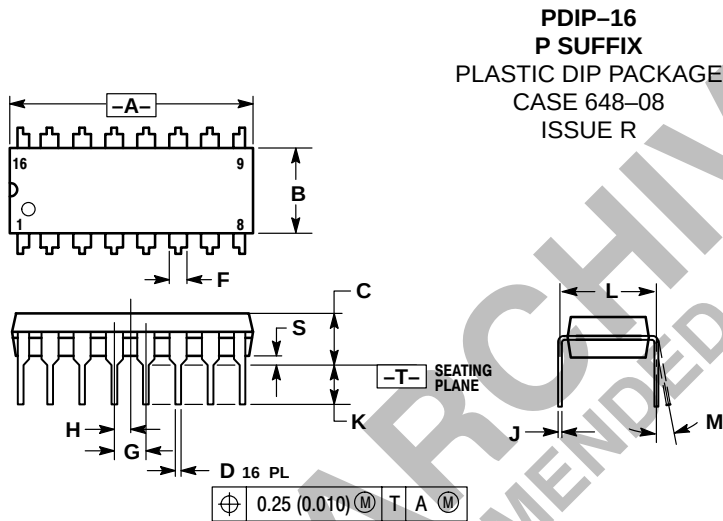
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PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

Notes
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DEVICE NOT RECOMMENDED FOR NEW DESIGN

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