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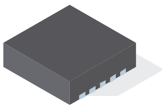


bq24020, bq24022, bq24023
bq24024, bq24025, bq24026
bq24027

SLUS549D – DECEMBER 2002 – REVISED MARCH 2006

SINGLE-CHIP, LI-ION AND LI-POL CHARGER IC WITH AUTONOMOUS USB-PORT AND AC-ADAPTER SUPPLY MANAGEMENT (bqTINY™-II)

FEATURES

- **Small 3 mm x 3 mm MLP Package**
- **Charges and powers Systems from Either AC Adapter or USB With Autonomous power-Source Selection**
- **Integrated USB Control With Selectable 100 mA and 500 mA Charge Rates**
- **Ideal for Low-Dropout Charger Designs for Single-Cell Li-Ion or Li-pol Packs in Space Limited portable applications**
- **Integrated power FET and Current Sensor for Up to 1-A Charge applications From AC Adapter**
- **Precharge Conditioning With Safety Timer**
- **power Good (AC Adapter Present) Status Output**
- **Optional Battery Temperature Monitoring Before and During Charge**
- **Automatic Sleep Mode for Low-power Consumption**

APPLICATIONS

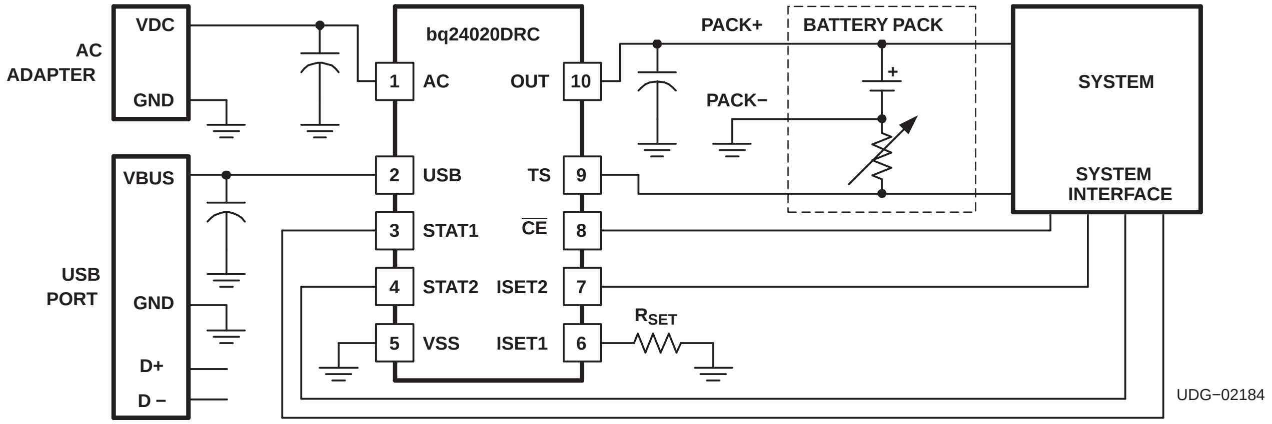
- **PDAs, MP3 Players**
- **Digital Cameras**
- **Internet appliances**
- **Smartphones**

DESCRIPTION

The bqTINY-II series are highly-integrated, flexible Li-Ion linear charge and system power management devices for space-limited charger applications. In a single monolithic device, the bqTINY-II offers integrated USB-port and ac-adapter supply management with autonomous power-source selection, power-FET and current-sensor interfaces, high-accuracy current and voltage regulation, charge status, and charge termination.

The bqTINY-II automatically selects the USB-port or the ac-adapter as the power source for the system. In the USB configuration, the host can select from two preset charge rates of 100 mA or 500 mA. In the ac-adapter configuration, an external resistor sets the system or charge current.

The bqTINY-II charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination. The bqTINY-II automatically restarts the charge if the battery voltage falls below an internal threshold. The bqTINY-II automatically enters sleep mode when both supplies are removed.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Different versions of the bqTINY-II offer many additional features. These include a temperature-sensor input for detecting hot or cold battery packs, a power-good output ($\overline{\text{PG}}$) indicating the presence of input power, a TTL-level charge-enable input ($\overline{\text{CE}}$) used to disable or enable the charge process, and a TTL-level timer and taper-detect enable input ($\overline{\text{TTE}}$) used to disable or enable the fast-charge timer and charge termination.

ORDERING INFORMATION

T_J	CHARGE REGULATION VOLTAGE (V)(1)	OPTIONAL FUNCTIONS(1)	FAST-CHARGE TIMER (Hours)	TAPER TIMER	USB TAPER THRESHOLD	PART NUMBER(2)	MARKINGS
–40°C to 125°C	4.2	$\overline{\text{CE}}$ and TS	5	Yes	10% of ISET1 Level	bq24020DRCR	AZS
	4.2	$\overline{\text{PG}}$ and $\overline{\text{CE}}$	5	Yes	10% of ISET1 Level	bq24022DRCR	AZU
	4.2	$\overline{\text{CE}}$ and $\overline{\text{TTE}}$	5	Yes	10% of ISET1 Level	bq24023DRCR	AZV
	4.2	$\overline{\text{TTE}}$ and TS	5	Yes	10% of ISET1 Level	bq24024DRCR	AZW
	4.2	$\overline{\text{CE}}$ and TS	7	Yes	10% of ISET1 Level	bq24025DRCR	AZX
	4.2	$\overline{\text{TE}}$ and TS	7	No	10% of selected USB charge rate	bq24026DRCR	ANR
	4.2	$\overline{\text{PG}}$ and $\overline{\text{CE}}$	7	No	10% of selected USB charge rate	bq24027DRCR	ANS

(1) The DRC package is available taped and reeled only in quantities of 3,000 devices per reel.

Dissipation Ratings

PACKAGE	θ_{JA}	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
DRC(1)	46.87 °C/W	1.5 W	0.021 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		bq24020, bq24022, bq24023, bq24024 bq24025, bq24026 bq24027	UNIT
Input voltage(2)	AC, $\overline{\text{CE}}$, ISET1, ISET2, OUT, $\overline{\text{PG}}$, STAT1, STAT2, $\overline{\text{TE}}$, TS, $\overline{\text{TTE}}$, USB	–0.3 to 7.0	V
Output sink/source current	STAT1, STAT2, $\overline{\text{PG}}$	15	mA
Output current	TS	200	μA
Output current	OUT	1.5	A
Operating free-air temperature range, T_A		–40 to 125	°C
Junction temperature range, T_J			
Storage temperature, T_{stg}		–65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (from AC input), V_{CC}	4.5		6.5	V
Supply voltage (from USB input), V_{CC}	4.35		6.5	V
Operating junction temperature range, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT							
$I_{CC}(V_{CC})$	V_{CC} current	$V_{CC} > V_{CC(min)}$			1.2	2.0	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT pin, $V_{CC} < V_{(SLP)}$			2	5	µA
$I_{CC(STBY)}$	Standby current	CE = High	0°C ≤ T_J ≤ 85°C		1	150	
$II_{B(OUT)}$	Input current on OUT pin	Charge DONE	$V_{CC} > V_{CC(MIN)}$			5	
$II_{B(CE)}$	Input current on CE pin					1	
$II_{B(TTE)}$	Input bias current on TTE pin					1	
$II_{B(TE)}$	Input bias current on TE pin					1	
VOLTAGE REGULATION $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$, $I_{(TERM)} < I_{O(OUT)} \le 1$ A							
$V_{O(REG)}$	Output voltage,				4.20		V
	Voltage regulation accuracy	T_A = 25°C		–0.35%		0.35%	
				–1%		1%	
$V_{(DO)}$	AC dropout voltage ($V_{(AC)}$–$V_{(OUT)}$)	$V_{O(OUT)} = V_{O(REG)}$ $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$	$I_{O(OUT)}$ = 1A		350	500	mV
$V_{(DO)}$	USB dropout voltage ($V_{(USB)} - V_{(OUT)}$)	$V_{O(OUT)} = V_{O(REG)}$ $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$	ISET2 = High		350	500	
		$V_{O(OUT)} = V_{O(REG)}$ $V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$	ISET2 = Low		60	100	
CURRENT REGULATION							
$I_{O(OUT)}$	AC output current range(1)	$V_{I(OUT)} > V_{(LOWV)}$ $V_{I(AC)} - V_{I(OUT)} > V_{(DO-MAX)}$	$V_{CC} \ge 4.5$ V	50		1000	mA
$I_{O(OUT)}$	USB output current range	$V_{CC(MIN)} \ge 4.5$ V $V_{USB} - V_{I(OUT)} > V_{(DO-MAX)}$	$V_{I(OUT)} > V_{(LOWV)}$ ISET2 = Low	80		100	
		$V_{CC(MIN)} \ge 4.5$ V $V_{USB} - V_{I(OUT)} > V_{(DO-MAX)}$	$V_{I(OUT)} > V_{(LOWV)}$ ISET2 = High	400		500	
$V_{(SET)}$	Output current set voltage	Voltage on ISET1 pin, $V_{CC} \ge 4.5$ V, $V_{IN} \ge 4.5$ V, $V_{I(OUT)} > V_{(LOWV)}$, $V_{IN} - V_{I(OUT)} > V_{(DO-MAX)}$		2.463	2.500	2.538	V
$K_{(SET)}$	Output current set factor	50 mA ≤ $I_{O(OUT)}$ ≤ 1 A		307	322	337	
		10 mA ≤ $I_{O(OUT)}$ < 50 mA		296	320	346	
		1 mA ≤ $I_{O(OUT)}$ < 10 mA		246	320	416	

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(1) $$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{SET}}$$

ELECTRICAL CHARACTERISTICS (continued)

over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION							
$V_{(LOWV)}$	Precharge to fast-charge transition threshold		Voltage on OUT pin	2.8	3.0	3.2	V
	Deglitch time for fast-charge to precharge transition		$V_{CC(MIN)} \geq 4.5$ V, t_{FALL} = 100 ns, 10 mV overdrive, $V_{I(OUT)}$ decreasing below threshold	250	375	500	ms
$I_{O(PRECHG)}$	Precharge range[2]		0 V < $V_{I(OUT)}$ < $V_{(LOWV)}$, t < $t_{(PRECHG)}$	5		100	mA
$V_{(PRECHG)}$	Precharge set voltage		Voltage on ISET1 pin 0 V < $V_{I(OUT)}$ > $V_{(LOWV)}$, $V_{O(REG)}$ = 4.2 V t < $t_{(PRECHG)}$	240	255	270	mV
CHARGE TAPER AND TERMINATION DETECTION							
$I_{(TAPER)}$	Charge taper detection range[3]		$V_{I(OUT)}$ > $V_{(RCH)}$, t < $t_{(TAPER)}$	5		100	mA
	USB-100 charge taper detection level	bq24026	$V_{I(OUT)}$ > $V_{(RCH)}$, ISET2 = Low	6.5	9	11	
	USB-500 charge taper detection level	bq24026	$V_{I(OUT)}$ > $V_{(RCH)}$, ISET2 = High	32	44	55	
$V_{(TAPER)}$	Charge taper detection set voltage		Voltage on ISET1 pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)}$ > $V_{(RCH)}$, t < $t_{(TAPER)}$	235	250	265	mV
$V_{(TERM)}$	Charge termination detection set voltage[4]		Voltage on ISET1 pin, $V_{O(REG)}$ = 4.2 V, $V_{I(OUT)}$ > $V_{(RCH)}$	11	18	25	
$t_{(TPRDET)}$	Deglitch time for TAPER detection		$V_{CC(MIN)} \geq 4.5$ V, t_{FALL} = 100 ns charging current increasing or decreasing above and below, 10 mV overdrive	250	375	500	ms
$t_{(TRMDET)}$	Deglitch time for termination detection		$V_{CC(MIN)} \geq 4.5$ V, t_{FALL} = 100 ns charging current decreasing below, 10 mV overdrive	250	375	500	
TEMPERATURE SENSE COMPARATOR							
$V_{(HTF)}$	High-voltage threshold		PTC thermistor	2.475	2.500	2.525	V
$V_{(LTF)}$	Low-voltage threshold		PTC thermistor	0.485	0.500	0.515	
$I_{(TS)}$	Current source			96	102	108	µA
$t_{(DEGL)}$	Deglitch time for temperature fault			250	375	500	ms

(2)
$$I_{O(PRECHG)} = \frac{\left(K_{(SET)} \times V_{(PRECHG)}\right)}{R_{SET}}$$

(3)
$$I_{O(TAPER)} = \frac{\left(K_{(SET)} \times V_{(TAPER)}\right)}{R_{SET}}$$

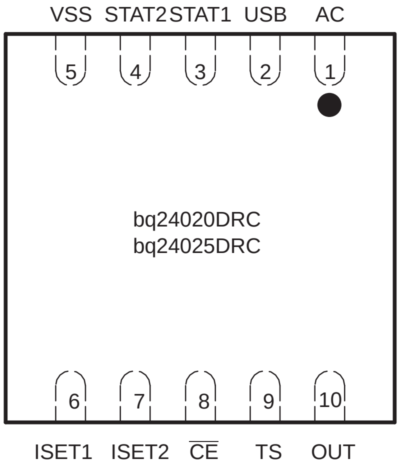
(4)
$$I_{O(TERM)} = \frac{\left(K_{(SET)} \times V_{(TERM)}\right)}{R_{SET}}$$

ELECTRICAL CHARACTERISTICS (continued)

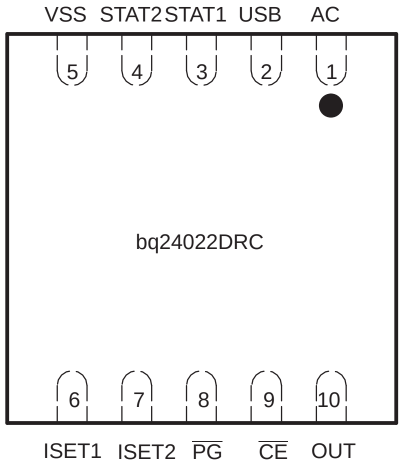
over 0°C ≤ T_J ≤ 125°C and recommended supply voltage, unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY RECHARGE THRESHOLD							
V_{RCH}	Recharge threshold			$V_{O(REG)}$ – 0.115	$V_{O(REG)}$ – 0.10	$V_{O(REG)}$ – 0.085	V
$t_{(DEGL)}$	Deglitch time for recharge detect		$V_{CC(MIN)} \geq 4.5$ V, t_{FALL} = 100 ns decreasing below or increasing above threshold, 10 mV overdrive	250	375	500	ms
	STAT1, STAT2, and PG OUTPUTS						
V_{OL}	Low-level output saturation voltage		I_O = 5 mA			0.25	V
	ISET2, CHARGE ENABLE (CE), TIMER AND TERMINATION ENABLE (TTE), AND TIMER ENABLE (TE) INPUTS						
V_{IL}	Low-level input voltage		I_{IL} = 10 µA	0		0.4	V
V_{IH}	High-level input voltage		I_{IL} = 20 µA	1.4			
II_L	CE, TE or TTE low-level input current			–1			µA
II_H	CE, TE or TTE high-level input current					1	
I_{IL}	ISET2 low-level input current		I_{ISET2} = 0	–20			
I_{IH}	ISET2 high-level input current		$I_{ISET2} = V_{CC}$			40	
I_{IH}	ISET2 high-Z input current					1	V
TIMERS							
$t_{(PRECHG)}$	Precharge time			1,620	1,800	1,930	s
$t_{(TAPER)}$	Taper time	bq24020 bq24022 bq24023 bq24024 bq24025		1,620	1,800	1,930	
$t_{(CHG)}$	Charge time	bq24020 bq24022 bq24023 bq24024		16,200	18,000	19,300	
		bq24025 bq24026 bq24027		22,680	25,200	27,720	
$I_{(FAULT)}$	Timer fault recovery current				200		µA
SLEEP COMPARATOR							
$V_{(SLP)}$	Sleep-mode entry threshold voltage		2.3 V ≤ $V_{I(OUT)} \leq V_{O(REG)}$			$V_{CC} \leq V_{I(OUT)}$ +80 mV	V
$V_{(SLPEXIT)}$	Sleep mode exit threshold voltage		2.3 V ≤ $V_{I(OUT)} \leq V_{O(REG)}$	$V_{CC} \geq V_{I(OUT)}$ +190mV			
	Sleep mode deglitch time		AC and USB decreasing below threshold, t_{FALL} = 100 ns, 10 mV overdrive	250	375	500	ms
THERMAL SHUTDOWN THRESHOLDS							
$T_{(SHTDWN)}$	Thermal trip threshold				165		°C
	Thermal hysteresis				15		
UNDERVOLTAGE LOCKOUT							
$V_{(UVLO)}$	Undervoltage lockout		Decreasing V_{CC}	2.4	2.5	2.6	V
	Hysteresis				27		mV

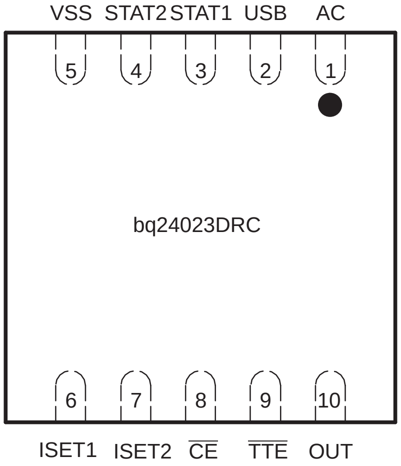
DRC PACKAGE
(TOP VIEW)



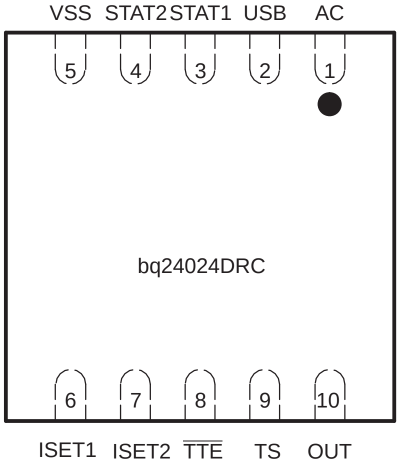
DRC PACKAGE
(TOP VIEW)



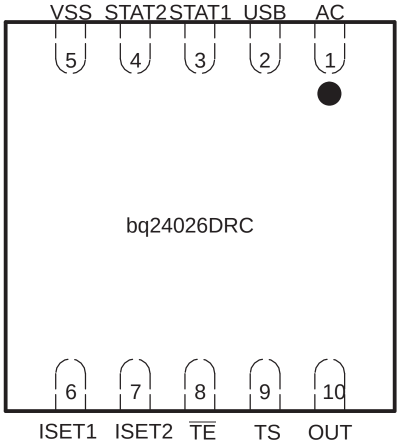
DRC PACKAGE
(TOP VIEW)



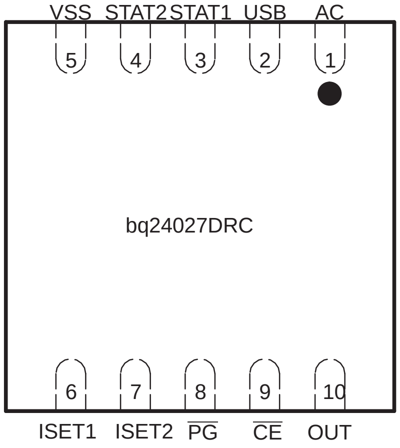
DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



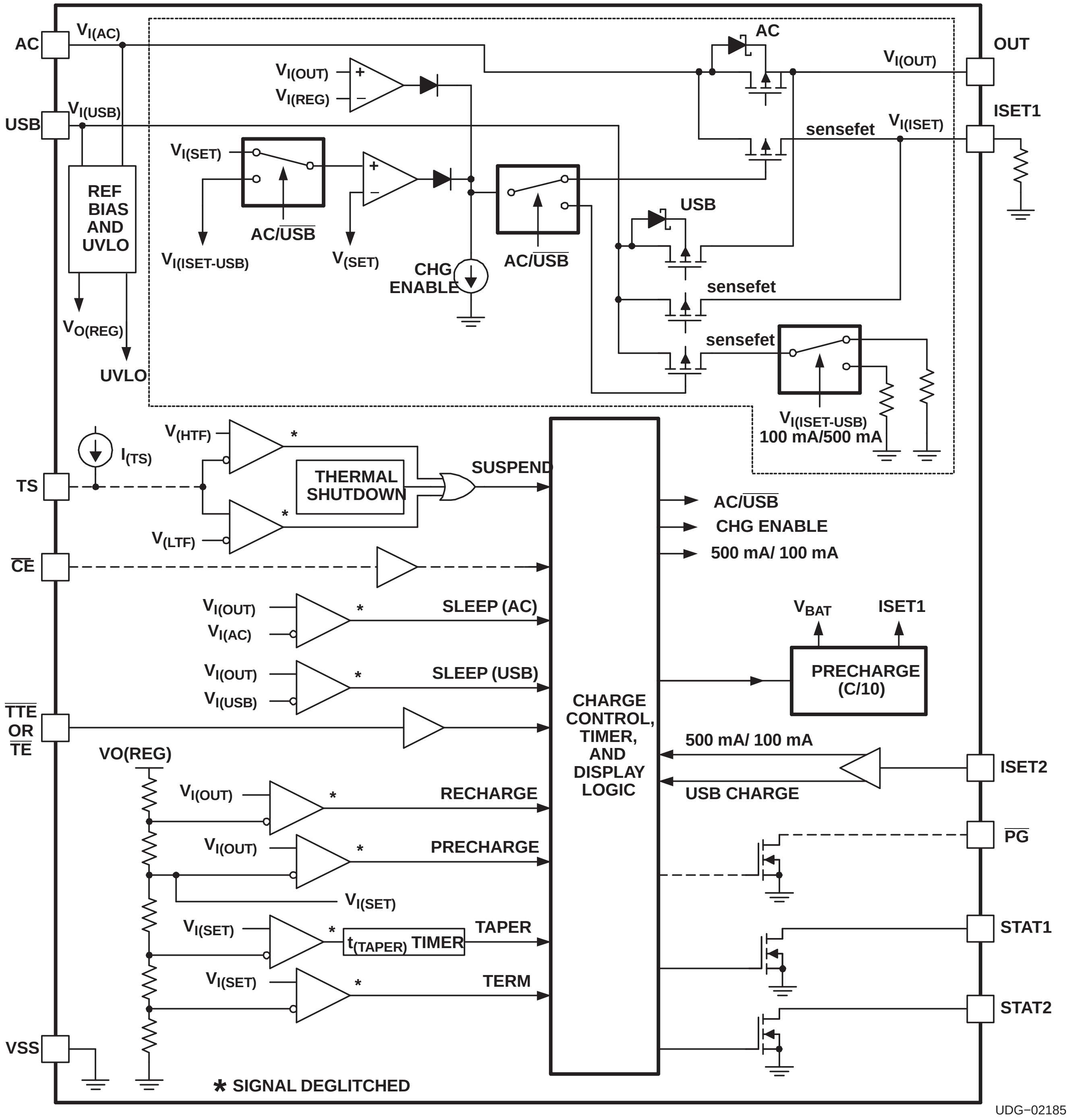
DRC PACKAGE
(TOP VIEW)



Terminal Functions

NAME	TERMINAL					I/O	DESCRIPTION
	bq24020 bq24025	bq24022 bq24027	bq24023	bq24024	bq24026		
AC	1	1	1	1	1	I	AC charge input voltage
$\overline{\text{CE}}$	8	9	8	-	-	I	Charge enable input (active low)
ISET1	6	6	6	6	6	I	Charge current set point for AC input and precharge and taper set point for both AC and USB
ISET2	7	7	7	7	7	I	Charge current set point for USB port (high=500 mA, low=100 mA, hi-z = disable USB charge)
OUT	10	10	10	10	10	O	Charge current output
$\overline{\text{PG}}$	-	8	-	-	-	O	powergood status output (active low)
STAT1	3	3	3	3	3	O	Charge status output 1 (open-drain)
STAT2	4	4	4	4	4	O	Charge status output 2 (open-drain)
$\overline{\text{TE}}$	-	-	-	-	8	I	Timer enable input (active low)
TS	9	-	-	9	9	I	Temperature sense input
$\overline{\text{TTE}}$	-	-	9	8	-	I	Timer and termination enable input (active low)
USB	2	2	2	2	2	I	USB charge input voltage
VSS	5	5	5	5	5	-	Ground input
Exposed Thermal Pad	pad	pad	pad	pad	pad	-	There is an internal electrical connection between the exposed thermal pad and VSS pin of the device. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. **Do not use the thermal pad as the primary ground input for the device.** VSS pin must be connected to ground at all times

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

AC DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

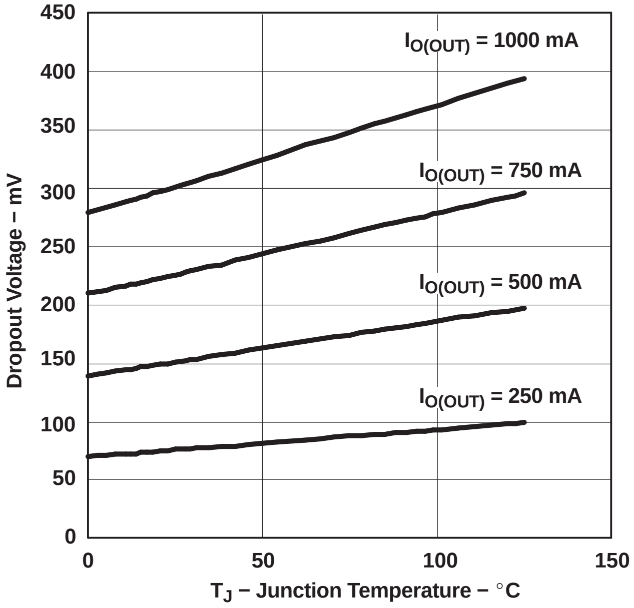


Figure 1.

The bqTINY-II supports a precision Li-Ion, Li-pol charging system suitable for single-cell packs. Figure 3 shows a typical charge profile, application circuit and Figure 4 shows an operational flow chart.

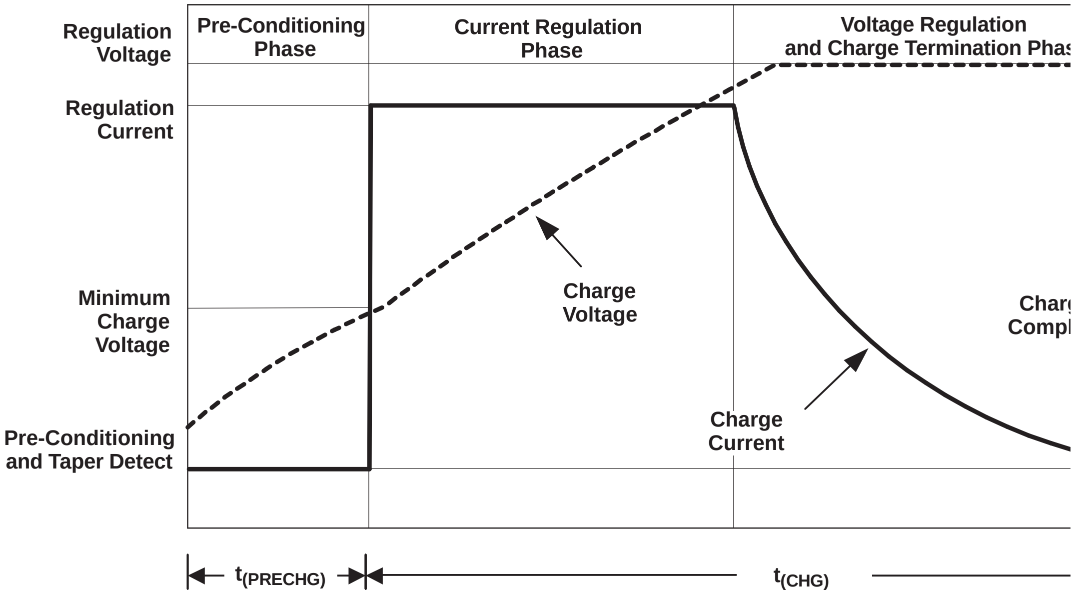


Figure 2. Typical Charging Profile

FUNCTIONAL DESCRIPTION

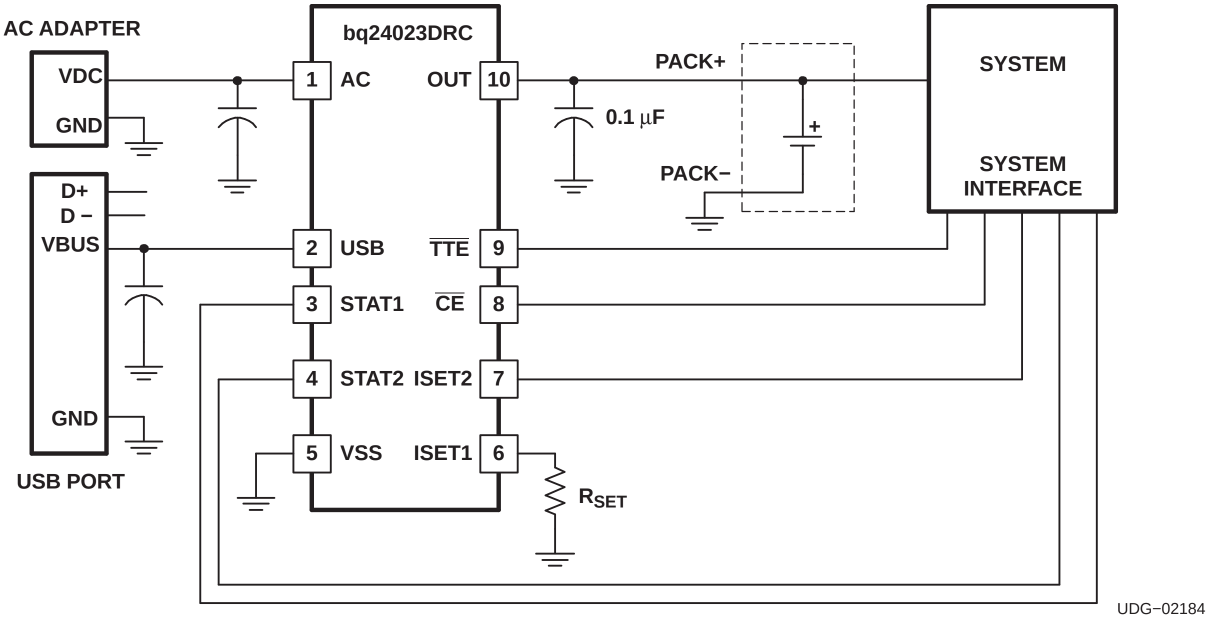
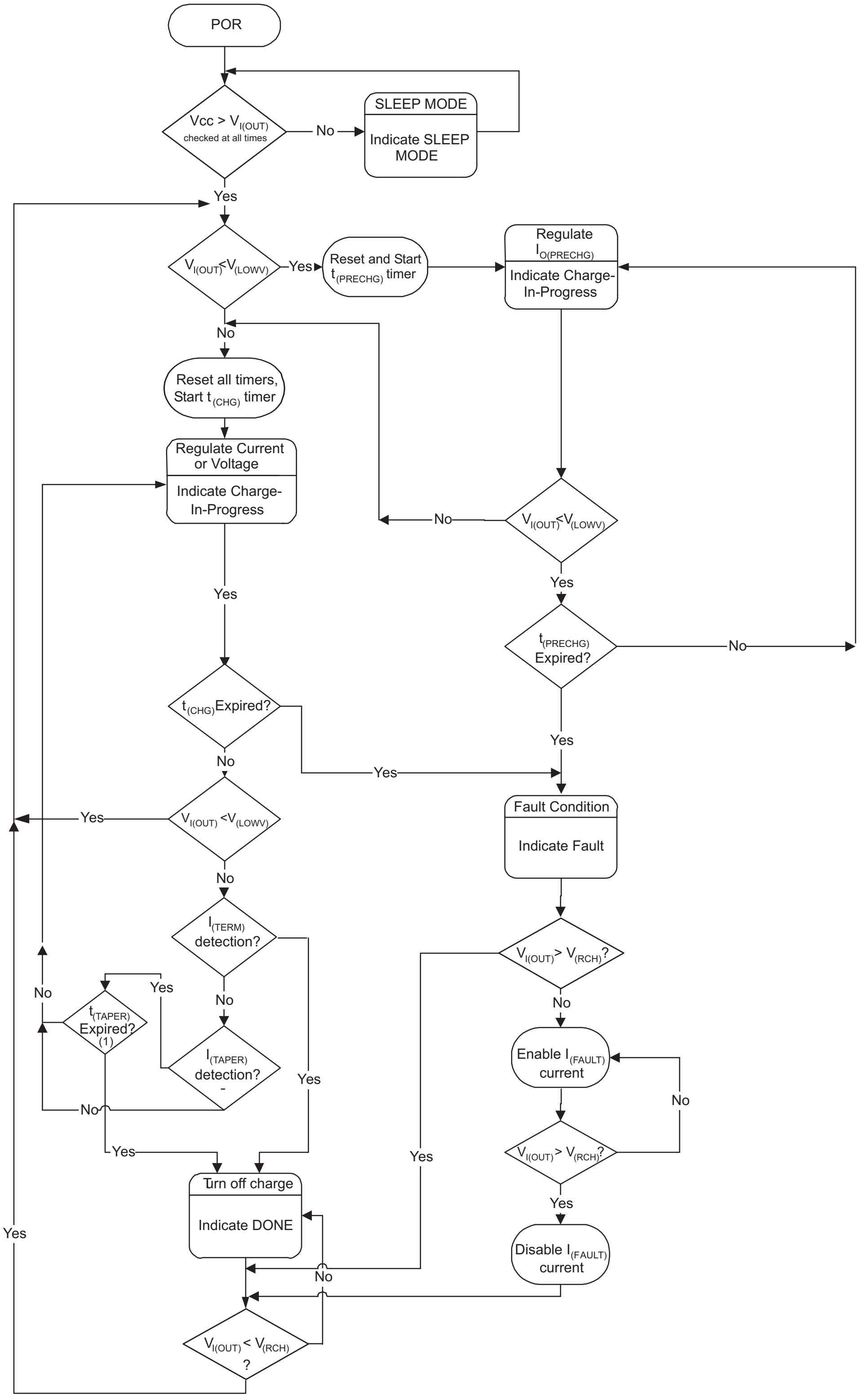


Figure 3. Typical Application Circuit

FUNCTIONAL DESCRIPTION (continued)



[1] t(TAPER) does not apply to bq24026/7

FUNCTIONAL DESCRIPTION (continued)

Figure 4. Operational Flow Chart

AUTONOMOUS POWER SOURCE SELECTION

As default, the bqTINY-II attempts to charge from the AC input. If AC input is not present, the USB is selected. If both inputs are available, the AC adapter has the priority. See for details.

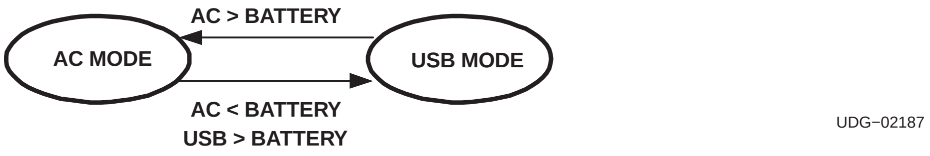


Figure 5. Typical Charging Profile

TEMPERATURE QUALIFICATION (bq24020, bq24024, bq24025, and bq24026 only)

The bqTINY-II continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. An internal current source provides the bias for common 10-kΩ negative-temperature coefficient thermistors (NTC) (see Figure 6). The device compares the voltage on the TS pin with the internal $V_{(LTF)}$ and $V_{(HTF)}$ thresholds to determine if charging is allowed. If a temperature outside the $V_{(LTF)}$ and $V_{(HTF)}$ thresholds is detected, the device immediately suspends the charge by turning off the power FET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns within the normal range.

The allowed temperature range for a 103AT-type thermistor is 0°C to 45°C. However the user may modify these thresholds by adding two external resistors. See Figure 7.

BATTERY PRE-CONDITIONING

If the battery voltage falls below the $V_{(LOWV)}$ threshold during a charge cycle, the bqTINY-II applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET1 and V_{SS}, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{O\ (PRECHG)} \quad \frac{V_{(PRECGH)} \quad K_{(SET)}}{R_{SET}} \tag{1}$$

The bqTINY-II activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY-II turns off the charger and asserts a FAULT code on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.

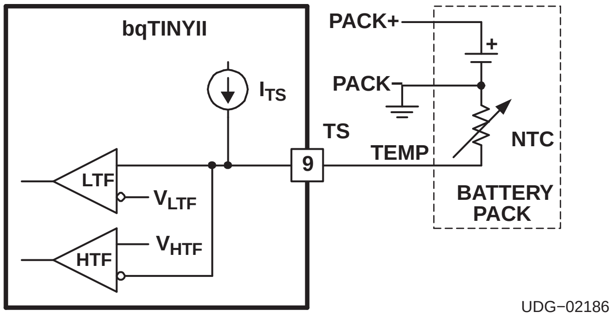


Figure 6. Temperature Sensing Configuration

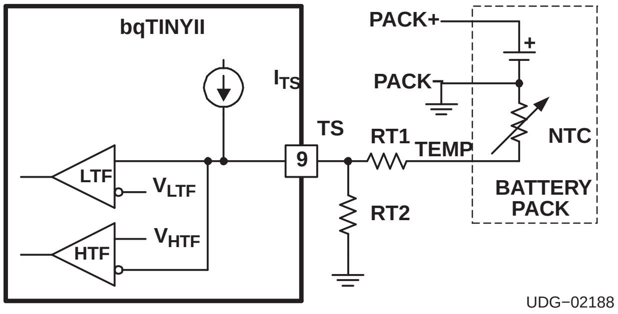


Figure 7. Temperature Sensing Thresholds

FUNCTIONAL DESCRIPTION (continued)

BATTERY CHARGE CURRENT

The bqTINY-II offers on-chip current regulation with a programmable set point. The resistor connected between the ISET1 and V_{SS}, R_{SET}, determines the AC charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{SET}} \tag{2}$$

When charging from a USB port, the host controller has the option of selecting either a 100-mA or a 500-mA charge rate using the ISET2 pin. A low-level signal sets the current at 100 mA, and a high-level signal sets the current at 500 mA. A high-Z input disables USB charging

BATTERY VOLTAGE REGULATION

The voltage regulation feedback is through the OUT pin. This input is tied directly to the positive side of the battery pack. The bqTINY-II monitors the battery-pack voltage between the OUT and VSS pins. When the battery voltage rises to the $V_{O(REG)}$ threshold, the voltage-regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY-II also monitors the charge time. If the charge is not terminated within the time period specified by $t_{(CHG)}$, the bqTINY-II turns off the charger and asserts a FAULT code on the STATx pins. Please refer to the *TIMER FAULT RECOVERY* section for additional details.

CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY-II monitors the charging current during the voltage-regulation phase. When the taper threshold, $I_{(TAPER)}$, is detected, the bqTINY-II initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET1 and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \tag{3}$$

The bqTINY-II resets the taper timer if the charge current rises above the taper threshold, $I_{(TAPER)}$.

In addition to taper-current detection, the bqTINY-II terminates charge if the charge current falls below the $I_{(TERM)}$ threshold. This feature allows quick recognition of a battery-removal condition, or insertion of a fully charged battery. Note that the charge timer and taper timer are bypassed for this feature. The resistor connected between the ISET1 and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table. Note that this applies to both AC and USB charging.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \tag{4}$$

After charge termination, the bqTINY-II re-starts the charge when the voltage on the OUT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

Note ON bq24026 AND bq24027

The bq24026 and bq24027 monitor the charging current during the voltage-regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected, the bq24026/27 terminates the charge. There is no taper timer ($t_{(TAPER)}$) for this version.

The resistor connected between the ISET1 and V_{SS}, R_{SET}, determines the taper-detect level for AC input. For USB charge, taper level is fixed at 10% of the 100- or 500-mA charge rate.

Also note that there is $I_{(TERM)}$ detection in the bq24026 and the bq24027.

SLEEP MODE

The bqTINY-II enters low-power sleep mode if both AC and USB are removed from the circuit. This feature prevents draining the battery in the absence of input supply.

FUNCTIONAL DESCRIPTION (continued)

CHARGE STATUS OUTPUTS

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-drain transistor is turned off.

Table 1. Status Pins Summary[1]

CHARGE STATE	STAT1	STAT2
Precharge in progress	ON	ON
Fast charge in progress	ON	OFF
Charge done	OFF	ON
Charge suspend (temperature)	OFF	OFF
Timer fault	OFF	OFF
Sleep mode	OFF	OFF

(1) OFF means the open-drain output transistor on the STAT1 and STAT2 pins is in an off state.

$\overline{\text{PG}}$ OUTPUT

The open-drain $\overline{\text{PG}}$ (power Good) indicates when the AC adapter is present. The output turns ON when a valid voltage is detected. This output is turned off in the sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or to communicate to the host processor.

$\overline{\text{CE}}$ INPUT (CHARGE ENABLE)

The $\overline{\text{CE}}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge. A high-level signal disables the charge, and places the device in a low-power mode. A high-to-low transition on this pin also resets all timers and timer fault conditions. Note that this applies to both AC and USB charging.

$\overline{\text{TTE}}$ INPUT (TIMER AND TERMINATION ENABLE)

The $\overline{\text{TTE}}$ digital input is used to disable or enable the fast-charge timer and charge-taper detection. A low-level signal on this pin enables the fast-charge timer and taper timer, and a high-level signal disables this feature. Note that this applies to both AC and USB charging.

THERMAL SHUTDOWN AND PROTECTION

The bqTINY-II monitors the junction temperature, T_J, and suspends charging if T_J exceeds $T_{(SHTDWN)}$. Charging resumes when T_J falls approximately 15°C below $T_{(SHTDWN)}$.

$\overline{\text{TE}}$ INPUT (TIMER ENABLED)

The $\overline{\text{TE}}$ digital input is used to disable or enable the fast-charge timer. A low-level signal on this pin enables the fast-charge timer and a high-level signal disables this feature.

Note that this applies to both AC and USB charging.

TIMER FAULT RECOVERY

As shown in Figure 4, the bqTINY-II provides a recovery method to deal with timer-fault conditions. The following discussion summarizes this method:

Condition #1: The charge voltage is above the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: bqTINY-II waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. When the battery voltage falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. Toggling POR, $\overline{CE}$, or $\overline{TTE}$ also clears the fault.

Condition #2: The charge voltage is below the recharge threshold ($V_{(RCH)}$), and a timeout fault occurs

Recovery method: In this scenario, the bqTINY-II applies the $I_{(FAULT)}$ current. This small current is used to detect a battery-removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY-II disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. When the battery voltage falls below the recharge threshold, the bqTINY-II clears the fault and starts a new charge cycle. Toggling POR, $\overline{CE}$, or $\overline{TTE}$ also clears the fault.

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

The bqTINY-II is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment Application Note* (TI Literature Number SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{5}$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow_lus549
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

$$P = \left(V_{IN} - V_{I(BAT)}\right) \times I_{O(OUT)} \tag{6}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See Figure 2.

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

APPLICATION INFORMATION (continued)

- To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the output filter capacitors from OUT to VSS should be placed as close as possible to the bqTINY, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small-signal ground path and the power-ground path.
- The BAT pin is the voltage feedback to the device. It should be connected with its trace as close to the battery pack as possible.
- The high-current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY-II is packaged in a thermally-enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24020DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24020DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24022DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24022DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24023DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24023DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24024DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24024DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24025DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24025DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24026DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24026DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24027DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24027DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24027DRCT	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24027DRCTG4	ACTIVE	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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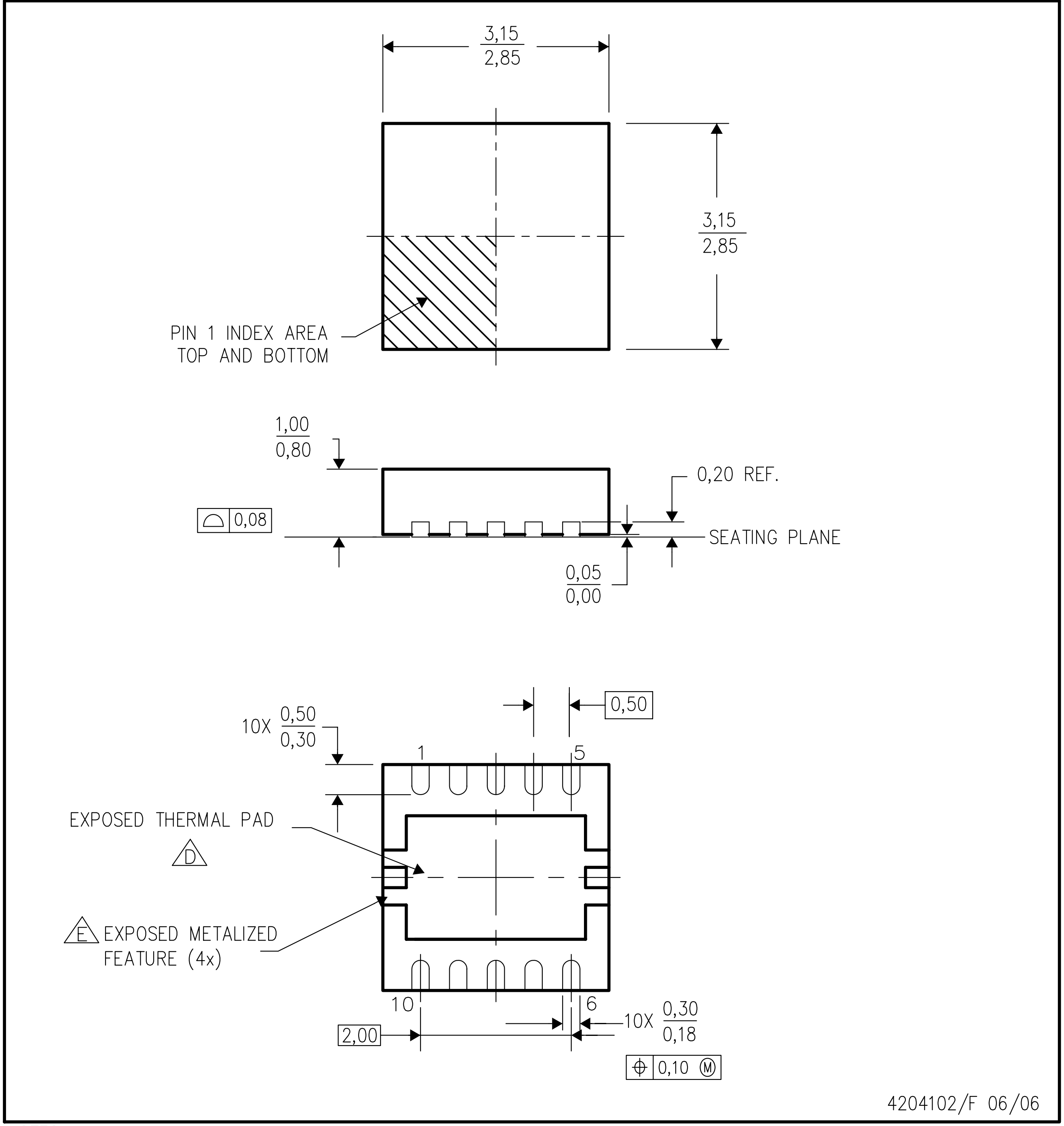
DRC (S-PDSO-N10) PLASTIC SMALL OUTLINE



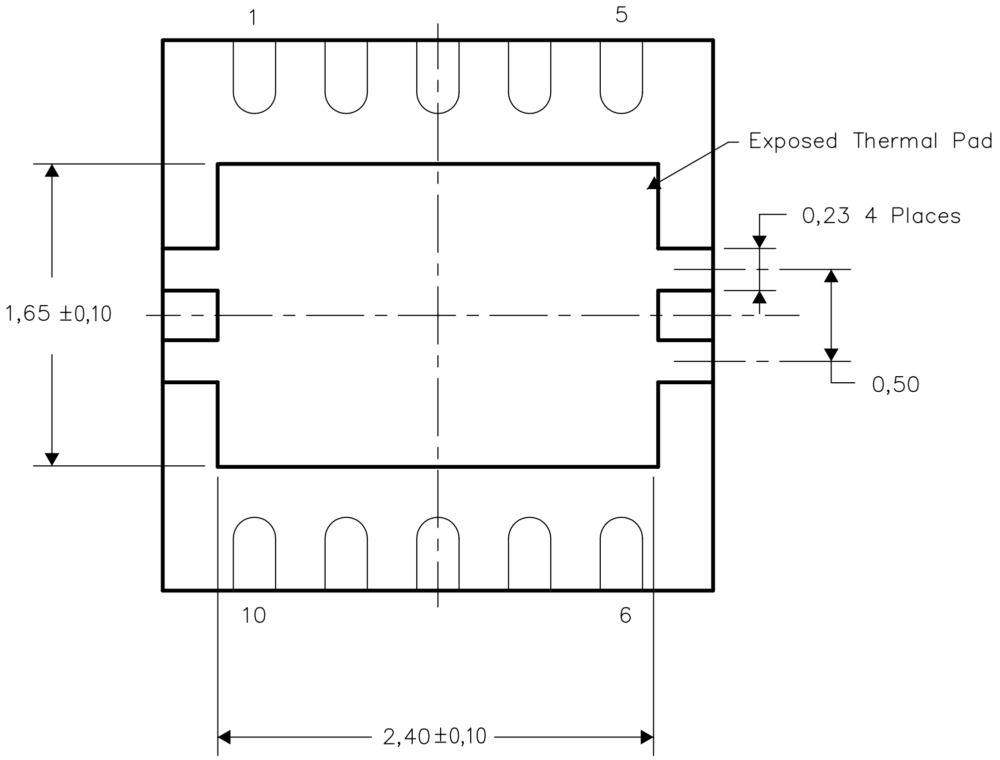
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

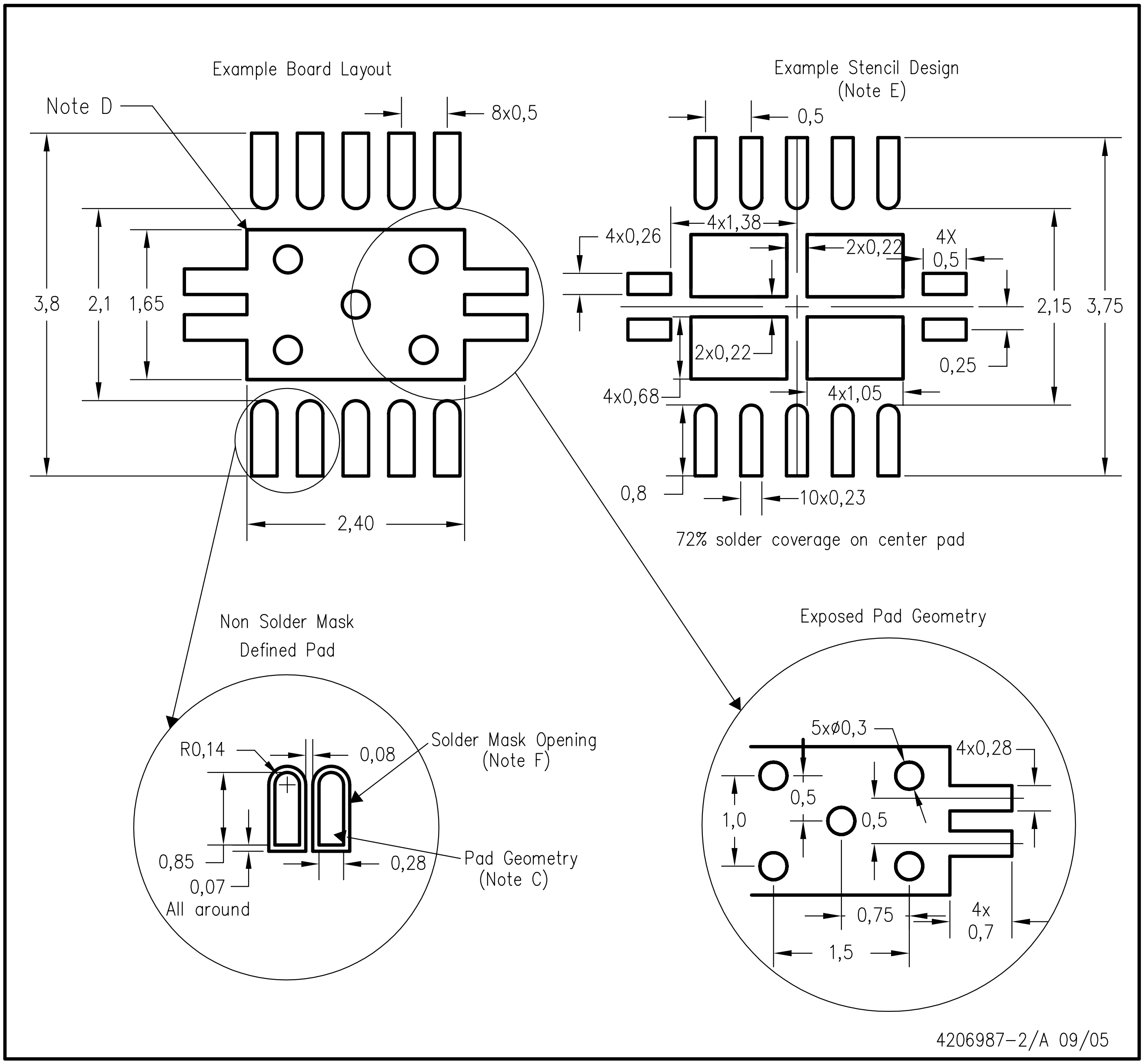


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRC (S-PDSO-N10)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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