

**MOTOROLA**

Dual Binary to 4 Decoder (Low)

ELECTRICALLY TESTED PER:
5962-8756801

The 10H571 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\bar{E}_0$ or $\bar{E}_1$ high, the corresponding selected 4 outputs are high. The common enable $\bar{E}$, when high, forces all outputs high.

- Propagation Delay, 2.0 ns Typical
- 460 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

FUNCTION	PIN ASSIGNMENTS			BURN-IN (CONDITION C)
	DIL	FLATS	LCC	
V_{CC1}	1	5	2	GND
$\bar{E}_1$	2	6	3	GND
Q_{13}	3	7	4	51 Ω to V_{TT}
Q_{12}	4	8	5	51 Ω to V_{TT}
Q_{11}	5	9	7	51 Ω to V_{TT}
Q_{10}	6	10	8	51 Ω to V_{TT}
B	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A	9	13	12	OPEN
Q_{03}	10	14	13	51 Ω to V_{TT}
Q_{02}	11	15	14	51 Ω to V_{TT}
Q_{01}	12	16	15	51 Ω to V_{TT}
Q_{00}	13	1	17	51 Ω to V_{TT}
$\bar{E}_0$	14	2	18	GND
$\bar{E}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

$V_{TT} = -2.0 \text{ V MAX} / -2.2 \text{ V MIN}$

$V_{EE} = -5.7 \text{ V MAX} / -5.2 \text{ V MIN}$

Military 10H571

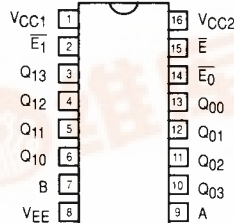


AVAILABLE AS

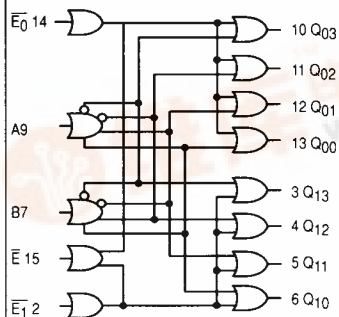
- 1) JAN: N/A
 - 2) SMD: 5962-8756801
 - 3) 883: 10H571/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



POSITIVE LOGIC DIAGRAM



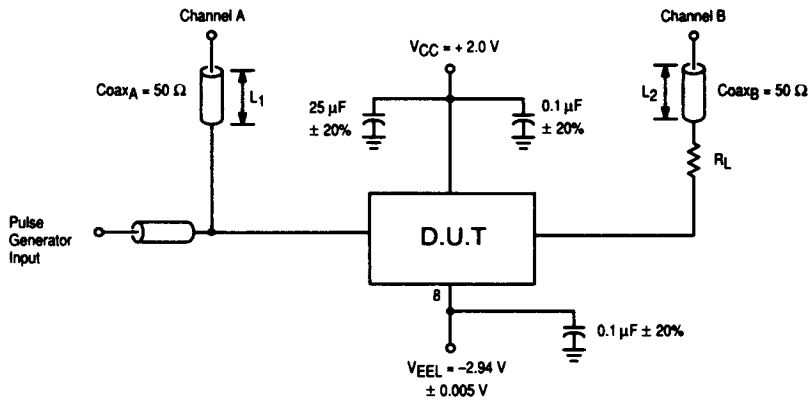
10H571

TRUTH TABLE

查询10H571/BEAJC"供应商

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{S}$	$\overline{E}$	A	B	Q ₁₀	Q ₁₁	Q ₁₂	Q ₁₃	Q ₀₀	Q ₀₁	Q ₀₂	Q ₀₃
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	L	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	L	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	$\emptyset$	$\emptyset$	$\emptyset$	$\emptyset$	H	H	H	H	H	H	H	H

$\emptyset$ = Don't Care

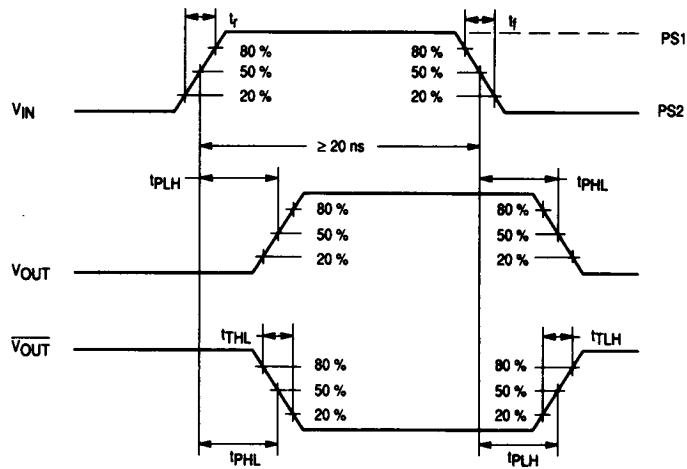


NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. $R_L = 50 \Omega$.

Figure 1. Switching Test Circuit

[查询"10H571/BEAJC"供应商](#)



NOTES

1. $V_{IN} = 20$ ns.
2. $f_{IN} = 1.0$ MHz.
3. $t_r = t_f = 1.0$ ns $\pm$ 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H571 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	V _{EE1}	V _{EE2}
T _A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-4.94	-5.46
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-4.94	-5.46
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-4.94	-5.46

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignment and VCC = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
	Functional Parameters:	Min	Max	Min	Max	Min	Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{EE2}	V _{EE1}	V _{CC}	P.U.T.		
V _{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	15						8	1, 16	3 - 6, 10 - 13	
V _{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9						8	1, 16	3 - 6, 10 - 13	
V _{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9		2, 7, 9 15	7, 9	8	8	1, 16	3 - 6, 10 - 13		
V _{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9		7, 9	2, 7, 9 15	8	8	1, 16	3 - 6, 10 - 13		
I _{EE}	Power Supply Current	-77		-85		-85		mA						8	1, 16	8		
I _{IH}	Input Current High		275		465		465	μA	2, 7, 9 14, 15					8	1, 16	2 - 7, 9, 15		
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		2, 7, 9 14, 15				8	1, 16	2 - 7, 9, 15		

10H571 QUIESCENT LIMIT TABLE *

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Test Temperature	Test Voltage Values (Volts)									
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	P _{S1}	P _{S2}	VEE1	VEE2	VEEL	VEEL
T _A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-4.94	-8.94	-5.46	-5.46
T _A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-4.94	-12.94	-5.46	-5.46
T _A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-4.94	-13.94	-5.46	-5.46

Symbol	Parameter	Limits							Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		- 55 °C				Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11											
t _{TLH}	Rise Time	0.5	2.0	0.6	2.2	0.4	2.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13			
t _{FHL}	Fall Time	0.5	2.0	0.6	2.2	0.4	2.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13			
t _{pLH}	Propagation Delay	0.5	3.0	0.5	3.2	0.5	3.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13			
t _{pHL}	Propagation Delay	0.5	3.0	0.5	3.2	0.5	3.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13			