REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-10-14

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL-LINEAR , CMOS, 12 BIT ANALOG TO DIGITAL CONVERTERS WITH SERIAL CONTROL AND 11 ANALOG INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96886

SHEET 1 OF 19

DESC FORM 193
JUL 94

9004708 0028110 466

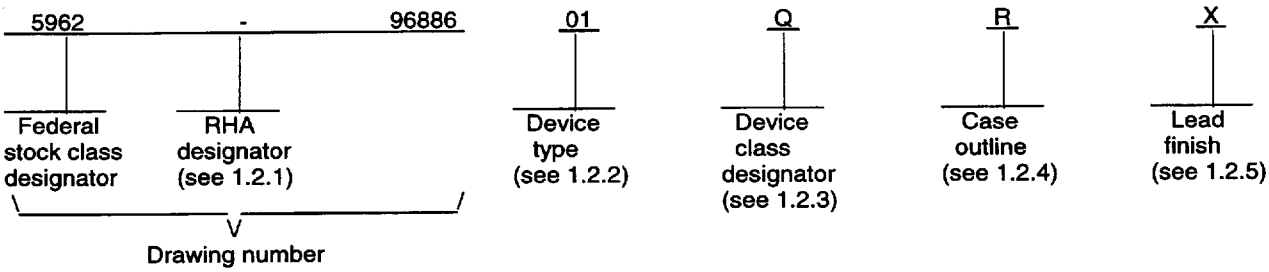
5962-E053-97

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC2543	12 Bit Analog to Digital Converters with Serial Control and 11 Analog Inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat package
2	CQCC1-N20	20	Leadless chip carrier package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range, (V_{CC})	-0.5 V dc to +6.5 V dc 2/
Input voltage range (V_{IN})(any input)	-0.3 V dc to V_{CC} +0.3 V dc
Output voltage (V_{OUT})	-0.3 V dc to V_{CC} +0.3 V dc
Positive reference voltage, V_{ref+}	V_{CC} +0.1 V d
Negative reference voltage, V_{ref-}	-0.1 V dc
Peak input current (any input)	±20 mA
Peak total input current (all inputs)	±30 mA
Storage temperature range (T_{STG})	-65 °C to +150°C
Lead remperature 1,6 mm (1/16 inch) from case for 10 seconds	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Positive reference voltage, (V_{ref+})	V_{CC} 3/
Negative reference voltage, (V_{ref-})	0.0 V 3/
Differential reference voltage, $V_{ref+} - V_{ref-}$	+2.5 V dc to V_{CC} +0.1 V dc 3/
Analog input voltage	0.0 V to V_{CC} 3/
High-level control input voltage, V_{IH} (V_{CC} =3.0 V to 3.6 V	2.0 V dc
Low-level control input voltage, V_{IL} (V_{CC} = 3.0 V to 3.6 V)	0.8 V dc
Clock frequency at I/O CLOCK	0.0 MHz to 4.1 MHz
Setup time, Address bits at data input before I/O CLOCK↑, $t_{su(A)}$	100 ns
Hold time, address bits after I/O CLOCK↑, $t_{h(A)}$	0.0 ns (MIN)
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_{h(CS)}$	0.0 ns (MIN)
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su\ (cs)}$	1.425 μs 4/
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$	120 ns (MIN)
Pulse duration I/O CLOCK Low, $t_{wL(I/O)}$	120 ns (MIN)
Transition time, I/O CLOCK, $t_{t(I/O)}$	1 μs (MAX)
Transition time, DATA INPUT and $\overline{CS}$, $t_{t(CS)}$	10 μs (MAX)
Operating free-air temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stress above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to digital ground with REF- and GND wired together (unless otherwise noted).
3/ Anaolg input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000). The device is functional with reference voltages down to $V(V_{ref+} - V_{ref-})$; However, the electrical specifications are no longer applicable.
4/ To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for a setup time plus two falling edges of the internal System clock after $\overline{CS}$↓ befor responding to control input signals. No attempt should be made to clock in an address until theminimum $\overline{CS}$ setup time has elapsed.
5/ This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max to V_{IH} min. In the vicinity of normal room temperatur, the devices function with input clock transition time as slow as 1 μs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835- Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780- Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagramshall be as specified on figure3 .

3.2.5 Load circuit. The load circuit shall be as speified on figure 4.

3.2.6 Timing waveforms. The timing waveforms shall be as spified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		V_{CC}	Group A subgroups	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	I_{OH} = -1.6 mA		4.5 V	1, 2, 3	2.4		V
		I_{OH} = -20 µA		4.5 V to 5.5 V		V_{CC} -0.1		
Low-level output voltage	V_{OL}	I_{OL} = 1.6 mA		4.5 V	1, 2, 3		0.4	V
		I_{OL} = 20 µA		4.5 V to 5.5 V			0.1	
Off-state (high-impedance state) output current	I_{OZH}	$V_{OUT} = V_{CC}$	$\overline{CS}$ at V_{CC}	4.5 V to 5.5 V	1, 2, 3		2.5	µA
	I_{OZL}	V_{OUT} = 0	$\overline{CS}$ at V_{CC}	4.5 V to 5.5 V			-2.5	
Input current high	I_{IH}	$V_I = V_{CC}$		4.5 V to 5.5 V	1, 2, 3		10.0	µA
Input current low	I_{IL}	V_I = 0		4.5 V to 5.5 V	1, 2, 3		-10.0	
Operating supply current	I_{CC}	$\overline{CS}$ at 0 V		4.5 V to 5.5 V	1, 2, 3		10.0	mA
Power-down current	$I_{cc(PD)}$	For all digital inputs, $0 \le V_I \le 0.5$ V or $V_I \ge V_{CC}$ -0.5 V			1, 2, 3		25	µA
Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V		4.5 V to 5.5 V	1, 2, 3		10	µA
		Selected channel at 0 V, Unselected channel at V_{CC}		4.5 V to 5.5 V			-10	
Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$, V_{ref-} = GND		4.5 V to 5.5 V	1, 2, 3		10.0	µA
Input capacitance	C_I	Analog inputs See 4.4.1.c		4.5 V to 5.5 V	4		60	pF
		Control inputs See 4.4.1.c					15	
Functional test		See 4.4.1.b			7, 8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
Linearity error 2/	E_L	See figure 5 3/	4.5 V to 5.5 V	4, 5, 6		± 1	LSB
Differential linearity error	E_D	See figure 5 3/				± 1	
Offset error 4/	E_O	See figure 5 3/				±1.5	
Gain error 4/	E_G	See figure 5 3/				± 1	
Total adjusted error 5/	E_T			4, 5, 6		±1.75	
Conversion time	t_{conv}	See figure 5	4.5 V to 5.5 V	9, 10, 11		10	µs
Total cycle time(access, sample, and conversion)	t_c	See figure 5 6/	4.5 V to 5.5 V	9, 10, 11		10 + total I/O CLOCK periods + $t_{d(I/O-EOC)}$	
Channel acquisition time (sample)	t_{acq}	See figure 5 6/	4.5 V to 5.5 V	9, 10, 11	4	12	I/O CLOCK periods
Valid time, DATA OUT remains valid after I/OCLOCK↓	t_v	See figure 5	4.5 V to 5.5 V	9, 10, 11	10		ns
Delay time, I/O CLOCK↓ to DATAOUT valid	$t_{d(I/O-DATA}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		150	ns
Delay time, last I/O CLOCK↓ to EOC ↓	$t_{d(I/O-EOC)}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		2.2	
Delay time, EOC↑ to DATA OUT (MSB)	$t_{d(EOC-DATA}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		100	ns
Enable time, $\overline{CS}$ ↓ to DATA OUT(MSB/LSB driven)	t_{PZH}, t_{PZL}	See figure 5	4.5 V to 5.5 V	9, 10, 11		1.3	µs
Disable time, $\overline{CS}$ ↑ to DATA OUT (high impedance)	t_{PHZ}, t_{PLZ}	See figure 4	4.5 V to 5.5 V	9, 10, 11		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	V_{CC}	Group A subgroups	Limits		Unit
					Min	Max	
Rise time, EOC	$t_{r(EOC)}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		50	ns
Fall time, EOC	$t_{f(EOC)}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		50	ns
Rise time, data bus	$t_{r(bus)}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		50	ns
Fall time, data bus	$t_{f(bus)}$	See figure 5	4.5 V to 5.5 V	9, 10, 11		50	ns
Delay time, last I/O CLOCK ↓ to $\overline{CS}$ ↓ to abort conversion	$t_{d(I/O-CS)}$	7/	4.5 V to 5.5 V	9, 10, 11		5	μs

1/ All voltage values are with respect to GND with REF- and GND wired together (unless otherwise noted).

2/ Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristic.

3/ Analog input voltages greater than applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF- convert as all zeros (0000000000).

4/ Gain error is the difference between the actual midstep value and the nominal midstep value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. Offset error is the difference between the actual midstep value and the nominal midstep at the offset point.

5/ Total unadjusted error comprises linearity, zero-scale, and full-scale errors.

6/ I/O CLOCK period = 1/(I/O CLOCK frequency).

7/ Any transitions of $\overline{CS}$ are recognized as valid only if the levels is maintained for a setup time. $\overline{CS}$ must be taken low at ≤ 5 μs of the tenth I/O CLOCK falling edge to ensure a conversion is aborted. Between 5μs and 10 μs, the result is uncertain as to whether the conversion is aborted or the conversion results are valid.

Device type	01
Case outline	R, S, 2
Terminal number	Terminal symbol
1	AIN0
2	ANI1
3	ANI2
4	ANI3
5	ANI4
6	ANI5
7	ANI6
8	ANI7
9	ANI8
10	GND
11	ANI9
12	ANI10
13	REF-
14	REF+
15	$\overline{CS}$
16	DATA OUT
17	DATA INPUT
18	I/O CLOCK
19	EOC
20	V_{CC}

Pin description	
Terminal symbol	Description
AINn (n = 0 to 10	Analog signal inputs
REF-	Lower reference voltage
REF+	Upper reference voltage
$\overline{CS}$	Chip select
DATA OUT	Serial data input
DATA INPUT	Serial data input
I/O CLOCK	Input-Output clock
EOC	End of conversion

FIGURE 1. Terminal connections.

Analog-Channel-Select Address

Analog Input Selected 3/	Value Shifted Into Address	
	Binary	Hex
A0	0000	0
A1	0001	1
A2	0010	2
A3	0011	3
A4	0100	4
A5	0101	5
A6	0110	6
A7	0111	7
A8	1000	8
A9	1001	9
A10	1010	A

Test-Mode-Select Address

INTERNAL SELF-TEST VOLTAGE SELECTED 1/	VALUE SHIFTED INTO DATA INPUT		UNIPOLAR OUTPUT RESULT (HEX) 2/
	BINARY	HEX	
$\frac{V_{ref+} - V_{ref-}}{2}$	1011	B	200
V_{ref-}	1100	C	000
V_{ref+}	1101	D	3FF

1/ V_{ref+} is the voltage supplied to REF+, and V_{ref-} is the voltage applied to REF-.
2/ The output results shown are the ideal values and may vary with the reerence stability and with internal offsets.

Power-Down-Select Address

INPUT COMMAND	VALUE SHIFTED INTO DATA INPUT		RESULT
	BINARY	HEX	
Power down	1110	E	$I_{CC} \leq 25\ \mu A$

FIGURE 2. Truth table.

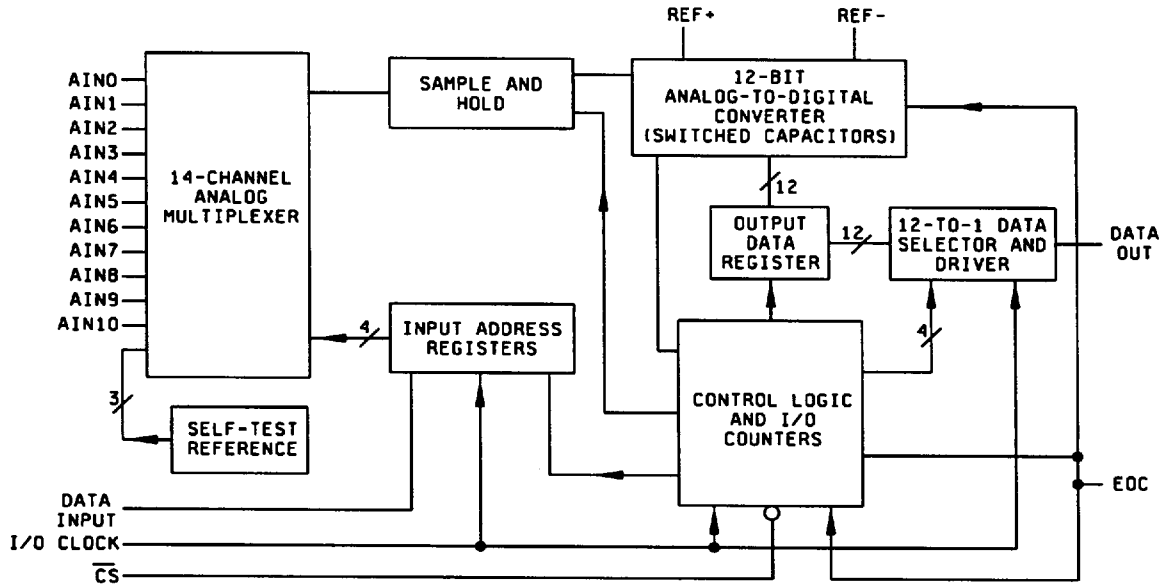
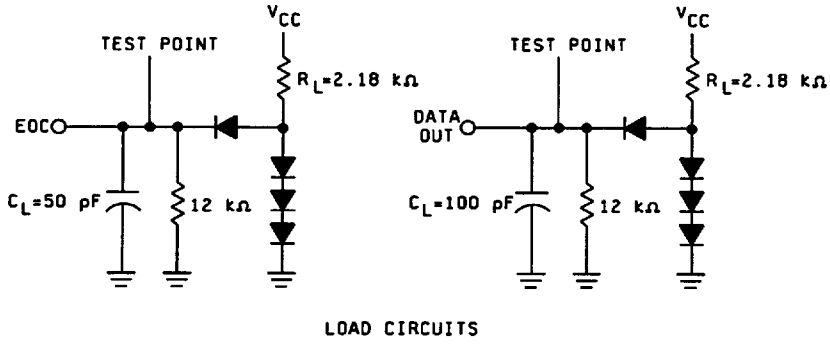
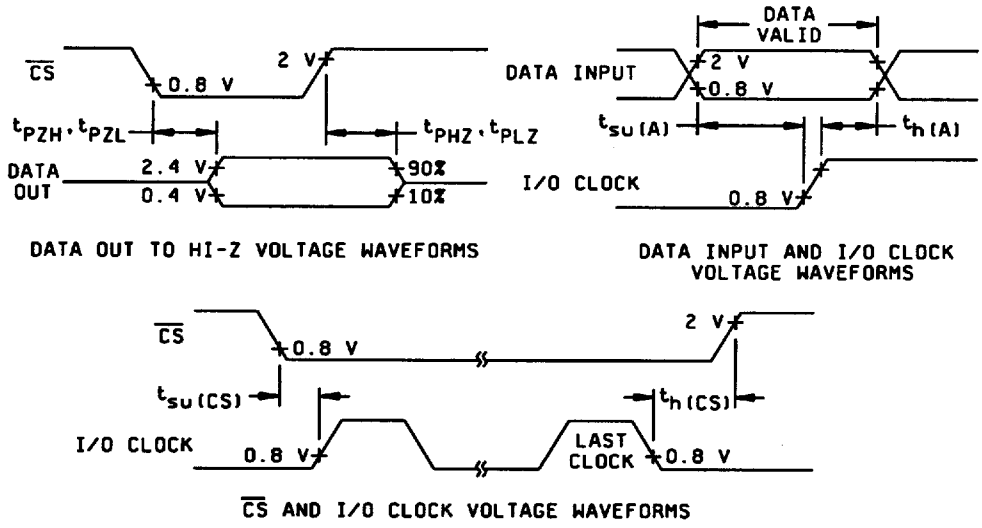


FIGURE 3. Block diagram.



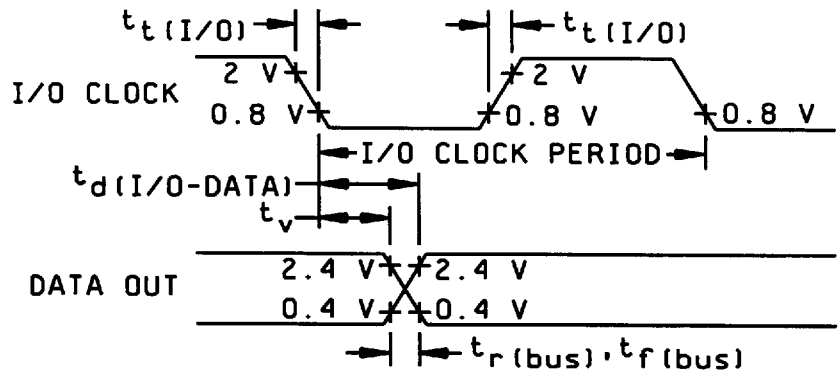
LOAD CIRCUITS

FIGURE 4. Load circuit.

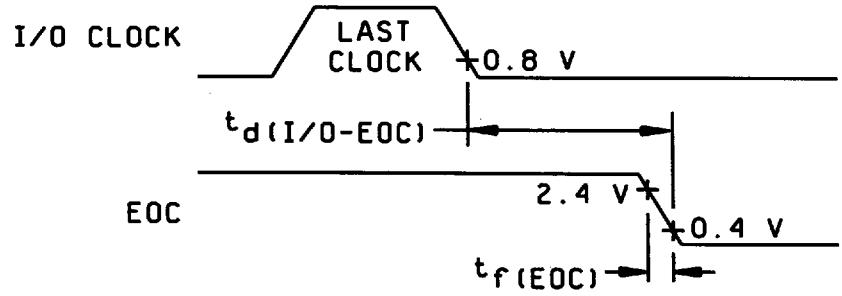


NOTE: To ensure full conversion accuracy, it is recommended that no input signal change occurs while a conversion is ongoing.

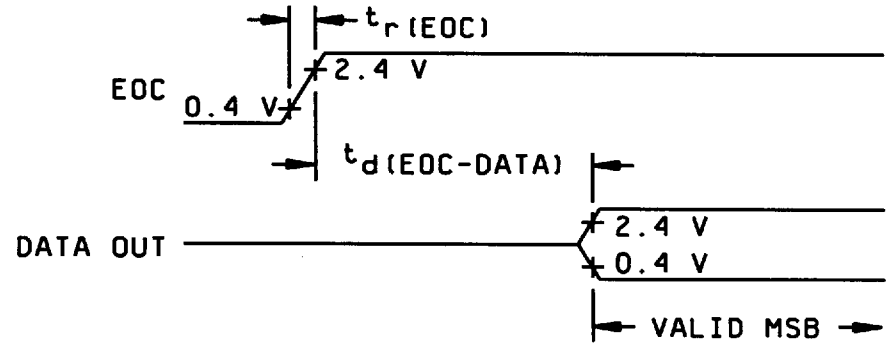
FIGURE 5. Timing waveforms.



I/O CLOCK AND DATA OUT VOLTAGE WAVEFORMS

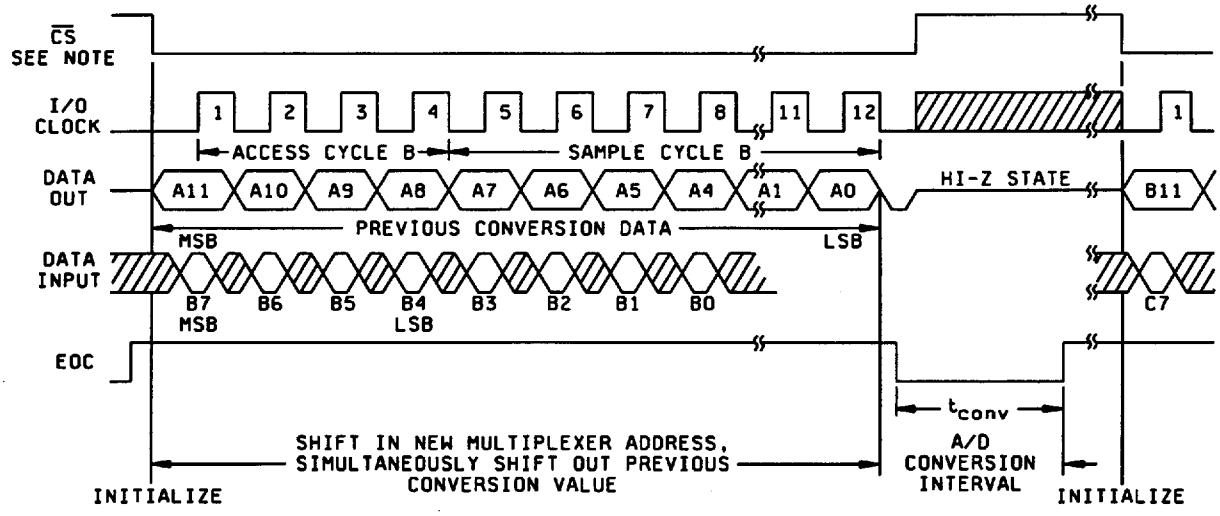


I/O CLOCK AND EOC VOLTAGE WAVEFORMS

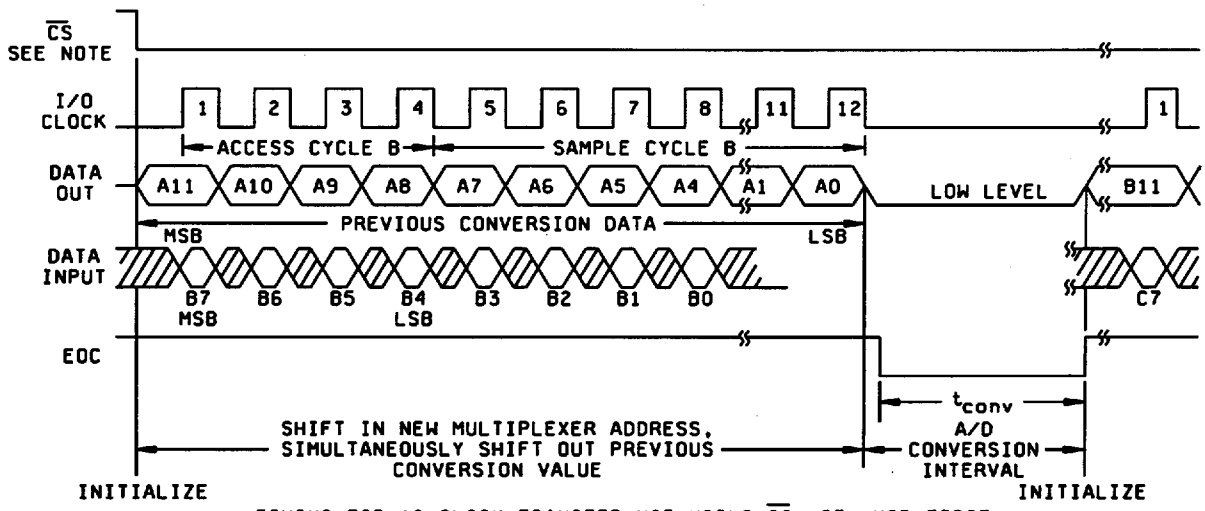


EOC AND DATA OUT VOLTAGE WAVEFORMS

FIGURE 5. Timing waveforms - continued.



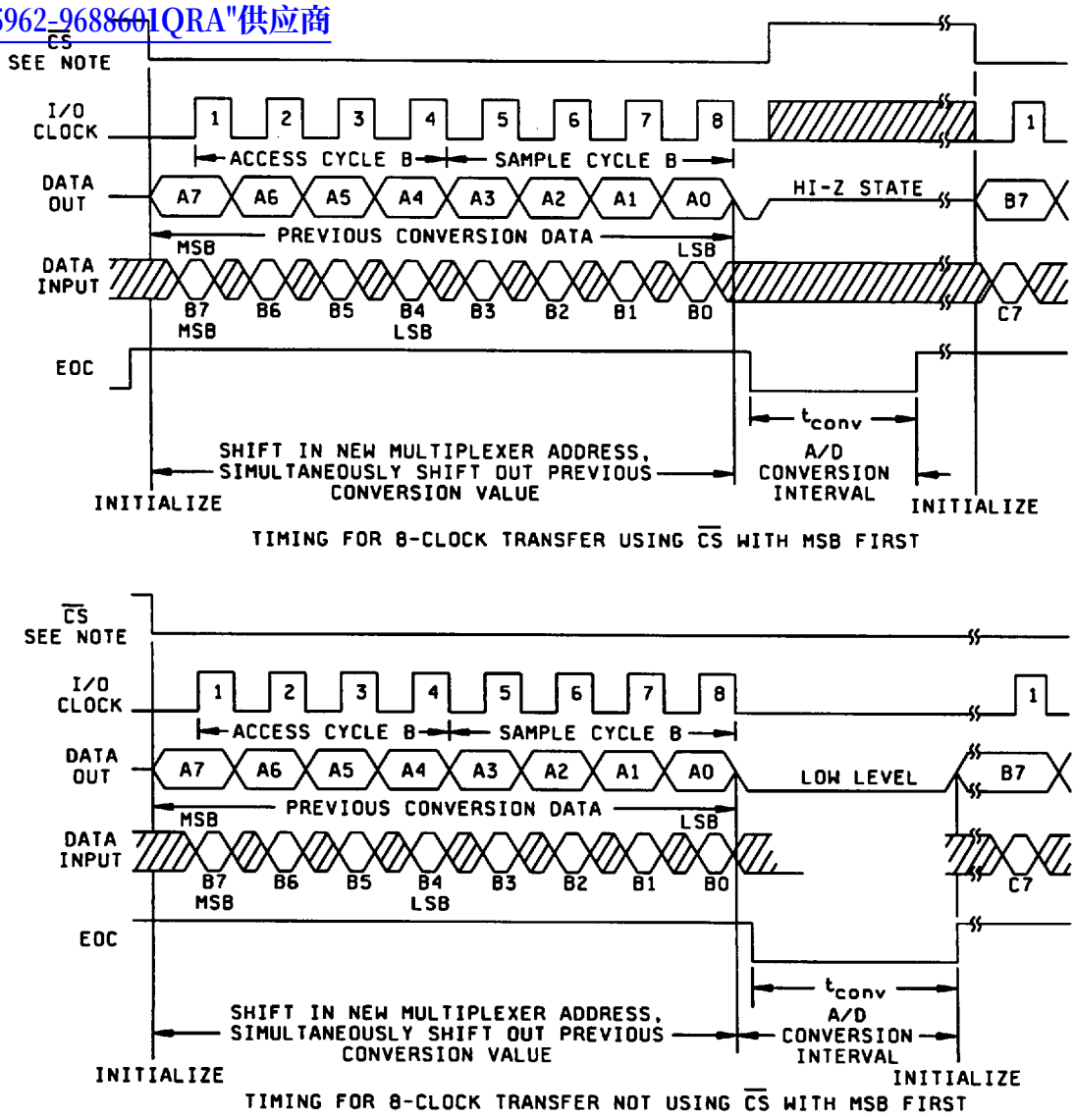
TIMING FOR 12-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



TIMING FOR 12-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuity waits for a setup time after $\overline{CS}$ ↓ before responding to control nput signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.

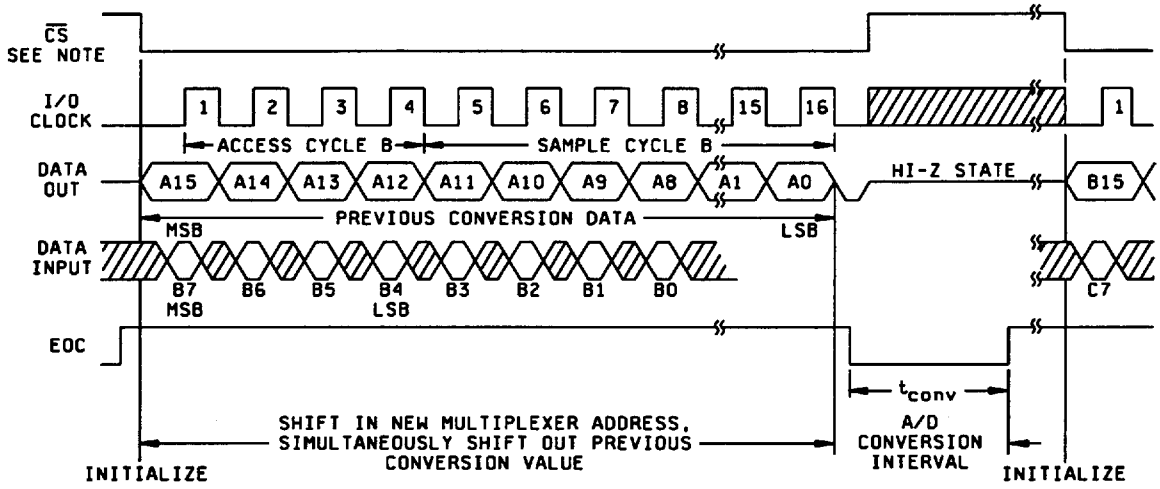


TIMING FOR 8-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST

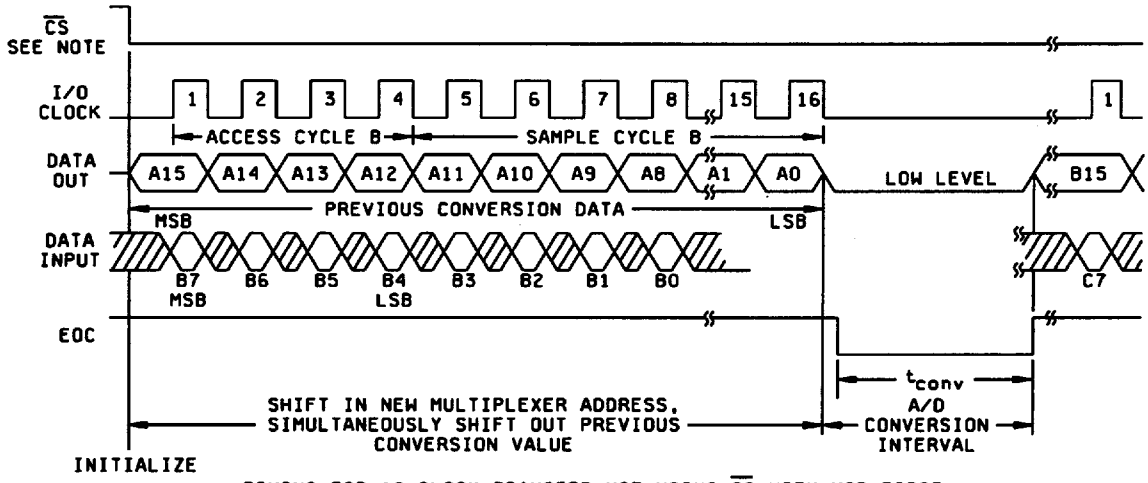
TIMING FOR 8-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuity waits for a setup time after $\overline{CS}\downarrow$ before responding to control nput signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.



TIMING FOR 16-CLOCK TRANSFER USING $\overline{CS}$ WITH MSB FIRST



TIMING FOR 16-CLOCK TRANSFER NOT USING $\overline{CS}$ WITH MSB FIRST

NOTE: To minimize errors caused by noise at $\overline{CS}$, the internal circuity waits for a setup time after $\overline{CS}$ is before responding to control nput signals. Therefore, no attempt should be made to clock in an address until the minimum $\overline{CS}$ setup time has elapsed.

FIGURE 5. Timing waveforms - continued.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	- - -
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1/ 1, 2, 3, 4, 5, 6, 7 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition B, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 96-10-14

Approved sources of supply for SMD 5962-96886 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9688601QRA	01295	TLC2543MJB
5962-9688601QSA	3/	TLC2543MWB
5962-9688601Q2A	3/	TLC2543MFKB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved supplier.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.