Isolated Profibus RS-485 Transceiver with Integrated Transformer Driver

Check for Samples: ISO1176T

FEATURES

- 4000V_{peak} Isolation, 560V_{peak} V_{IORM}
- Meets or Exceeds the Requirements of EN 50170 and TIA/EIA RS-485
- Signaling Rates up to 40 Mbps
- Differential Output exceeds 2.1V (54Ω Load)
- Low Bus Capacitance 10pF (MAX)
- 50kV/μs Typical Transient Immunity
- UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2) Approvals Pending
- Fail-safe Receiver for Bus Open, Short, or Idle

APPLICATIONS

- Profibus®
- Factory Automation
- Networked Sensors
- Motor/motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

DESCRIPTION

The ISO1176T is an isolated differential line transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is ideal for long transmission lines because the ground loop is broken to allow the device to operate with a much larger common-mode voltage range. The symmetrical isolation barrier of each device is tested to provide 2500Vrms of isolation between the line transceiver and the logic-level interface.

The galvanically isolated differential bus transceiver is an integrated circuit designed for bi-directional data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential input line receiver. The driver has an active-high enable with isolated enable-state output on the ISODE pin (pin 10) to facilitate direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC2} = 0.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. The ISO1176T can significantly reduce the risk of data corruption and damage to expensive control circuits.

The device is characterized for operation over the ambient temperature range of –40°C to 85°C.

PRODUCT PREVIEW

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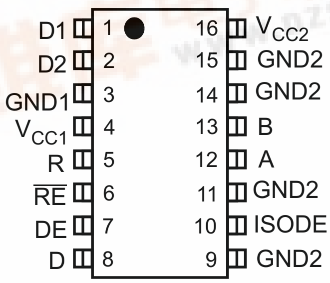

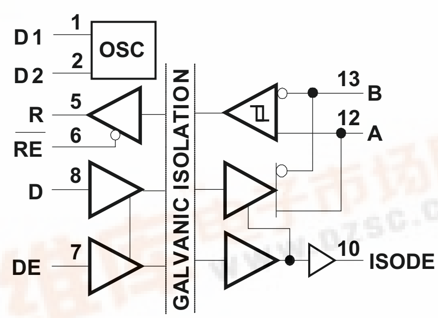

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC1}, V_{CC2}	Input supply voltage(2)				–0.5 to 7	V
V_O	Voltage at any bus I/O terminal				–9 to 14	V
	Voltage at D1, D2				14	V
V_I	Voltage input at D, DE or $\overline{RE}$ terminal				–0.5 to 7	V
I_O	Receiver output current				±10	mA
I_{D1}, I_{D2}	Transformer Driver Output Current				450	mA
ESD	Electrostatic Discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus pins to GND1	±6	kV
				Bus pins to GND2	±16	
				all pins	±4	
		Charged Device Model	JEDEC Standard 22, Test Method C101	all pins	±1	kV
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				170	°C
T_{STG}	Storage temperature				-65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Logic side supply voltage, V_{CC1} (with respect to GND1)		3		5.5	V
	Bus side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	
V_{CM}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	$\overline{RE}$	2		V_{CC1}	V
		D, DE	0.7 V_{CC1}			
V_{IL}	Low-level input voltage	$\overline{RE}$	0		0.8	V
		D, DE			0.3 V_{CC1}	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output Current	RS-485 driver	–70		70	mA
		Receiver	–8		8	
T_A	Ambient temperature		-40		85	°C
T_J	Operating junction temperature				150	°C
1 / t_{UI}	Signaling Rate				40	Mbps

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SUPPLY CURRENT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1} (1)	Logic-side quiescent supply current	V_{CC1} = 3.3 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		4.5	8	mA
		V_{CC1} = 5 V ± 10%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		7	11	mA
I_{CC2} (1)	Bus-side quiescent supply current	V_{CC2} = 5 V ± 5%, DE, $\overline{RE}$ = 0V or V_{CC1}, No load		13.5	18	mA

(1) I_{CC1} and I_{CC2} are measured when device is connected to external power supplies. D1 and D2 are disconnected from external transformer.

ISODE-PIN ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –8mA	V_{CC2} – 0.8	4.6		V
		I_{OH} = –20μA	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 8mA		0.2	0.4	V
		I_{OL} = 20μA		0	0.1	

RS-485 DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OD}	Open-circuit differential output voltage	$\|V_A – V_B\|$, See Figure 1		1.5		V_{CC2}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	See Figure 2 and Figure 6		2.1			V
		See Figure 3, Common-mode loading with Vtest from –7V to +12V		2.1			
$\|\Delta V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See Figure 4 and Figure 5, R_L = 54Ω		-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 4 and Figure 55, R_L = 54Ω		2		3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			–0.2		0.2	
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage				0.5		
$V_{OD(ring)}$	Differential output voltage over and under shoot	See Figure 6 and Figure 9				10%	$V_{OD(pp)}$
I_I	Input current	D, DE at 0V or V_{CC1}		–10		10	μA
$I_{O(OFF)}$	Power-off output current	V_{CC2} = 0 V		See receiver input current			
I_{OZ}	High-impedance output current	DE at 0V					
$I_{OS(P)}$	Peak short-circuit output current	See Figure 8 and Figure 19, DE at V_{CC1}	V_{OS} = –7V to 12V	-250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current		V_{OS} = 12V, D at GND1	60		135	
			V_{OS} = –7V, D at V_{CC1}	–135		–60	
C_{OD}	Differential output capacitance			See receiver C_{IN}			
CMTI	Common-mode transient immunity	See Figure 19		25			kV/μs

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RS-485 DRIVER SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Prop delay time	V_{CC1} = 5V ± 10%, V_{CC2} = 5V ± 5%	See Figure 9			35	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				2	5	
t_{PLH}, t_{PHL}	Prop delay time	V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 5%				40	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				2	5	
t_r	Differential output signal rise time			2	3	7.5	ns
t_f	Differential output signal fall time			2	3	7.5	
t_{pDE}	DE to ISODE prop delay		See Figure 13			30	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew		See Figure 10			1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$, $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay, high-impedance-to-active output		See Figure 11 and Figure 12, C_L = 50 pF, $\overline{RE}$ at 0 V			80	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$, $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay, active-to-high-impedance output					80	
$\| t_{p(AZL)} – t_{p(BZH)} \|$ $\| t_{p(AZH)} – t_{p(BZL)} \|$	Enable skew time				0.55	1.5	ns
$t_{(CFB)}$	Time from application of short-circuit to current fold back		See Figure 8		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown		See Figure 8, T_A = 25°C	100			µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage		See Figure 15	I_O = –8mA		–80	-10	mV
$V_{IT(–)}$	Negative-going input threshold voltage			I_O = 8mA	–200	–120		
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					25		
V_{OH}	High-level output voltage	V_{CC1} = 3.3V ± 10% and V_{CC2} = 5V ± 5%	V_{ID} = 200 mV, See Figure 15	I_{OH} = -8mA	V_{CC1} – 0.4	3		V
				I_{OH} = -20µA	V_{CC1} – 0.1	3.3		
V_{OL}	Low-level output voltage		V_{ID} = -200 mV, See Figure 15	I_{OL} = 8mA		0.2	0.4	V
				I_{OL} = 20µA		0	0.1	
V_{OH}	High-level output voltage	V_{CC1} = 5V ± 10% and V_{CC2} = 5V ± 5%	V_{ID} = 200 mV, See Figure 15	I_{OH} = –8mA	V_{CC1} – 0.8	4.6		V
				I_{OH} = –20µA	V_{CC1} – 0.1	5		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 15	I_{OL} = 8mA		0.2	0.4	V
				I_{OL} = 20µA		0	0.1	
I_A, I_B	Bus pin input current		V_I = –7 or 12V, Other input = 0 V	V_{CC2} = 4.75V or 5.25V	–160		200	µA
$I_{A(off)}$, $I_{B(off)}$				V_{CC2} = 0V				
I_I	Receiver enable input current		$\overline{RE}$ = 0 V		–50		50	µA
I_{OZ}	High-impedance state output current		$\overline{RE}$ = V_{CC1}		–1		1	µA
R_{ID}	Differential input resistance		A, B		60			kΩ
C_{ID}	Differential input capacitance		Test input signal is a 1 MHz sine wave with 1Vpp amplitude. CD is measured across A and B.			7	10	pF
CMR	Common mode rejection		See Figure 18			4		V

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	V_{CC1} = 5V ± 10%, V_{CC2} = 5V ± 5%	See Figure 15		50	65	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				2	5	
t_{PLH}, t_{PHL}	Propagation delay time	V_{CC1} = 3.3V ± 10%, V_{CC2} = 5V ± 5%			53	70	
$t_{sk(p)}$	Pulse skew (|tpHL - tpLH|)				2	5	
t_r	Output signal rise time				2	4	
t_f	Output signal fall time				2	4	
t_{PZH}	Propagation delay, high-impedance-to-high-level output		DE at V_{CC1}, See Figure 16		13	25	
t_{PHZ}	Propagation delay, high-level-to-high-impedance output				13	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output		DE at V_{CC1}, See Figure 17		13	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				13	25	

TRANSFORMER DRIVER CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	V_{CC1} = 5V ± 10%, D1 and D2 connected to Transforme	350	450	550	kHz
		V_{CC1} = 3.3V ± 10%, D1 and D2 connected to Transformer	300	400	500	
R_{ON}	Switch on resistance	D1 and D2 connected to 50-Ω pull-up resistors		1	2.5	Ω
R_{OFF}	Switch off resistance	D1 and D2 connected to 50-Ω pull-up resistors	1	5		kΩ
t_{r_D}	D1, D2 output rise time	V_{CC1} = 5V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	40	80	110	ns
		V_{CC1} = 3.3V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	30	70	110	
t_{f_D}	D1, D2 output fall time	V_{CC1} = 5V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	20	55	70	ns
		V_{CC1} = 3.3V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	40	80	140	
f_{St}	Startup frequency	V_{CC1} = 1.9 V, D1 and D2 connected to Transformer		230		kHz
t_{BBM}	Break before make time delay	V_{CC1} = 5V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	12	38	75	ns
		V_{CC1} = 3.3V ± 10%, See Figure 20, D1 and D2 connected to 50-Ω pull-up resistors	100	140	200	

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

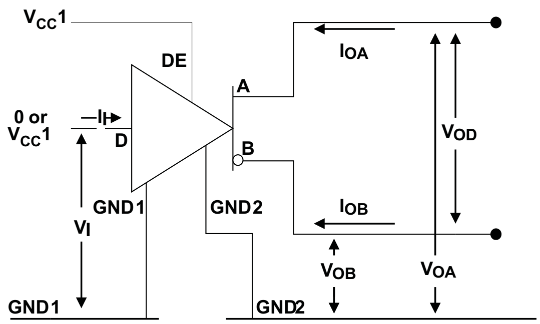

Figure 1. Open Circuit Voltage Test Circuit

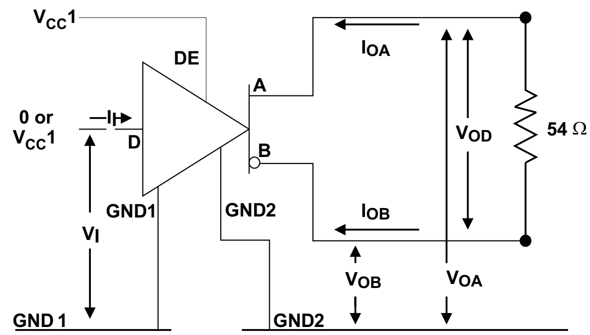

Figure 2. V_{OD} Test Circuit

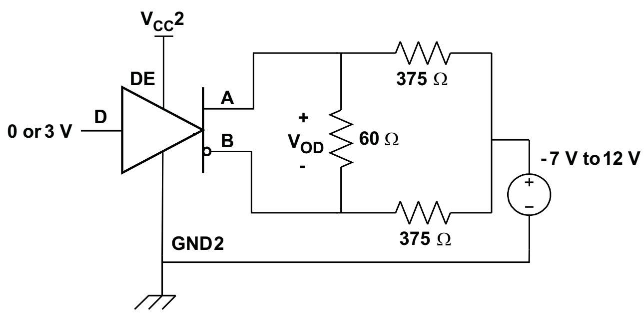

Figure 3. Driver V_{OD} with Common-mode Loading Test Circuit

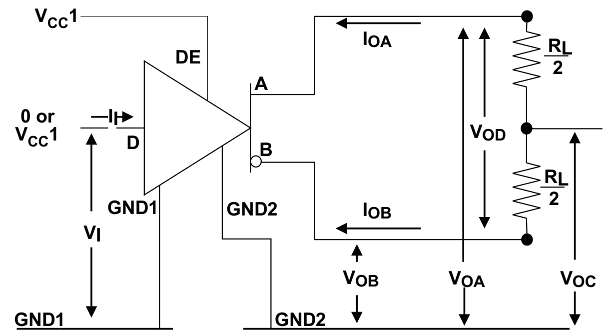

Figure 4. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit

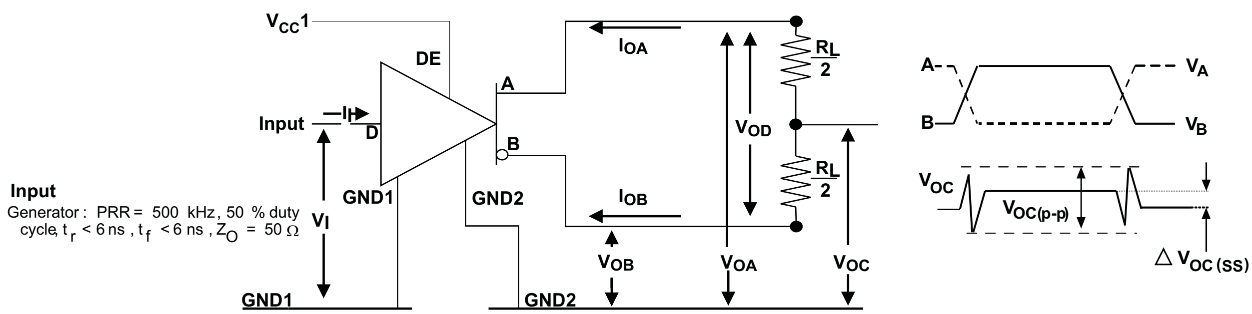

Figure 5. Steady-State Output Voltage Test Circuit and Voltage Waveforms

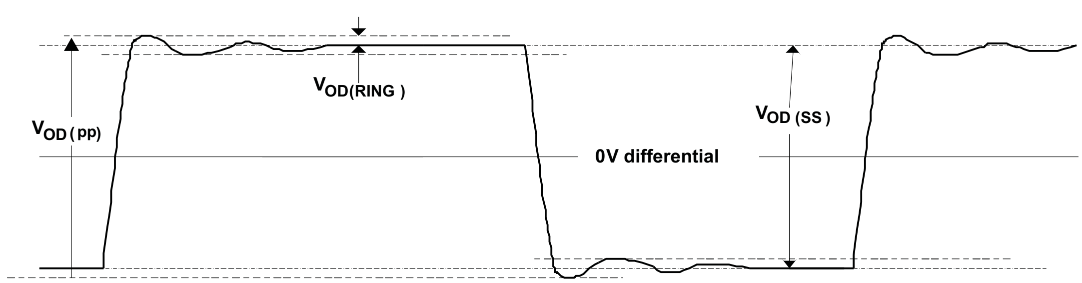

Figure 6. $V_{OD(RING)}$ Waveform and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

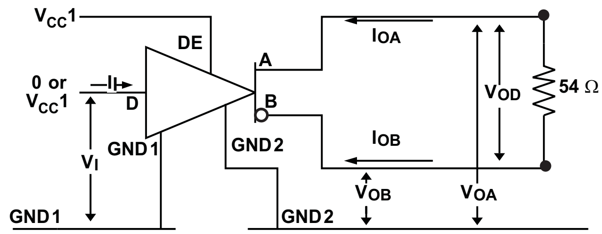

Figure 7. Input Voltage Hysteresis Test Circuit

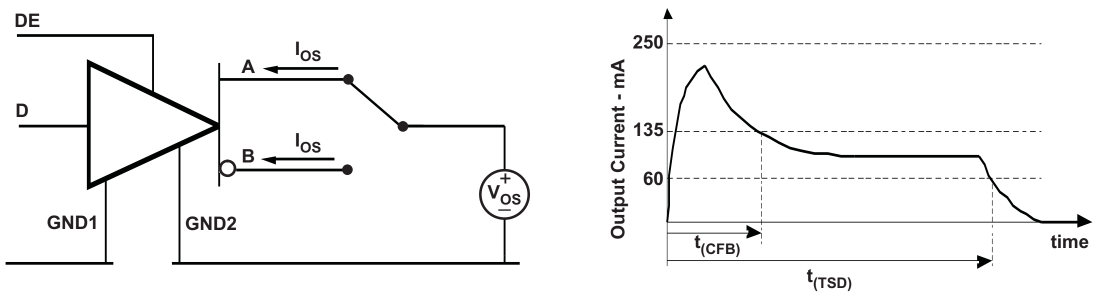

Figure 8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t=0)

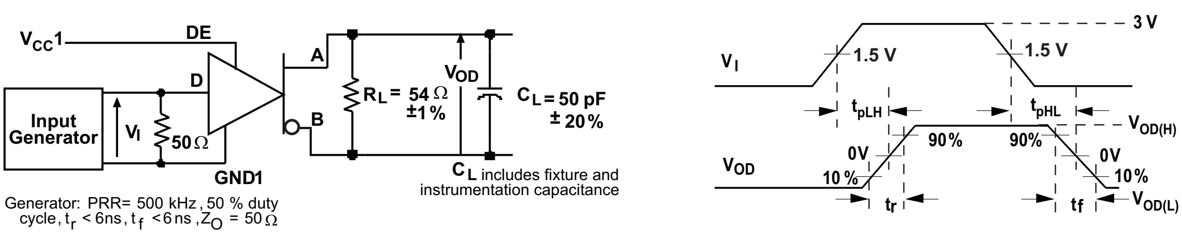

Figure 9. Driver Switching Test Circuit and Waveforms

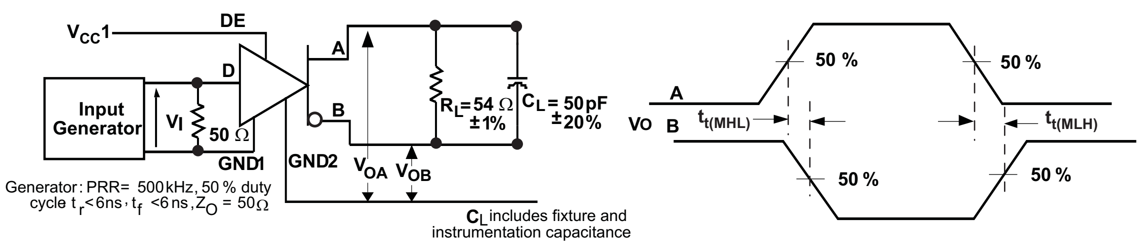

Figure 10. Driver Output Transition Skew Test Circuit and Waveforms

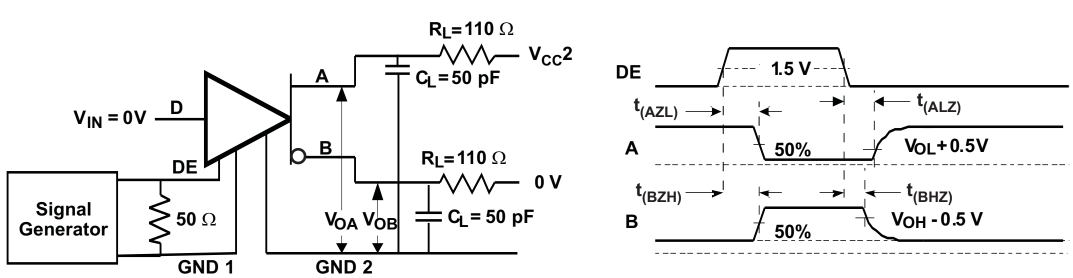

Figure 11. Driver Enable/Disable Test, D at Logic Low Test Circuit and Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)

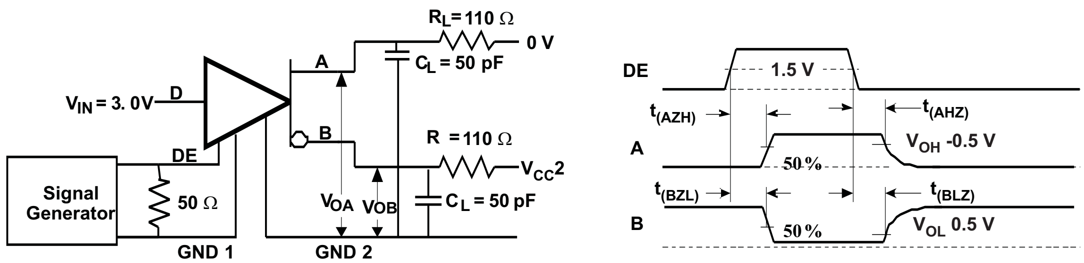

Figure 12. Driver Enable/Disable Test, D at Logic High Test Circuit and Waveforms

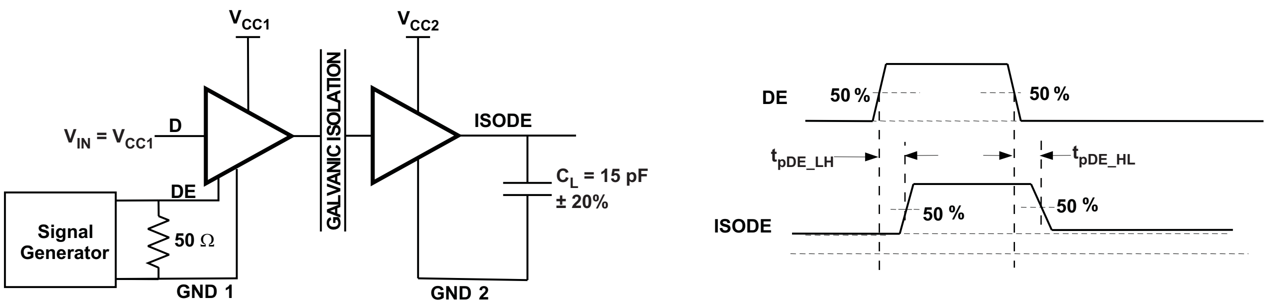

Figure 13. DE to ISODE Prop Delay Test Circuit and Waveforms

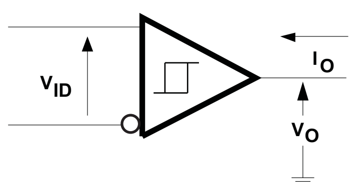

Figure 14. Receiver DC Parameter Definitions

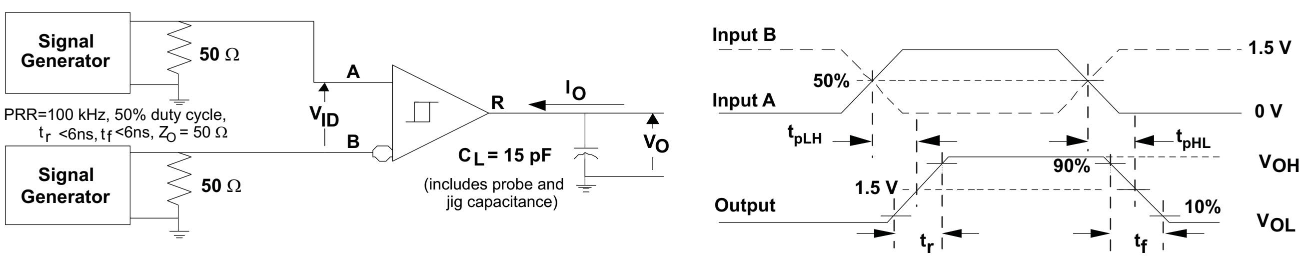

Figure 15. Receiver Switching Test Circuit and Waveforms

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PARAMETER MEASUREMENT INFORMATION (continued)

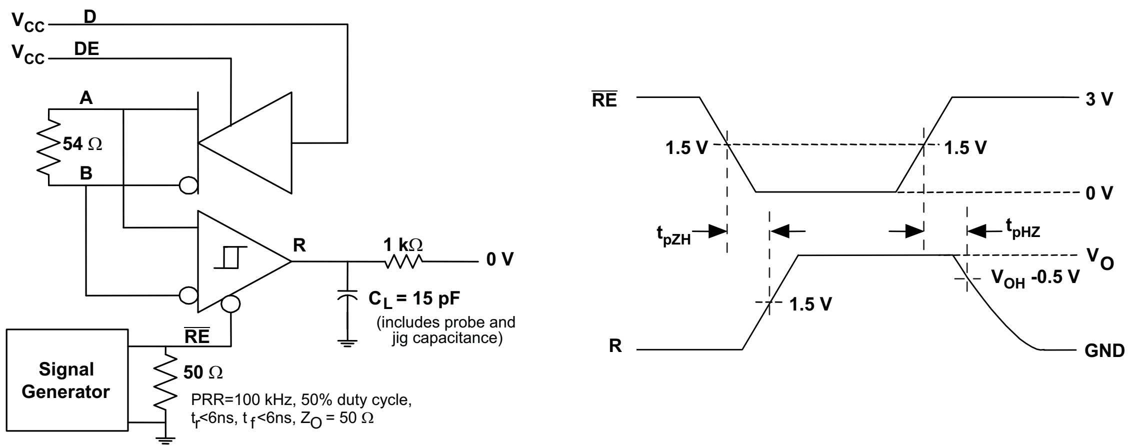

Figure 16. Receiver Enable Test Circuit and Waveforms, Data Output High

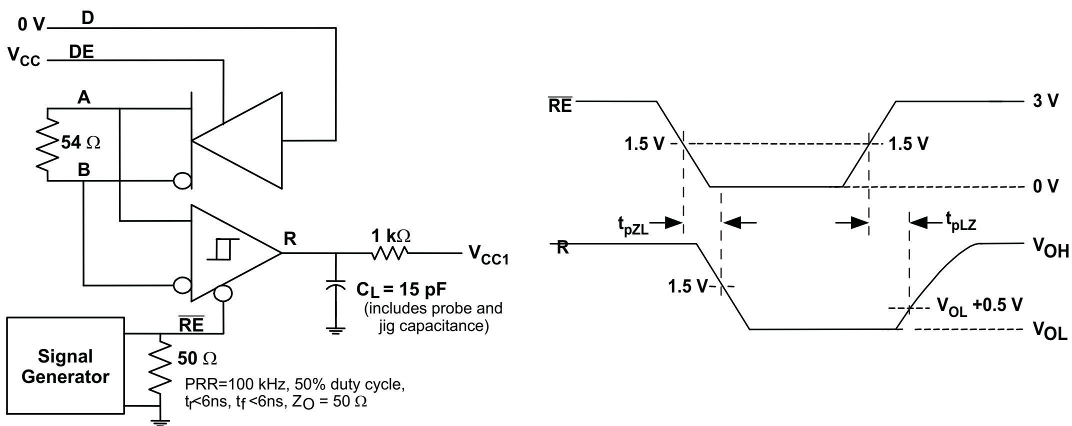

Figure 17. Receiver Enable Test Circuit and Waveforms, Data Output Low

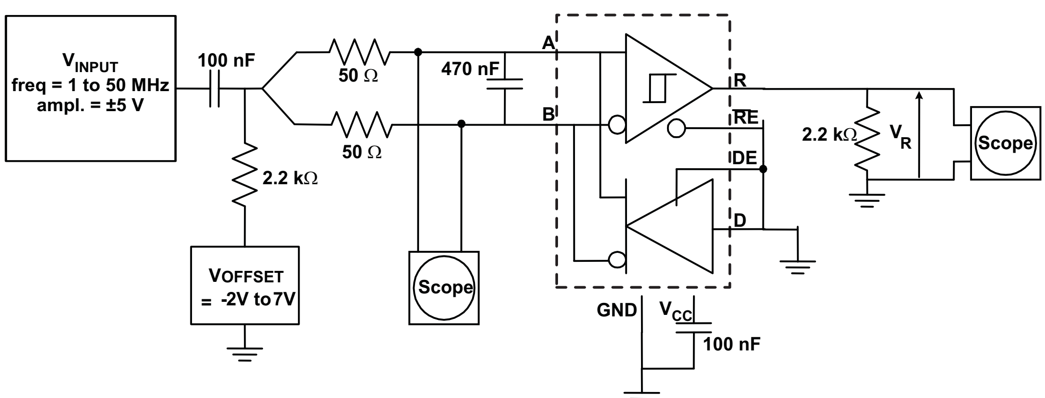

Figure 18. Common-Mode Rejection Test Circuit

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PARAMETER MEASUREMENT INFORMATION (continued)

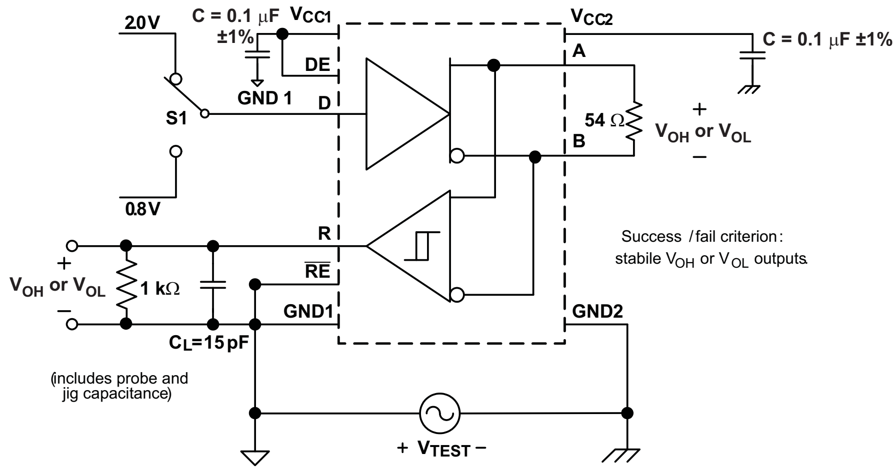

Figure 19. Common-Mode Transient Immunity Test Circuit

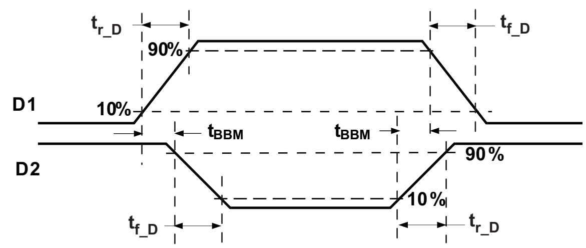

Figure 20. Transition Times and Break Before Make Time Delay for D1, D2 Outputs

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DEVICE INFORMATION

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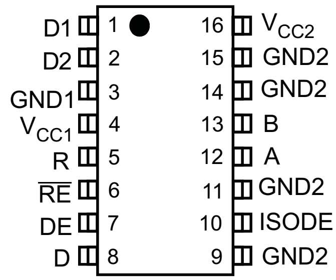

PIN DESCRIPTIONS

NAME	PIN #	FUNCTION
D1	1	Transformer Driver Terminal 1, Open Drain Ouput
D2	2	Transformer Driver Terminal 2, Open Drain Ouput
GND1	3	Logic-side Ground
V_{CC1}	4	Logic-side Power Supply
R	5	Receiver Output
$\overline{RE}$	6	Receiver Enable Input. This pin has complementary logic.
DE	7	Driver Enable Input
D	8	Driver Input
GND2	9, 11, 14, 15	Bus-side Ground. All pins are internally connected.
ISODE	10	Bus-side Driver Enable Output Status
A	12	Non-inverting Driver Output / Receiver Input
B	13	Inverting Driver Output / Receiver Input
VCC2	16	Bus-side Power Supply

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Table 1. DRIVER FUNCTION TABLE[(1)]

V_{CC1}	V_{CC2}	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
					A	B
PU	PU	H	H	H	H	L
PU	PU	L	H	H	L	H
PU	PU	X	L	L	Z	Z
PU	PU	X	open	L	Z	Z
PU	PU	open	H	H	H	L
PD	PU	X	X	L	Z	Z
PU	PD	X	X	L	Z	Z
PD	PD	X	X	L	Z	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don't Care, Z = High Impedance (off)

Table 2. RECEIVER FUNCTION TABLE[(1)]

V_{CC1}	V_{CC2}	DIFFERENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	$–0.01V \le V_{ID}$	L	H
PU	PU	$-0.2V < V_{ID} < –0.01V$	L	?
PU	PU	$V_{ID} \le –0.2V$	L	L
PU	PU	X	H	Z
PU	PU	X	open	Z
PU	PU	Open circuit	L	H
PU	PU	Short Circuit	L	H
PU	PU	Idle (terminated) bus	L	H
PD	PU	X	X	Z
PU	PD	X	L	H
PD	PD	X	X	Z

(1) PU = Powered Up, PD = Powered Down, H = High Level, L= Low Level, X = Don’t Care, Z = High Impedance (off), ? = Indeterminate

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)(1)	Shortest terminal to terminal distance through air	8.3			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	$V_I = V_{CC}/2 + 0.4 \sin(2\pi ft)$, f = 1 MHz, V_{CC} = 5 V		2		pF
C_I	Input capacitance to ground	$V_I = 0.4 \sin(2\pi ft)$, f = 1 MHz		2		pF
P_D	Device power dissipation	V_{CC1} = 5.5V, V_{CC2} = 5.25V, T_J = 150°C, C_L = 15 pF, Input a 20 MHz 50% duty cycle square wave			TBD	mW

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤ $150V_{rms}$	I-IV
	Rated mains voltage ≤ $300V_{rms}$	I-III
	Rated mains voltage ≤ $400V_{rms}$	I-II

IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	Vpeak
V_{PR}	Input to output test voltage	Method b1, $V_{PR} = V_{IORM} \times 1.875$, 100% Production test with t = 1 s, Partial discharge < 5pC	1050	Vpeak
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$, t = 10 s, Partial discharge < 5pC	896	
		After Input/Output Safety Test Subgroup 2/3, $V_{PR} = V_{IORM} \times 1.2$, t = 10 s, Partial discharge < 5 pC	672	
V_{IOTM}	Transient overvoltage	t = 60s (qualification), t = 1s (100% production)	4000	Vpeak
R_S	Insulation resistance	V_{IO} = 500V at T_S = 150°C	$> 10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

PRODUCT PREVIEW

REGULATORY INFORMATION

VDE	UL
Certified according to IEC 60747-5-2	Recognized under 1577 Component Recognition Program(1)
File Number: Pending	File Number: Pending

(1) Production tested ≥ 3000 V_{rms} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			128	mA
T_S	Maximum case temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

THERMAL INFORMATION

THERMAL METRIC(1)		PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	48	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance		
θ_{JB}	Junction-to-board thermal resistance		
ψ_{JT}	Junction-to-top characterization parameter	29	
ψ_{JB}	Junction-to-board characterization parameter	n/a	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

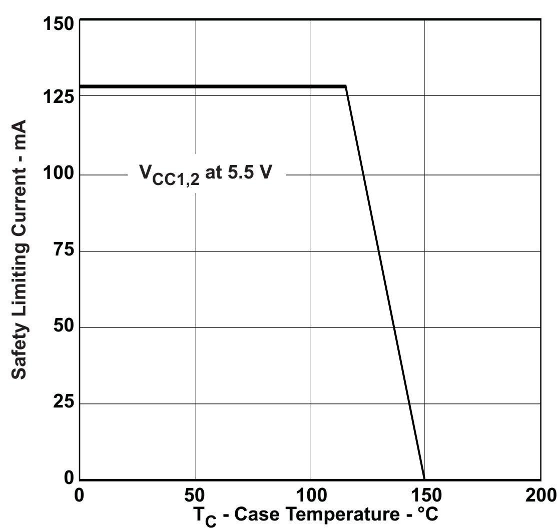
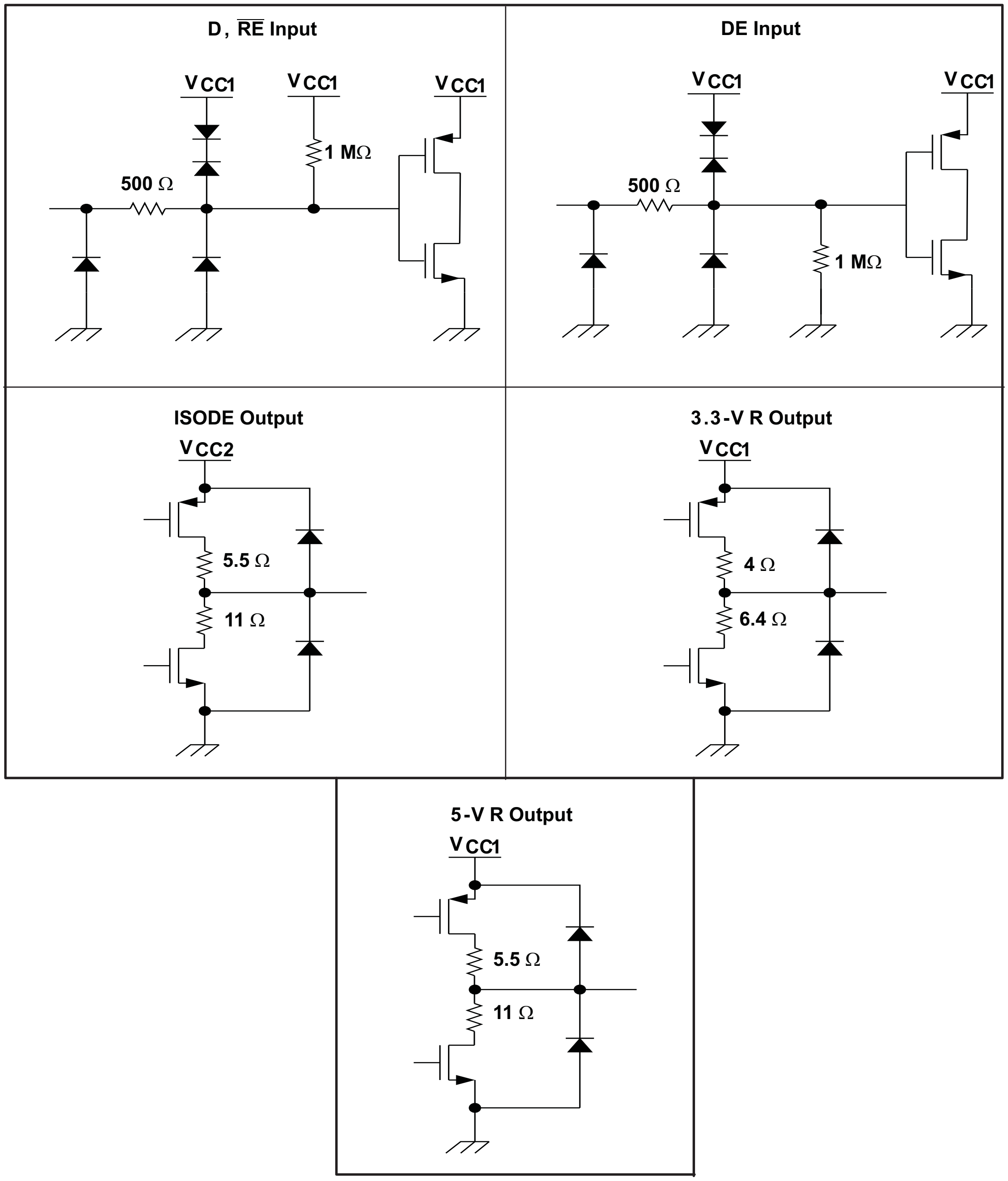


Figure 21. DW-16 θ_{JC} THERMAL DERATING CURVE per IEC 60747-5-2

PRODUCT PREVIEW

EQUIVALENT CIRCUIT SCHEMATICS



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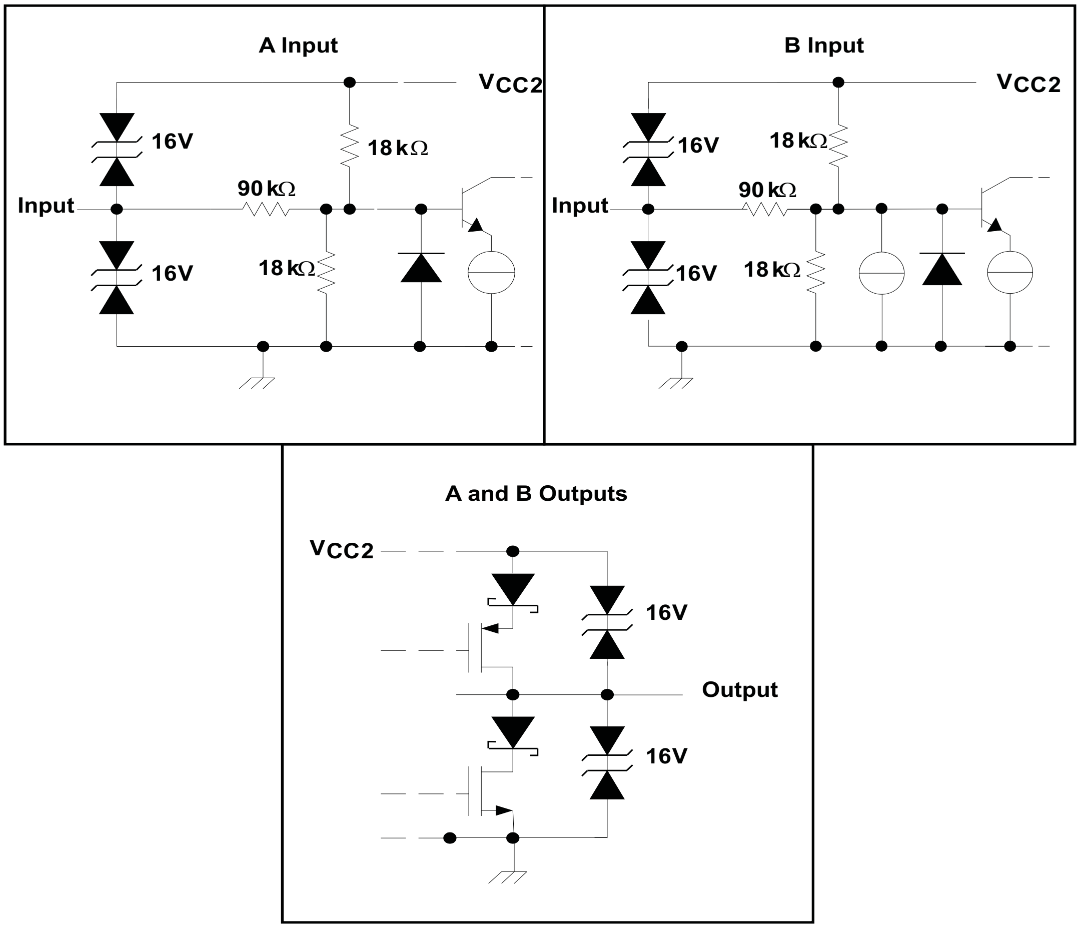

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

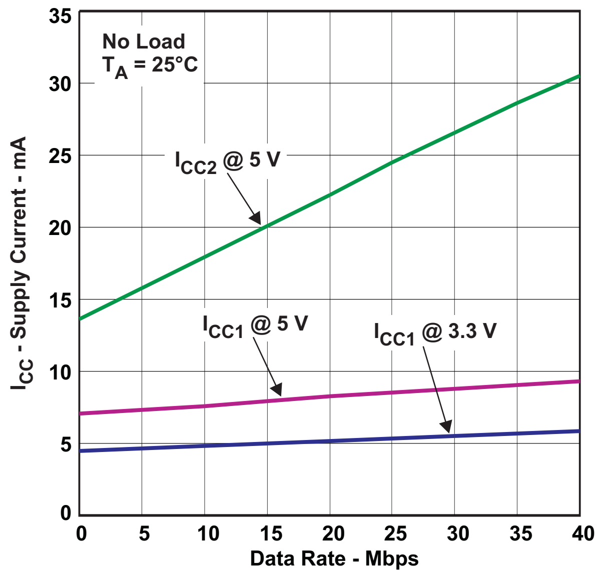

Figure 22. RMS SUPPLY CURRENT (I_{CC1} and I_{CC2}) vs SIGNALING RATE WITH NO LOAD

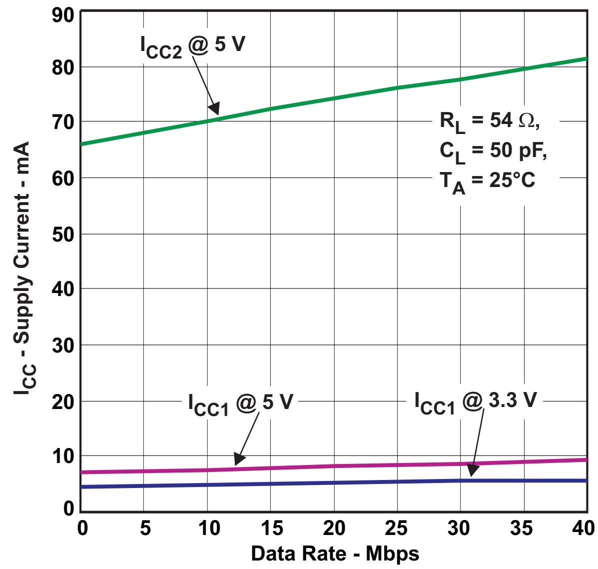

Figure 23. RMS SUPPLY CURRENT (I_{CC1} and I_{CC2}) vs SIGNALING RATE WITH LOAD

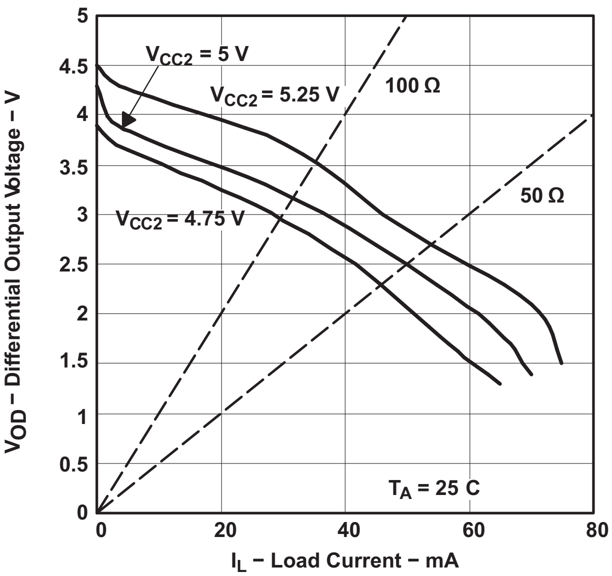

Figure 24. DIFFERENTIAL OUTPUT VOLTAGE vs LOAD CURRENT

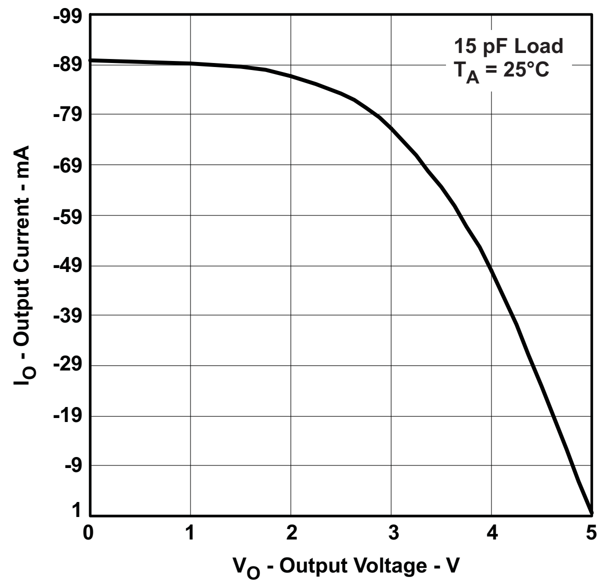

Figure 25. RECEIVER HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

PRODUCT PREVIEW

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

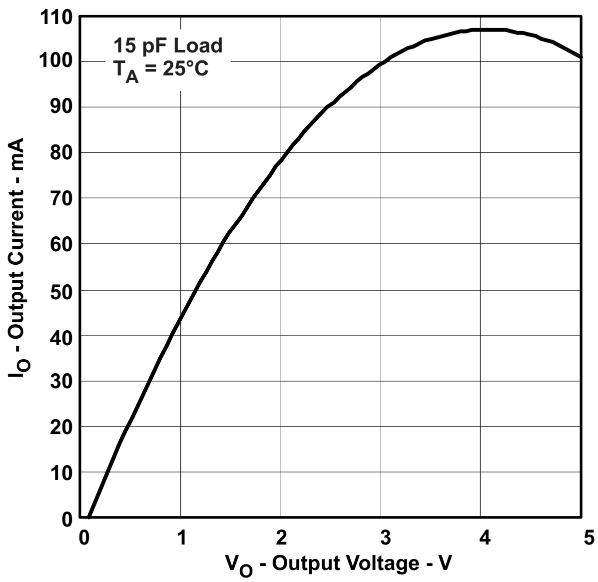

Figure 26. RECEIVER LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

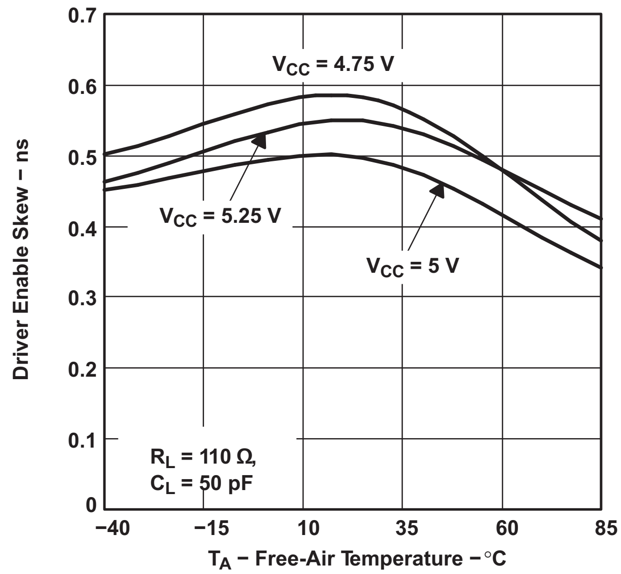

Figure 27. DRIVER ENABLE SKEW vs FREE-AIR TEMPERATURE

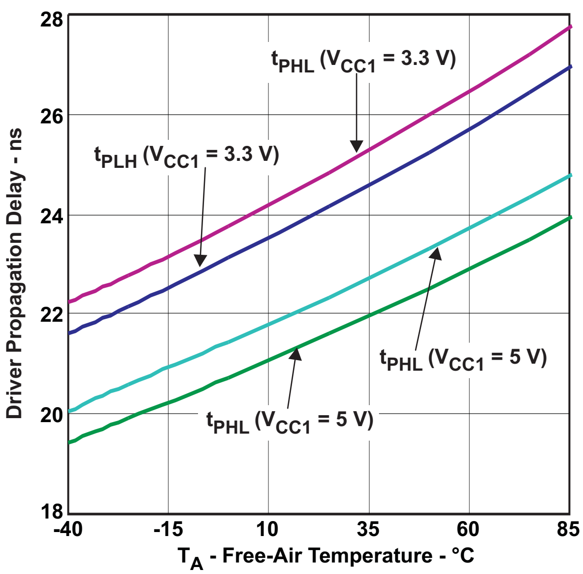

Figure 28. DRIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

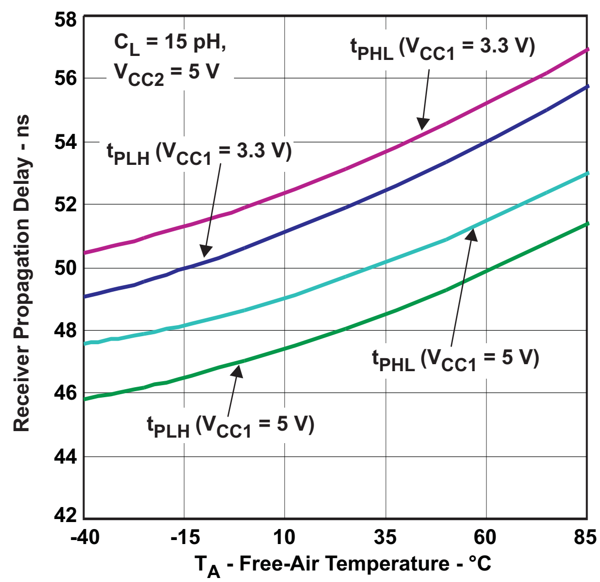

Figure 29. RECEIVER PROPAGATION DELAY vs FREE-AIR TEMPERATURE

APPLICATION INFORMATION

REFERENCE DESIGN

ISO1176T Reference design documentation and boards are available at TBD location

TRANSIENT VOLTAGES

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of ISO1176T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high voltage transients.

Figure 30 models the ISO1176T bus IO connected to a noise generator. C_{IN} and R_{IN} is the device and any other stray or added capacitance or resistance across the A or B pin to GND2, C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of ISO1176T plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is $v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}}$ and will always be less than 16 V from V_N. If ISO1176T is tested as a stand-alone device, $R_{IN} = 6 \times 10^4 \Omega$, $C_{IN} = 16 \times 10^{-12}$ F, $R_{ISO} = 10^9 \Omega$ and $C_{ISO} = 10^{-12}$ F.

Note from Figure 30 that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4}$$

or essentially all of noise appears across the barrier. At very high frequency,

$$\frac{v_{GND2}}{v_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of transient noise appears across the isolation barrier, as it should.

We recommend the reader not test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.

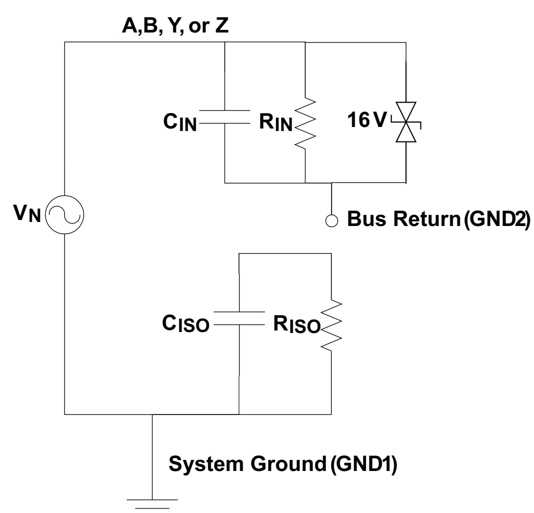

Figure 30. Noise Model

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
ISO1176TDW	PREVIEW	SOIC	DW	16	40	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.t information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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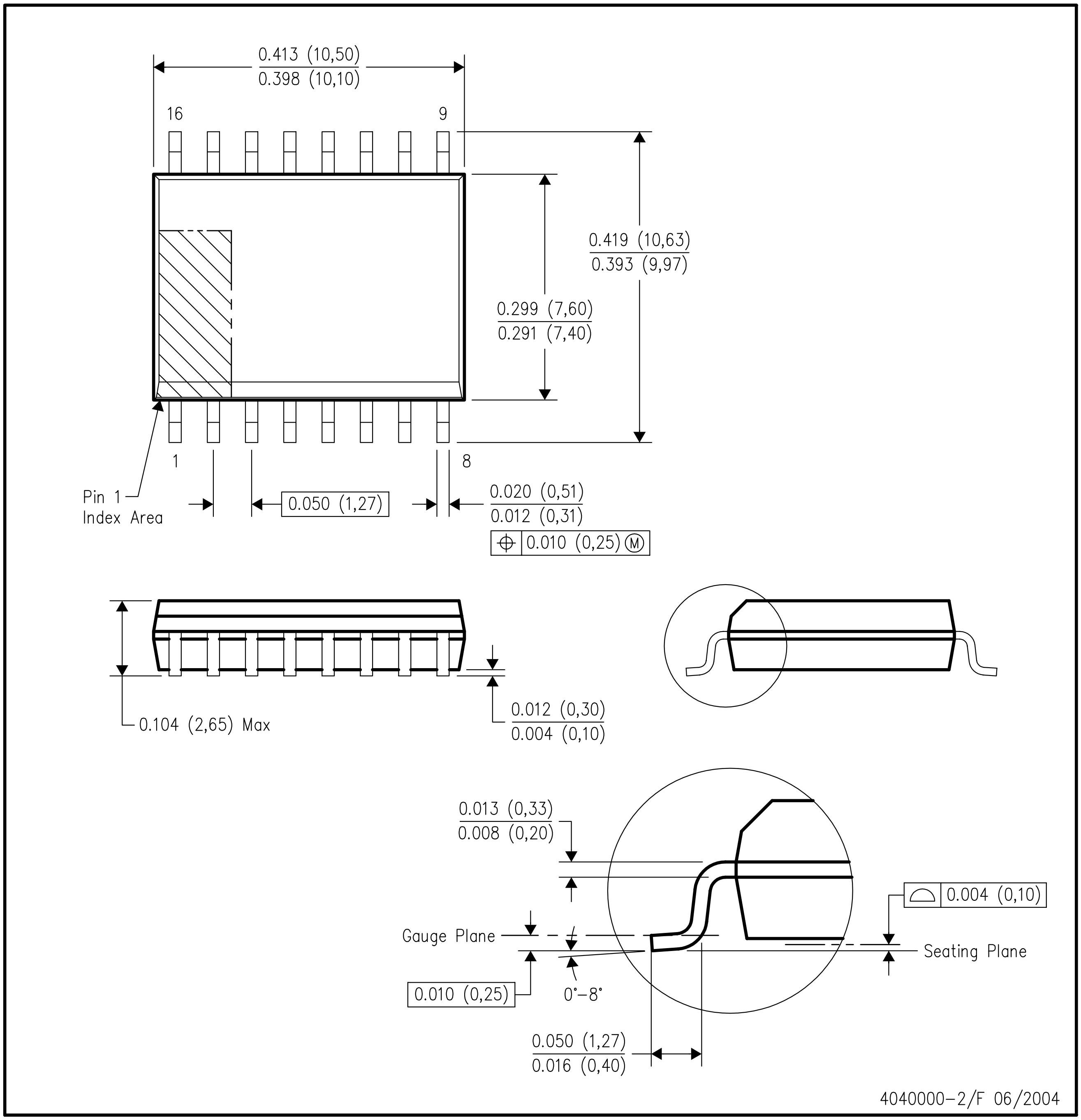
DW (R-PDSO-G16) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

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