October 2004

LM27262
Intel CPU Core Voltage Regulator Controller for VRD10 Compatible PCs

General Description

The LM27262 is a versatile synchronous buck voltage regulator controller designed according to the Intel VRD10 Specification. It's a fixed-frequency voltage-mode control PWM with average current modulation of the reference voltage to achieve the desired output impedance. This approach imparts a pseudo current mode behavior to the control loop. The part provides the control for a voltage regulator consisting of either 2-, 3- or 4-phases to provide power to a desktop CPU. Pulse-by-pulse phase current balancing ensures accurate current sharing. CPU core currents of over 90A can be supported without requiring significant over design of the power path. The LM27262 contains a precision 6-bit digital-to-analog converter (DAC) that uses a VID-code provided by the CPU to program the desired CPU core voltage. The regulator output voltage can be dynamically adjusted by changing the VID-code "on the fly".

The part is intended to provide all the specified functions laid out in the VRD-10 specification, making it as simple as possible for the user to realize a fully compliant CPU core supply for Intel's Pentium™4 and Prescott™ processors.

The LM27262 is available in a 48-lead TSSOP package and in a 48-lead LLP package.

Features

- Compatible with "VRD10 Voltage Regulation Specification" for Intel Pentium 4 and Prescott Processors
- Supports Intel SpeedStep™ technology (Geyserville-III™), which enables real-time dynamic switching of the CPU core voltage and the CPU clock frequency
- Uses external gate drivers (LM2724) for maximum layout flexibility and noise immunity
- Fixed frequency PWM architecture
- Pin selectable internal or external voltage reference
- 0.5% core voltage set-point accuracy when using external voltage reference
- 0.9% accurate internal bandgap reference
- 2-, 3- or 4-phase operation
- Out-of-phase switching reduces input ripple current, thereby minimizing input capacitor requirements
- VID-code programmable output voltage range of 0.8375V through 1.6000V
- User programmable, low loss, load line slope
- User programmable Standard VID offset
- User programmable VCORE slew rate
- 5V power rail Under Voltage Lock Out (UVLO)
- Over Voltage Protection (OVP), Under Voltage Protection (UVP), and Over Current Protection (OCP) to defend against potentially catastrophic events
- User programmable fault latch that can be used to disable the regulator in the event a power system fault
- Very fast transient response
- VID-transition masked PWRGOOD output
- True-differential current sensing for each phase ensures accurate load current sharing
- User programmable cycle-by-cycle current limit

Key Specifications

- Fast transient response to minimize output capacitor requirements
- Shorter design cycles through the use of external gate drivers for reduced power dissipation, ease of PCB layout and reduced noise sensitivity
- Fully integrated solution. All VRD-10 control functions provided by a single device
- Accurate current balancing eliminates need to over design the power path
- Fixed frequency PWM minimizes EMI issues
- Low input capacitor requirements due to multi-phase interleaving
- Fault latching allows use of smaller power path components and minimizes the chance of damage to the load in the event of a fault
- Only need to buy as many drivers as the design needs while keeping only one controller in inventory

Applications

- Server and desktop computer CPU core power supplies requiring a 2, 3- or 4-phase voltage regulator delivering up to 100A
- Transportable notebook computers using desktop CPUs
- Low cost transportable notebook computers using 2- or 3-phase designs

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Typical Application Circuit

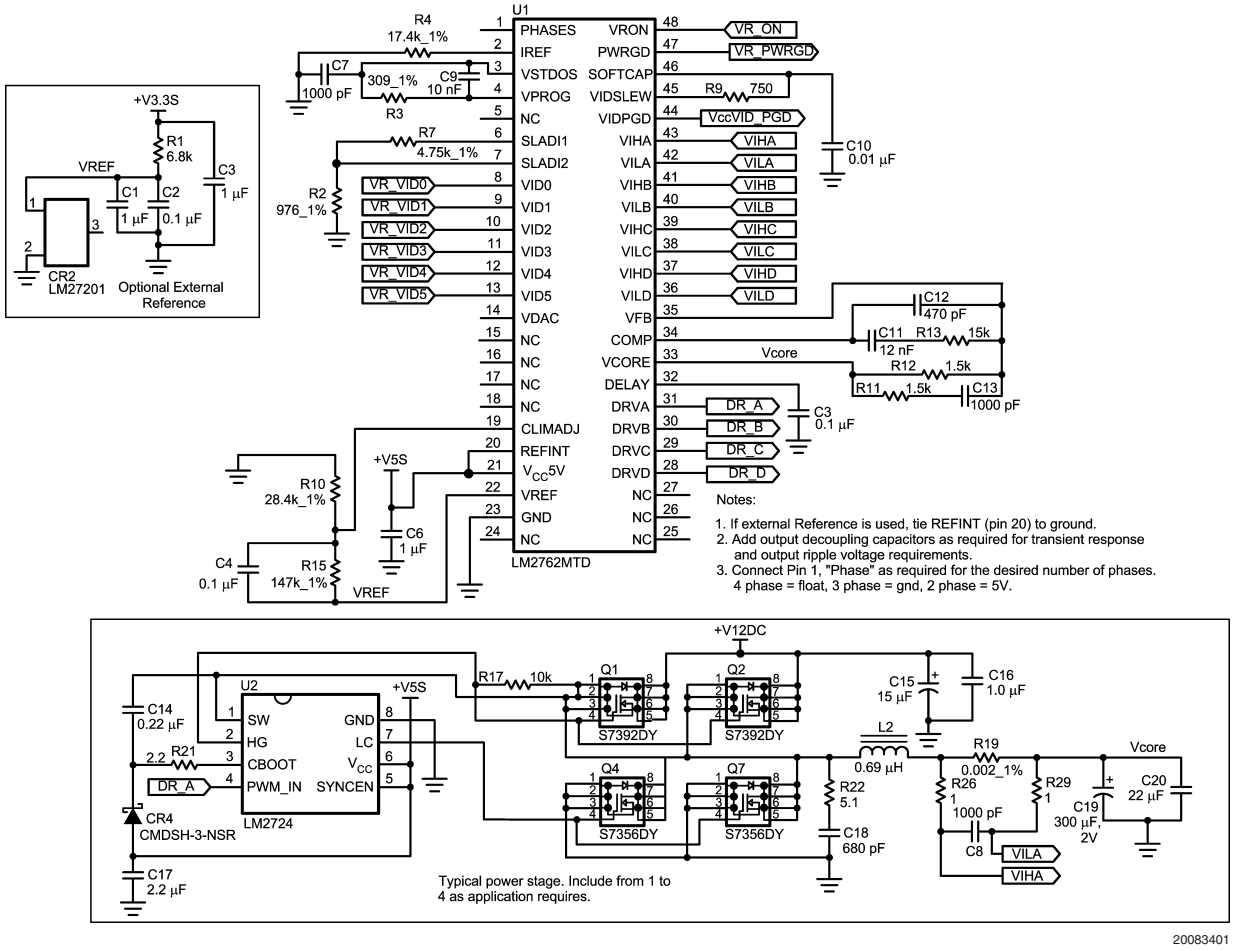
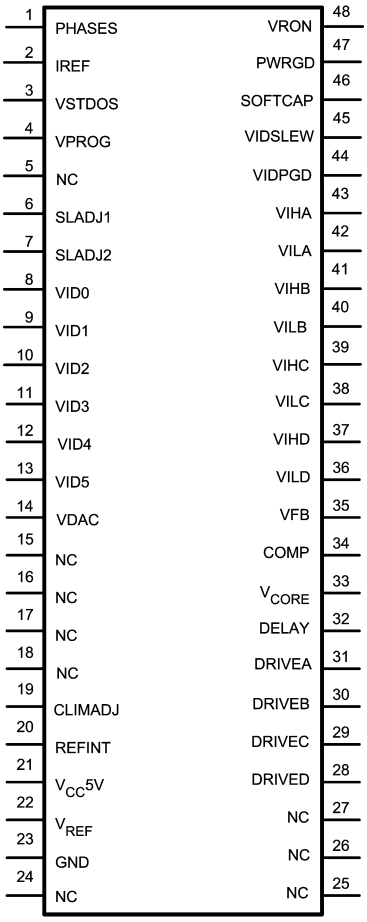


FIGURE 1.

Connection Diagrams

Top View



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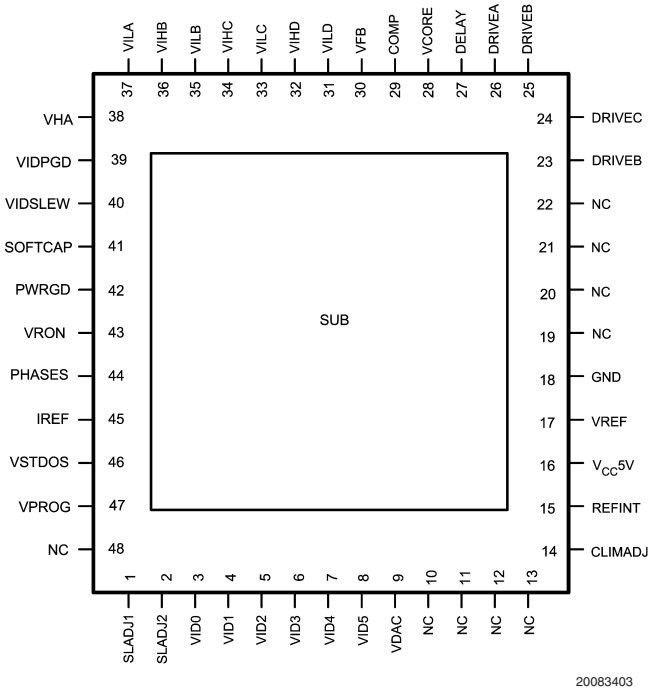
48-Lead TSSOP (MTD)
Order Number LM27262MTD
See NS Package Number MTD48

Top View



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48-Lead LLP
Order Number LM27262LQ
NS Package Number LQA48B

Ordering Information

Order Number	Package Drawing	Supplied As
LM27262MTD	MTD48	38 Units/Rail
LM27262MTDX	MTD48	1000 Units Tape and Reel
LM27262LQ	LQA48B	1000 Units Tape and Reel
LM27262LQX	LQA48B	4500 Units Tape and Reel

Pin Description

(All pin numbers referred to here correspond to the TSSOP/LLP package)

Pin 1/44, PHASES: tri-level logic input: HIGH logic level switches controller into 2-phase operation mode, phases A and C active. LOW logic level activates 3-phase operation, phases A, B and C active, OPEN (floating) input activates 4-phase operation

Pin 2/45, IREF: connect a 1% resistor to ground to program a precision current source for a standard offset voltage, typically –25mV, across a resistor connected between VPROG and VSTDOS pins. Recommended current value is approximately 80µA. Typical resistor value is R = 1.4V / 80µA equals 17.4k.

Pin 3/46, VSTDOS: input; $V_{VSTDOS} = V_{VPROG} - V_{OS}$. This pin allows setting a programmable offset voltage (typically 25mV). The offset is programmed via an external 1% resistor connected between the VPROG and VSTDOS pins. The offset is the Pin 2 current multiplied by this offset programming resistor.

Pin 4/47, VPROG: output used for programming a standard offset. Connect a 1% resistor between VPROG and VSTDOS. VPROG output voltage is the buffered internal DAC output.

Pin 5/48: No connect pin

Pin 6/1, SLADJ1: load line slope adjustment via external resistor divider

Pin 7/2, SLADJ2: load line slope adjustment via external resistor divider

Pin 8 – 13/3-8, VID0-VID5: voltage identification code inputs

Pin 14/9, VDAC: buffered output of onboard DAC. Voltage determined by VID code.

Pin 15-18/10-13: no connect pin

Pin 19/14, CLIMADJ: output current limit adjustment input for one phase. For 4-phase operation the current limit is 4x the single phase current limit, for 3-phase operation it is 3x the single phase limit, and 2x the single phase current for 2-phase operation

Pin 20/15, REFINT: internal/external voltage reference selection logic input. When logic high, selects internal reference

Pin 21/16, VCC5V: 5V power supply input to the part. Should be decoupled to GND pin with a 1uF capacitor.

Pin 22/17, VREF: internal voltage reference output or external voltage reference input depending on REFINT input logic state

Pin 23/18, GND: the chip ground pin. Use for 5V supply ground connection, Make a single-point ground connection at this pin.

Pin 24 – 27/19-22: no connect pins

Pin 28-31/23-26: DRIVED-DRIVEA: PWM logic level outputs for phases D through A. **Not short-circuit protected.**

Pin 32/27, DELAY: OVP, UVP and OCP latch-off delay adjustment pin. A delay programming capacitor is connected between this pin and ground. This pin disables UVP, OVP and OCP latch-off when grounded to facilitate debugging

Pin 33/28, VCORE: CPU core voltage rail connection. This pin is the OVP/UVP sense point.

Pin 34/29, COMP: output of error amplifier. Use for external loop compensation connection

Pin 35/30, VFB: input of error amplifier. Use for external loop compensation connection Pin 36/31, VILD: phase D current sense resistor low-side connection input

Pin 37/32, VIHD: phase D current sense resistor high-side connection input

Pin 38/33, VILC: phase C current sense resistor low-side connection input

Pin 39/34, VIHC: phase C current sense resistor high-side connection input

Pin 40/35, VILB: phase B current sense resistor low-side connection input

Pin 41/36, VIHB: phase B current sense resistor high-side connection input

Pin 42/37, VILA: phase A current sense resistor low-side connection input

Pin 43/38, VIHA: phase A current sense resistor high-side connection input

Pin 44/39, VIDPGD: VID Power Good Delayed output. Outputs a VID_PWRGD signal that is delayed approximately 2msec after receiving an externally supplied active high signal to VRON. Pin VIDPGD should be connected to the system's VID_PWRGD input. This delay ensures that Vcore will power on only after the 6 VID bit signals have settled. The LM27262 is only enabled after the delay has timed out.

Pin 45/40, VIDSLEW: connect a resistor between this pin and the SOFTCAP pin to program VCORE slew rates for VID transitions

Pin 46/41, SOFTCAP: soft start/soft stop capacitor connection; this output sources charging current to the softstart capacitor at power on. An internal 50k resistor discharges the softstart capacitor during power off

Pin 47/42, PWRGD: power good output, open drain, active high

Pin 48/43, VRON: logic input that turns the switching regulator on and off. If VCC5V is present when the LM27262 is shutdown then the DRIVEx outputs are active low. VRON has a 2msec assertion delay. When VRON is de-asserted, the VID DAC latches the latest VID code and executes soft-stop. There is no de-assertion delay on VRON.

LLP DAP, SUB: die substrate. The exposed die attach should be connected to ground potentful.

Processor Pins (0 = low, 1 = high)						
VID5	VID4	VID3	VID2	VID1	VID0	V_{OUT} (V)
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF
0	1	1	1	1	1	OFF
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	0	0	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
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0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750
0	0	1	1	1	1	1.4875
1	0	1	1	1	0	1.5000
0	0	1	1	1	0	1.5125
1	0	1	1	0	1	1.5250
0	0	1	1	0	1	1.5375
1	0	1	1	0	0	1.5500
0	0	1	1	0	0	1.5625
1	0	1	0	1	1	1.5750
0	0	1	0	1	1	1.5875
1	0	1	0	1	0	1.6000

FIGURE 2. VID Code vs DAC Output

Absolute Maximum Ratings (Notes 1, 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC}5V	-0.3V to 7V
PHASES, IREF, VSTDOS, VPROG, SLADJ1, SLADJ2, VREF, REFINT, CLIMADJ, VCORE, COMP, VFB, VILx, VIHx, SOFTCAP, PWRGD, VIDPGD, VID0-VID5, VRON	-0.3V to V_{CC}5V + 0.3V
Differential Voltage (VILx – VIHx)	1V
Ambient Storage Temp. Range	-65˚C to +150˚C
Junction Temperature	-20˚C to +150˚C
Minimum ESD Rating (Note 4)	±2kV
Human Body Model	100pF
Machine Model	1.5 kΩ
Soldering Dwell Time, Temperature (Note 3)	
Wave	4sec, 260˚C
Infrared	10sec, 240˚C
Vapor Phase	75sec, 219˚C

Operating Ratings (Note 1)

V_{CC}5V	4.65V to 5.5V
Junction Temperature (Note 2)	0˚C to +110˚C

Electrical Characteristics (Note 5),(Note 6) V_{CC}5V = 5V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Q5V}	Quiescent V_{CC}5V current	V_{CC}5V = 5.5V, not switching		8.4	10.5	mA
I_{Q5V}	Quiescent V_{CC}5V current	V_{CC}5V = 5.5V, 4-phase switching		8.5	11	mA
I_{SD5V}	Shutdown V_{CC}5V current	V_{CC}5V = 5.5V, VRON = Low		0.1	10	µA
T_{SD}	Thermal Shutdown Threshold	Rising temperature		165		˚C
T_{SDH}	Thermal Shutdown Threshold Hysteresis			10		˚C
UNDER VOLTAGE LOCKOUT						
V_{5UVLO}	VCC5V UVLO THreshold	Rising Edge	**4.15**	4.3	**4.6**	V
		Falling Edge	**3.85**	4.05	**4.35**	
V_{5UVLOH}	VCC5V UVLO Hysteresis			0.25		V
DAC: VID0-5, VDAC						
	VID0-5 Inputs Logic LOW				**0.4**	V
	VID0-5 Inputs Logic HIGH		**0.8**			V
	VID0-5 Low-to-High Threshold			0.7		V
	VID0-5 Threshold Hysteresis			0.2		V
	VID0-5 Inputs Internal Pull-up Current	VID0-5 = Low		5	**20**	µA
	DAC Output Voltage Programming Resolution	Per VID code table, Measured at VPROG		12.5		mV
		DAC Accuracy measured at VPROG pin over -5˚C < T_J < 110˚C				

Electrical Characteristics (Note 5),(Note 6) $V_{CC}5V$ = 5V unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	DAC Voltage Accuracy with Internal VREF	VID codes from 1.5625V to 1.6000V		±0.9		%
		VID codes from 0.8375V to 1.1000V		±0.9		%
		VID codes from 1.1125V to 1.5500V		±0.75		%
	DAC Voltage Accuracy with External VREF = 1.225V	VID codes: 1.5500V & 1.6000V	-0.6 **-0.8**	±0.15	0.75 **0.8**	%
		VID codes: 0.8375V & 1.0000V	-1.0 **-1.2**	-0.15	1.0 **1.2**	%
		VID codes: 1.1000V, 1.2000, 1.3000, 1.4000 & 1.5000	-0.5 **-0.8**	±0.1	0.5 **0.8**	%
REFERENCE VOLTAGE						
	Internal Reference Voltage		**1.210**	1.235	**1.260**	V
	VREF Output Load Regulation	I_{VREF} from 0 to 50 µA		-2.5		mV
	VREF Line Regulation	$V_{CC}5V$ = (4.65V to 5.5V), I_{VREF} = 50uA		±0.2		mV
	External VREF Voltage	REFINT=LOW, see LM27201 Electrical Specs.		1.225		V
	External VREF Compensating Offset (applied internally)	REFINT=LOW		10		mV
STANDARD OFFSET PROGRAMMING INPUTS: VPROG, VSTDOS, IREF						
	IREF Output Voltage	100 µA Load Current		1.400		V
	VOS (VSTDOS-VPROG)	IREF = 80.4 µA, R_{OS} = 309		-25		mV
LOAD LINE SLOPE ADJUSTMENT (SLADJ), CURRENT LIMIT (CLIMADJ)						
	SLADJ2 Input Source Current	SLADJ2 connected to GND		0.07		µA
	CLIMADJ Input Source Current	$V_{CLIMADJ}$ = VREF		2		µA
	Load Line Slope (LLS)	SLADJ divider 41.2k/8.45k, R_{SENSE} = 2mΩ		-1.3		mΩ
	LLS Maximum Error	Nominal LLS = -1.3mV/A, I_{SLADJ1} = 50 µA, Isense diff. input = 20mV; not switching		±0.06		mΩ
CURRENT SENSE LINES VILx AND VIHx						
	Current Sense Amplifier Input Offset Voltage	Common Mode Voltage = 1.30V		±0.5		mV
	Current Sense Differential Voltage Range	Over full VID range		0-100		mV
	Current Sense Input Source Current	VIHx = VILx = 100mV		14	**25**	µA
	Differential Input Resistance	Common Mode Voltage = 1.3V		1		kΩ
CORE VOLTAGE ERROR AMPLIFIER						
	VCORE Input Bias Current	VFB = 1.4V		0.3		µA
	COMP Output Sink Current	Vcomp = 2.5V VFB = 5V		100		µA
	COMP Output Source Current	Vcomp = 4V VFB = 0V		0.5		mA
	VFB Input Bias Source Current	VFB = 1.4V VDAC = 1.3V			1.0	µA

Electrical Characteristics (Note 5),(Note 6) V_{CC}5V = 5V unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Error Amp Input Offset Voltage	VDAC = 1.3V		±1		mV
	Error Amplifier Open loop DC Gain	VFB = 1.3V, Comp Pin open		730		V/V
OSCILLATOR						
	Active Mode Switching Frequency		**235**	300	**345**	kHz
	Minimum On-Time			120		ns
	Maximum Duty Cycle			75		%
SOFT START AND SOFT STOP (SOFTCAP), VIDSLEW						
	SOFTCAP Charge Current		**2.2**	3.2	**4.4**	µA
	SOFTCAP Discharge Resistor	Measured from SOFTCAP pin to GND pin		50		kΩ
DELAY FUNCTION						
	DELAY Source/Charge Current	V_{DELAY} = 0V	**9**	12	**15**	µA
	DELAY Discharge Current	V_{DELAY} = 5V		1		mA
	DELAY Threshold Voltage	V_{DELAY} rising		1.4		V
PWRGOOD, UVP, OVP FAULT LATCHING THRESHOLD						
VPGH%	PWRGD OVP Threshold	Difference of VCORE pin above EA int. reference voltage measured at VFB pin in test mode; VID = 110110 = 1.3V, V_{OS} = 25mV		0.23		V
VPGL%	PWRGD UVP Threshold	Percentage of VCORE pin below EA int. reference voltage measured at VFB pin in test mode; VID = 110110 = 1.3V, V_{OS} = 25mV	**86**	89	**92**	%
	PWRGD Output Low Voltage	PWRGD sinking 4mA (open drain)		0.15		V
	PWRGD Leakage Current	PWRGD pulled up to 5.5V		1	10	µA
	VCORE OVP Latch Threshold	Difference of VCORE pin above EA int. reference voltage measured at VFB pin in test mode; VID = 110110 = 1.3V, V_{OS} = 25mV		0.23		V
	VCORE UVP Latch Threshold	Percentage of VCORE pin below EA int. reference voltage measured at VFB pin in test mode; VID = 110110 = 1.3V, V_{OS} = 25mV	**86**	89	**92**	%
V_{RON}						
	Low Logic Level Input Voltage				**0.3**	V
	High Logic Level Input Voltage		**1.2**			V
	Low-to-High Voltage Threshold			0.95	-	V
	V_{RON} Threshold Hysteresis			0.1	-	V
	V_{RON} Leakage Current	V_{VRON} = 3.3V		5	**20**	µA
		V_{VRON} = GND		50		nA
	V_{RON} Assertion Delay	Delay of power on after VRON transition (SOFTCAP = 0.01µF)		2		msec

Electrical Characteristics (Note 5),(Note 6) V_{CC}5V = 5V unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	VRON De-assertion Delay	Delay of VRON falling edge by the internal logic		50		nsec
REFINT						
	REFINT Leakage Current	REFINT = 3.3V or GND		±2		µA
	Logic Low Input Voltage			0.5		V
	Logic High Input Voltage			3.0		V
PHASES						
	PHASES Leakage Current	V_{PHASES} =0V		- 25		µA
		V_{PHASES} = 3.3V		4		µA
	PHASES Open Circuit Voltage	10MΩ to Ground		2.8		V
	Logic Low Max Input Voltage			0.2		V
	Logic High Min Input Voltage	Relative to Vcc (5V nominal)		-0.2		V
LOGIC OUTPUTS: DRIVEx						
	Output High Voltage	Output Source Current is 10 mA		3.5		V
		Output Source Current is 0 mA (no load)		4.5		
	Output Low Voltage	Output Sink Current is 10 mA		0.3		V
	Low-to-High Transition Time	10% to 90% of V_{CC}5V, C_{LOAD} = 50pF		20		ns
	High-to-Low Transition Time	90% to 10% of V_{CC}5V, C_{LOAD} = 50pF		20		ns
VIDPGD						
	VIDPGD Output Max Low Voltage	VIDPGD sinking 4mA (open drain)		0.17	0.25	V
	VIDPGD Leakage Current	VIDPGD = 5.5V		1	10	µA
	VIDPGD Assertion Delay	VRON assertion to VIDPGD assertion (SOFTCAP = 0.01µF)		2		ms
	VIDPGD De-assertion Delay	VRON de-assertion to VIDPGD de-assertion		50		ns

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics table.

Note 2: The maximum allowable power dissipation is calculated by using $P_{Dmax} = (T_{JMAX} - T_A) / \theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 1.56W rating results from using 150˚C, 25˚C, and 80˚C/W for T_{JMAX}, T_A, and θ_{JA} respectively. The θ_{JA} of 90˚C/W represents the worst-case condition with no heat sinking of the 48-Pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation should be de-rated by 12.5mW per ˚C above 25˚C ambient. The LM27262 actively limits its junction temperature to about 165˚C.

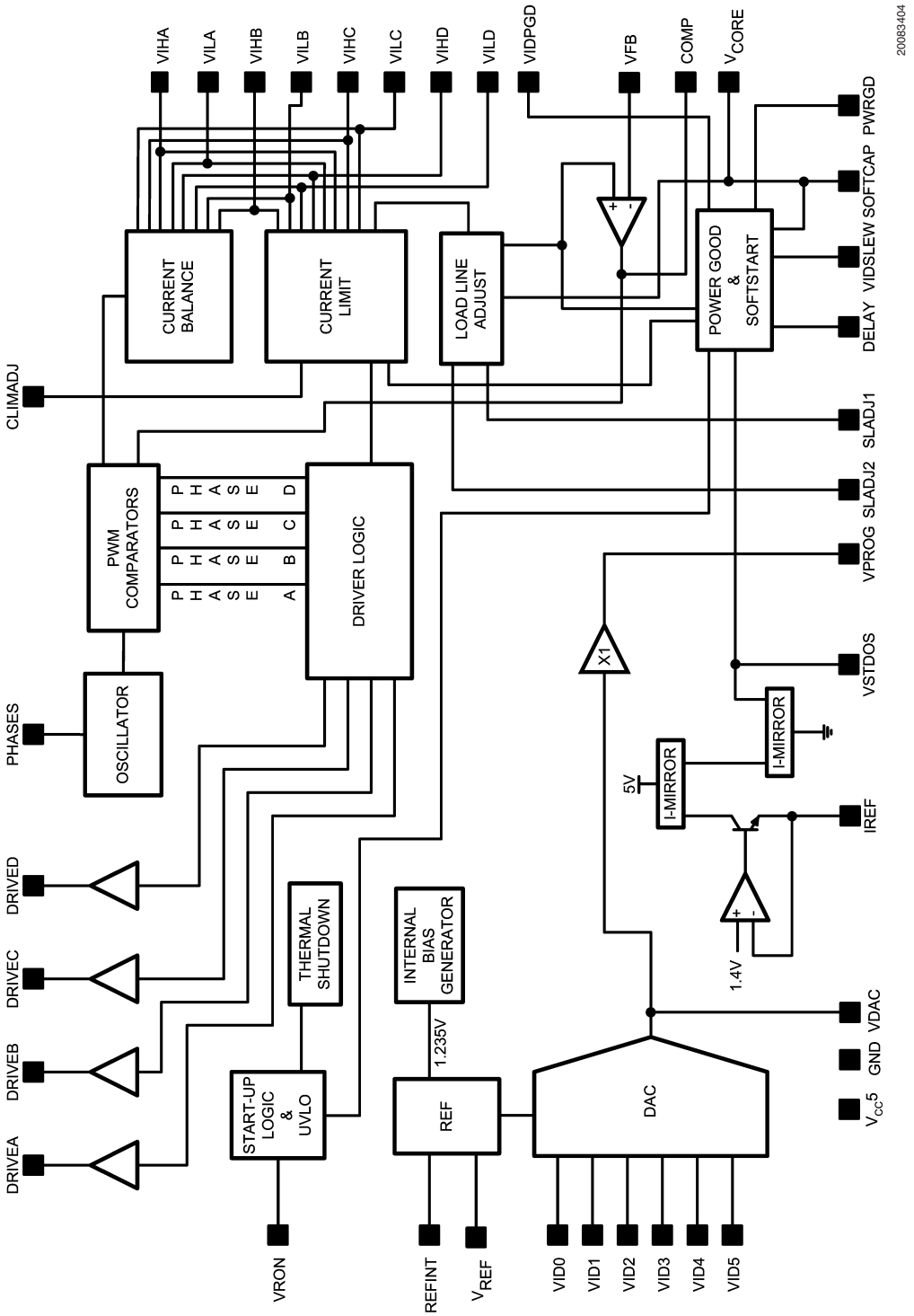
Note 3: For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook available from National Semiconductor Corporation.

Note 4: For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.

Note 5: All limits are guaranteed at room temperature (standard face type) and at temperature extremes (bold face type). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

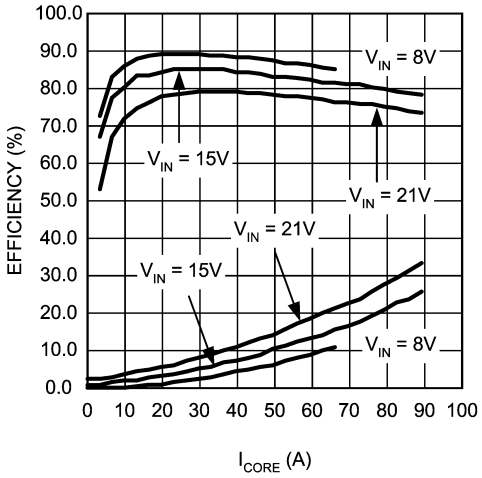
Note 6: A “typical” specification is the center of characterization data distribution taken with $T_A = T_J = 25$˚C. Typical data are not guaranteed.

Block Diagram



Typical Performance Characteristics

LM27262 Efficiency vs I_{CORE}



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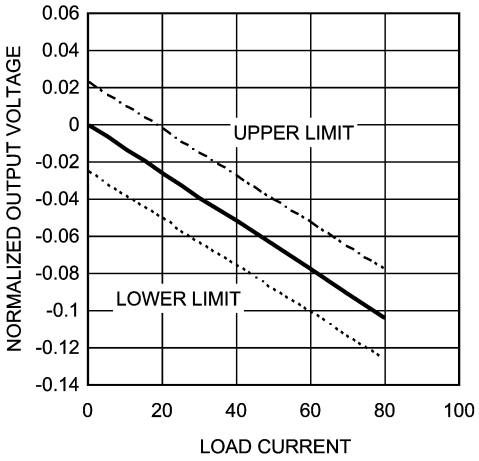
LM27262 V_{CORE} vs I_{CORE}



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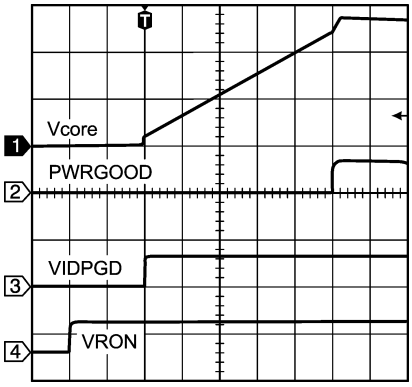
Soft-Start



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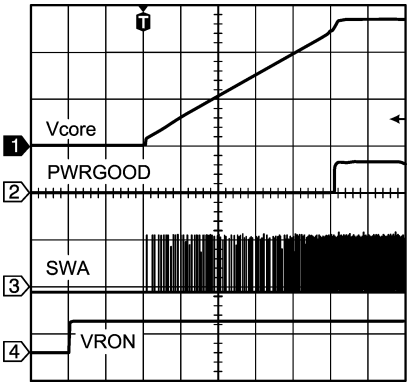
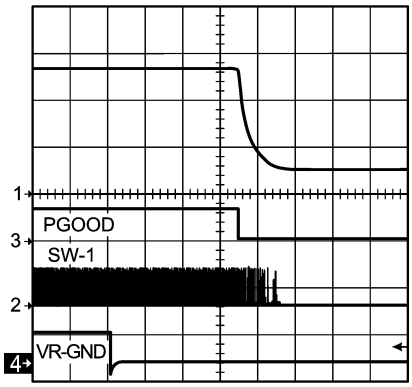
Soft-Start



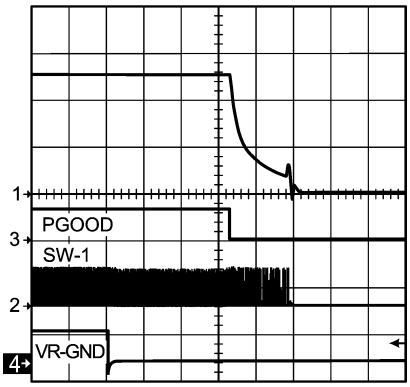
20083408

Soft-Stop at I_{CORE} = 0A



20083409

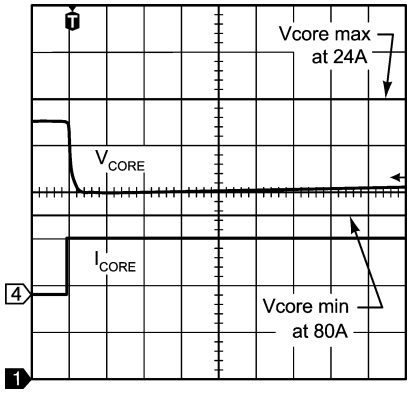
Soft-Stop at I_{CORE} = 30A



20083410

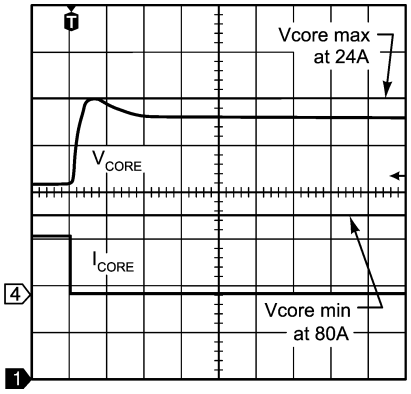
Typical Performance Characteristics (Continued)

Load Transient 24A to 75A



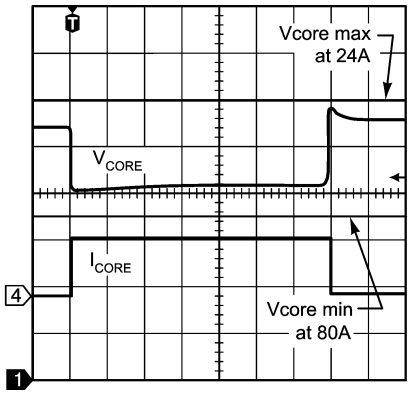
20083413

Load Transient 75A to 24A



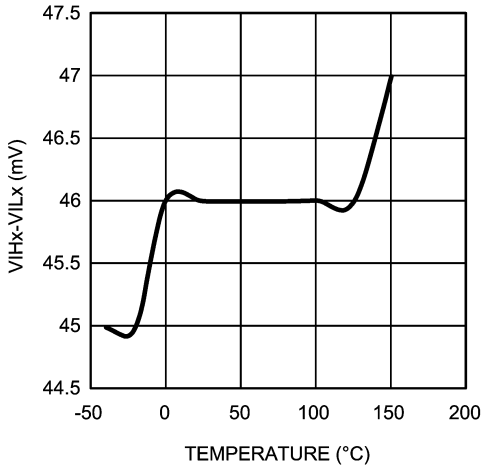
20083414

Load Transient 24A to 75A to 24A



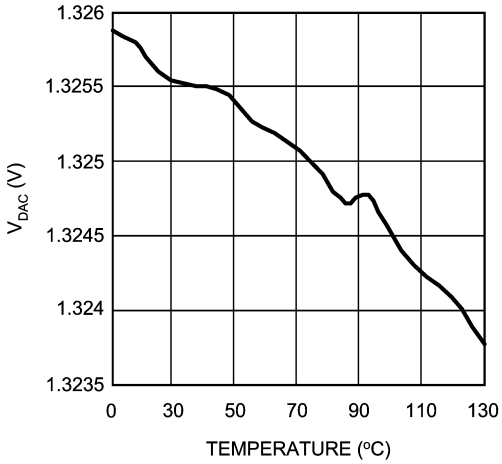
20083415

Over Current Protection Threshold vs Temperature



20083416

V_{DAC} vs Temperature
External Ref, DAC Trim @ 1.325V



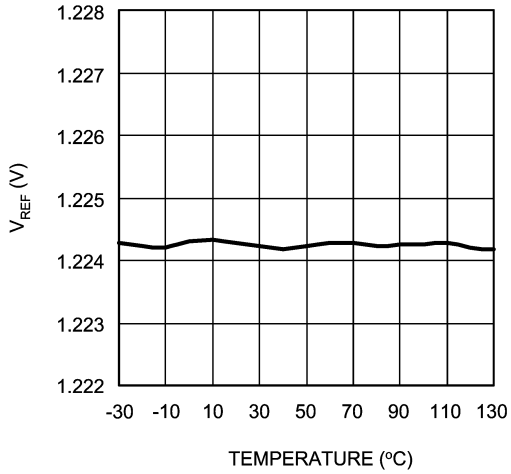
20083417

V_{DAC} vs Temperature
External Ref, DAC Trim @ 1.525V

20083418

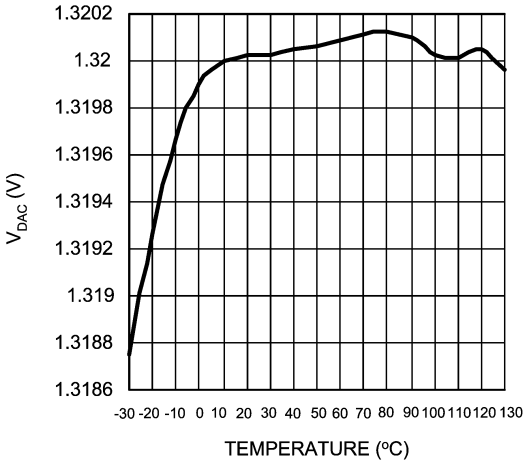
Typical Performance Characteristics (Continued)

External V_{REF} vs Temperature (LM27201)



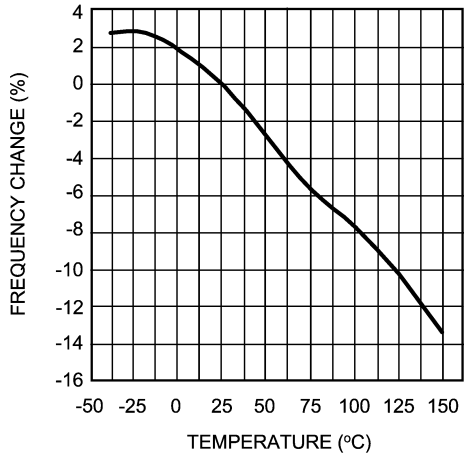
20083419

V_{DAC} vs Temperature
Internal Ref, DAC Trim @ 1.325V



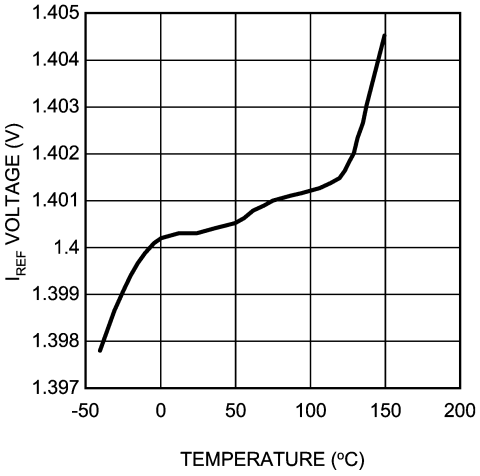
20083420

Switching Frequency Percent Change vs Temperature



20083421

Pin I_{REF} Voltage vs Temperature



20083422

Operation Descriptions

GENERAL

The LM27262 is a selectable 2-, 3-, or 4-phase step down switching regulator controller. It's a fixed-frequency, voltage-mode control PWM with user programmable average current modulation of the reference voltage. This approach imparts a pseudo current mode behavior to the control loop as well as load line shaping for improved dynamic performance. The individual phase currents are continuously monitored and the duty cycles of each phase are adjusted as necessary so that the phase currents are all kept equal. The MOSFET drivers are contained in separate driver chips. This offers several advantages. From a cost standpoint, the largest amount of die area in most controllers is used for the drivers. As such, with external drivers, only the required drivers for a given design need be purchased. From an electrical standpoint, the drivers produce large pulse currents that tend to disturb the analog circuitry close by, particularly within the controller. By moving the drivers off chip, these pulse currents can be localized to the drivers themselves. PCB layout is also simplified since the drivers will not need long, hi di/dt traces. The drivers can be located very close to their respective MOSFETs. This is especially advantageous in a multi–phase design that, by it's nature, occupies a fair amount of board real estate. Shorter gate drive runs will also help minimize radiated emissions from the power supply. The result is much better-behaved control circuitry and less likelihood of needing several PCB iterations to optimize the circuit's performance.

CURRENT BALANCING CIRCUIT

In order to ensure current balance between phases, the LM27262 measures the instantaneous load current for the "on" phase and forces this current to be equal to the average of all the active phase currents.

Refer to *Figure 3*. Only two phases are shown for simplicity. The circuitry in *Figure 3* is duplicated on the other two phases of a 4-phase design. The VIL pins connect to the output side of the current sense resistors, while the VIH pins connect to the inductor side of the sense resistors. All of the VIL signals are summed through the internal 10kΩ resistors so that the difference between the signals VILAVG and VIHAVG represents the average value of all the corresponding sense voltages.

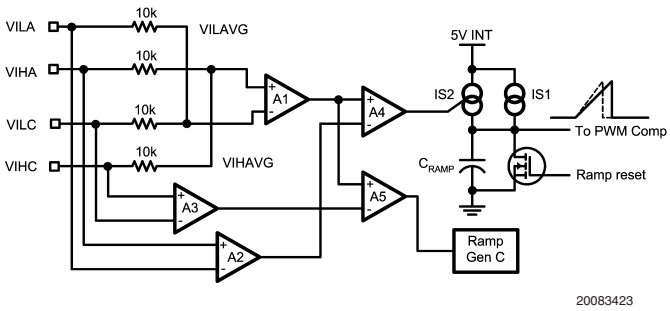


FIGURE 3. Current Balancing Circuit

Amplifier A1 converts the difference, VIHAVG-VILAVG, to a ground-referenced signal, which represents the instantaneous average current per phase. Amplifier A2 converts the instantaneous current information for phase A from a differential to a ground referenced signal. Amplifier A4 acts as an error amplifier, the output of which drives an adjustable current source, I2. Current source I1 provides a continuous current for charging the internal ramp capacitor, C_{RAMP}, while I2 makes slight adjustments to this charging current. The resulting ramp voltage is ultimately compared to the voltage loop's error amplifier output to control the regulator's pulse width. When the PWM comparator trips, it also turns on the ramp generator's reset transistor and dumps the ramp capacitor. Amplifiers A3 and A5 perform the same function for Phase C by controlling an identical ramp generator. In summary, the slope of the PWM generator's ramp signal is adjusted as required to keep the phase currents balanced. For instance, if the phase A current is a bit too high compared to the average phase current, the slope of the PWM ramp for this phase is increased slightly. This tends to turn the phase off a bit early and reduce its output current.

UNDER VOLTAGE LOCK OUT (UVLO)

The 5V supply input has a UVLO function with hysteresis, assuring stable, predictable start-up performance.

POWER GOOD FUNCTION

The PWRGD window is -12% to +230mV (typical) of the programmed output voltage. The PWRGD function is masked during VID transitions to prevent false power fail indications. Masking time is guaranteed to be at least 100usec over the full temperature range.

INTEL SpeedStep™ TECHNOLOGY

The LM27262 supports IST. See also respective Intel specs. IST or Geyserville-III operation is a real-time dynamic switching of the CPU core voltage and frequency between multiple performance modes.

DAC ACCURACY and V_{REF} SELECTION

The LM27262's internal voltage reference is nominally 1.235V. Accuracy is ±0.9% or better at room temperature. Due to the required precision of the VRD-10 specification, the LM27262 was designed with the ability to use an external precision reference. Since National Semiconductor's precision 0.2% accurate voltage references have a 1.225V typical output voltage, the LM27262 has a 10mV internal offset switched in when REFINT selects an external reference. This allows compensating for the 10mV difference between the internal and external references. The LM27201 is the recommended external reference for use with the LM27262.

STANDARD VID CODE OFFSET

Intel's VRD-10 specification requires a "Standard Offset". This offset is typically 25mV but is subject to change with future specification revisions. As such, the LM27262 has an externally programmable offset. A resistor from the I_{REF} pin to ground programs a precision current thru a resistor connected between VPROG and VSTDOS pins. The recommended nominal current value is 80µA. The IREF pin forces 1.4V across the current programming resistor. The IREF programming resistor value is therefore: R = 1.4V / 80µA = 17.4kΩ.

The VPROG output is a buffered version of the internal DAC output. The voltage drop between this pin and the VSTDOS pin is equal to the IREF current times the value of the offset resistor. For a 25mV offset and R_{IREF} equal to 17.4kΩ, the offset resistor should be 309Ω. The error from using standard 1% resistor values is as follows: The source current can

Operation Descriptions (Continued)

be recalculated as 1.4V / 1.74kΩ = 80.46mA. Using a standard 309Ω, 1% value for the offset resistor produces a nominal offset voltage of 24.86mV for an error of 0.14mV.

LOAD LINE SLOPE

The Load Line Slope (LLS) is commonly known as Adaptive Voltage Positioning (AVP). In the LM27262 the AVP is implemented as "active voltage positioning". Active voltage positioning synthesizes the load line actively so as to limit power dissipation. In a typical four-phase application using 2 mΩ sense resistors, the effective impedance due to the resistors is only 0.5 mΩ. Yet with active voltage positioning an effective 1.3 mΩ impedance is synthesized with no additional losses. If implemented in a purely passive manner, nearly three times the losses would be incurred.

For an LM27262 application the LLS can be calculated as follows:

Slope = 3.818 x RSENSE x R2/(R7+R2); where 3.818 is a function of the gain of the LM27262's internal load line circuit; Slope and RSENSE are measured in mΩ. Referring to the typical application circuit, the total resistance of the R7+R2 resistor divider should be about 5.5kΩ. For a slope of −1.3 mΩ and 2 mΩ current sense resistors the 1% standard resistor values calculate as R7=4.75kΩ and R2=976Ω. The LM27262 will automatically compensate if the number of active phases is reduced to either two or three.

OUTPUT OVER-CURRENT PROTECTION (OCP) and PROGRAMMABLE CURRENT LIMIT

The LM27262 has a genuine OCP feature based on actual load current measurement as a voltage drop across the current sense resistors. Unlike some other OCP techniques, such as a short-circuit protection based on detection of an under-voltage condition, this true current limit approach allows a system designer to use power train components that are not significantly over designed. There is also a time delayed latch off feature that will be discussed later to further protect the regulator from sever overload conditions. The LM27262 has a CLIMADJ input that allows the voltage regulator designer to set the current limit threshold via a simple resistor divider. Refer to *Figure 4* below. The current limit is programmed for each phase. For instance, for a 44A current limit in a 2-phase application program 22A per phase; for 44A current limit in a 4-phase application, program 11A per phase. In the latter case, the programming resistor R1 should be smaller. The current limit threshold will change somewhat as a function of input voltage and die temperature, reducing somewhat at higher input line voltages and temperatures. This is due largely to changes in inductor ripple current. Therefore, current limiting should be tested at the highest input voltage and operating temperature likely to be encountered in a particular application. Some empirical adjustment of the current limit program resistors may be necessary.

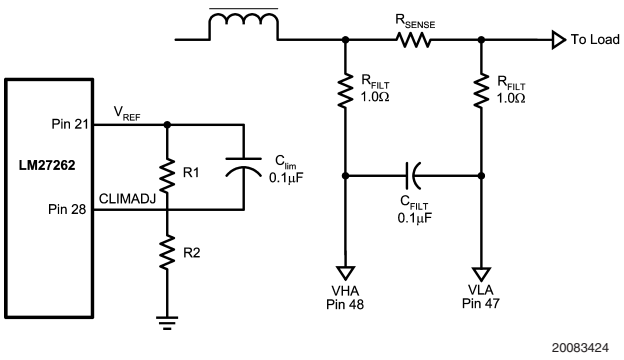


FIGURE 4. Current Sense Filtering

Total resistance of R1+R2 resistor divider should be approximately 50kΩ ±10%. Lower values will tend to overload the VREF output while higher values may increase the OCP threshold error due to variations in CLIMADJ pin input bias current.

To calculate the divider values assuming a total divider resistance of 50kΩ:

$V_{R1} = V_{RS} / 0.48$

$R1 = V_{R1} \times 50k\Omega / V_{REF}$

$R2 = R1 \times (V_{REF} - V_{R1}) / V_{R1}$

A 0.1µF filter capacitor should be connected across R1 for reducing switching noise pickup.

Careful connection to the current sense resistors is crucial for OCP threshold accuracy. Always use Kelvin connections to low value sense resistors in order to minimize the effects of trace resistance. With only a couple of µΩs of sense resistance, a few hundred µΩs of trace resistance will result in significant measurement errors. The connections to all sense resistors should be as close to physically identical as possible to ensure good phase-to-phase matching.

Generally, the worst-case low limit for the OCP threshold should be set at least 10% to 15% above the maximum desired continuous load current. The voltage across the current sense resistors at the onset of current limit is approximately 48% of the voltage between the CLIMADJ pin and Vref. Keep in mind that the current limit is pulse by pulse, so the peak inductor current needs to be calculated to determine the actual current limit trip point.

In order to avoid noisy current sense measurements, it is usually desirable to add small RC filters at the current sense inputs (see *Figure 4*). Typical values are on the order of 1Ω and 0.1µF. These filters will slow down the current limit circuit's response time a bit and increase the actual current limit relative to the theoretically expected value. The 48% scale factor mentioned above includes an empirical adjustment for this. It will be necessary to verify the final value experimentally.

SOFT START, VIDPGD DELAY and TURN-ON TIME

The soft-start feature minimizes inrush current and prevents output voltage overshoot. The SOFTCAP pin has an internal current source of approximately 3.2µA that charges a programming soft-start/soft-stop capacitor. There is an approximately 2msec built-in delay between the time that VRON is asserted and the SOFTCAP starts charging. This allows the VID code to settle before the switching regulator turns on. The soft-start ramp time can be calculated using the following formula:

Operation Descriptions (Continued)

$T_{SOFTSTART-RAMP} = (V_{CORE}/I_{SOFTCAP})C_{SOFTCAP}$;

$T_{VIDPGD} = T_{SOFTSTART-RAMP}$ x 0.5V/V_{CORE};

$T_{TURN-ON} = T_{VIDPGD} + (V_{CORE}/I_{SOFTCAP})C_{SOFTCAP}$; where $I_{SOFTCAP}$ = 3.2µA and Volt, Amp and Farad units are used.

For example:

If $T_{SOFTSTART-RAMP} \cong$ 5 msec for V_{CORE} = 1.55V and Css = 10nF then $T_{VIDPGD} \cong$ 1.6 msec and $T_{TURN-ON}$ = 6.6 msec. If $T_{SOFTSTART-RAMP} \cong$ 3.6 msec for V_{CORE} = 1.15V and Css = 10nF then $T_{VIDPGD} \cong$ 1.6 msec and $T_{TURN-ON}$ = 5.2 msec

SOFT STOP

The soft-stop feature forces a well-controlled power off transition. The output voltage ramps down smoothly, eliminating the possibility of a large negative voltage at the output. This feature eliminates the large need for a Schottky protection diode or a clamp transistor at the load.

The LM27262 has an internal 50kΩ resistor connected to the SOFTCAP pin that discharges the SOFTCAP capacitor. The soft-stop ramp-down time is approx. 9msec with a 33nF capacitor, or approximately 5 x RC, where R is 50kΩ, and C is the soft-start capacitor.

VID-CODE CONTROLLED V_{CORE} TRANSITIONS

The VID transition slew rate is set by an external resistor connected between the VIDSLEW and SOFTCAP pins. This permits an additional level of slew rate control beyond that provided by the soft-start function.

UVP, OVP and OCP SHUTDOWN PROGRAMMABLE Delay

If PWRGD is de-asserted for any reason, the voltage regulator can disable its output and latch itself off. Different systems can tolerate various fault conditions for different time durations. A programmable delay feature enables the system designer to chose how long the supply will wait following the detection of an OVP or UVP event prior to shutting down. By adding a capacitor to the DELAY pin, pin 34, the latching of fault events can be delayed. If the DELAY pin is grounded, latch off is defeated entirely. The following formula should be used for calculating a programming capacitor value:

CDELAY = TDELAY x 12.5µA/1.4V or

TDELAY/112kΩ where C is in Farads, 1.4V is the

"DELAY Threshold Voltage", and 12.5µA is the

"DELAY Charge Current". For example,

CDELAY = 0.22µF programs a 25ms delay.

Grounding the DELAY pin will disable the latch off function. This can be most helpful during system de-bug or if the latch-off feature is not desired for some reason.

2-, 3- or 4-PHASE OPERATION

2-, 3- or 4-phase operation is user selectable. For lower current designs it may be desirable to use fewer than 4 phases.

LOGIC INPUTS and OUTPUTS - GENERAL

All logic control inputs have hysteresis that increases noise immunity and, particularly for the VRON signal, enables a designer to turn the LM27262 on from a 3.3V rail via an external RC-delay circuit. Note that the logic outputs are not short circuit protected and must not be short-circuited to either power rails or ground.

LOOP COMPENSATION

An RC network connected between the VFB and VCOMP pins compensates the feedback loop's gain/phase characteristics. These two pins are respectively, the input and output of the error amplifier. Feedback loops such as these are best compensated through the use of an empirical approach. The best approach is to measure the control to output transfer function and then design an appropriate error amplifier compensation.

Component Selection

POWER PATH COMPONENT SELECTION

The choice of power path components is critical to achieving a properly behaved regulator. Design considerations usually include such things as efficiency, transient response, output ripple, size and cost. The process tends to be somewhat iterative while converging on a workable design.

The first decision that must be made is the number of phases to use. The maximum load current that the design must deliver usually dictates this. With the power devices available at the time of this writing, the practical upper limit is about 20 to 25 amps per phase. Trying to run higher per phase load currents results in thermal problems as well as the inability to maintain an all surface-mount design. In some instances, it is possible to pull higher phase currents if the peak's duration is relatively short and the average current is well below peak. Another possible criteria for selecting the number of phases is to capitalize on the ripple current cancellation effects of multiphase designs. In theory, at a V_{IN} to V_{OUT} ratio equal to the number of phases, the input and output ripple currents approach zero. If the design will run close to this "sweet spot" it may influence the number of phases selected. For instance, adding a phase may prove most advantageous.

One's initial reaction to increased phase count is that the solution becomes much more costly. But this assumption isn't always correct. In theory, the total energy stored in the output inductors decreases as phases are added. This is due in part to the ripple cancellation effects and in part to the energy storage being a function of the square of the inductor currents. So for equal inductor values in a two-phase design, the energy stored is only 50% that of a single phase design. In practice, for equal output ripple, the inductance in each phase of a 2-phase design could be about ½ that of a comparable single phase design. Therefore, energy storage per inductor is only 25% that of a one phase design. So, although there may be two inductors in the 2-phase design, they are each much smaller, lighter and hopefully lower cost, than the comparable single-phase solution. As for MOSFET selection, since the total current being switched is the same regardless the number of phases, in theory, the total Rds(on) required is the same as well. It just gets split into more packages in the multi-phase design. Some difficult to characterize advantages of a higher phase count relate to MOSFET parasitics. For instance, the body diode reverse recovery effects of the low side switch adversely effect the switching loses in a buck regulator. Larger FETs for both the low side and high side switches will have much greater losses than smaller devices switching lower currents. Spurious turn-on of the low side FET due to its Miller capacitance is also less problematic in smaller devices. The result is that in many cases, the higher phase count design will prove to be somewhat more efficient than a lower phase count design that can provide comparable full load current.

Component Selection (Continued)

Since VRD-10 designs must support large load transients while maintaining very tight output regulation, a good place to start the design is the output capacitors.

OUTPUT CAPACITOR SELECTION

For designs that will be subjected to large load current transients, the output capacitor array is probably the best place to start. It is assumed that the full amplitude of the load current step will be drawn from the output capacitors for a short time. As such, there will be a significant droop in the output voltage that's a function of the step size and the output capacitor's impedance. The output voltage step will have three basic components. The first is a more or less vertical edge equal to the ESR (Equivalent Series Resistance) of the output caps multiplied by the load step amplitude or ΔI x ESR. There's also a component equal to the ESL (Equivalent Series Inductance) multiplied by the rate of change of the load current, (ΔI/Δt) x ESL. The ESL induced spike is usually small in value and short lived, assuming a clean board layout with good high frequency decoupling, and can usually be ignored. In sizing the output capacitors, a good starting point is to assume that the ESR step will be 20% to 50% of the allotted transient voltage spec. The low end of the range will apply to ceramic capacitors and the high end of the range to tantalum or aluminum electrolytic devices. The remainder of the tolerance can be allocated to the output capacitor's droop voltage. The droop rate, ΔV/Δt, is equal to I_{STEP}/C_{OUT}, where Istep is the amplitude of the load transient. The total droop amplitude is equal to ΔV/Δt multiplied by the time it takes for the regulator to get the output voltage slewing in the opposite direction. See *Figure 5* for details.

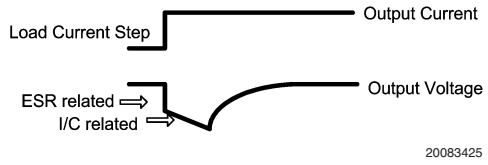


FIGURE 5. Output Transient Response

In a design with voltage positioning, the ideal ESR of the output capacitor array should be less than or equal to the load line slope. So for a VRD-10 design we should assume 1.5mΩ for the output capacitor ESR.

In a four-phase design, it's likely that the latency prior to getting a high-side switch turned on is approximately 1/4 of a full cycle. An estimate of about twice that, or around 1.5µs, is a good place to start for making the droop calculation. As an example, assume a 50 amp load step and a tolerance of 85mV with high performance polymer capacitors: Using a 390µF, 5mΩ capacitor, the design requires a minimum of 4 in parallel to meet the ESR estimate. The droop in 1.5µs would be:

$$\text{Droop} = 1.5\mu s \times 50A/1560\mu F = 48mV$$

Add this to the 75mV ESR droop and we can see the spec is not met. Therefore several additional capacitors must be added. Rerunning the numbers with 6 capacitors we get:

$$\text{Droop} = 1.5\mu s \times 50A/2340\mu F = 32mV$$

Plus an ESR step of 50A x 0.833mΩ + 32mV = 73.6mV

In general, it will be necessary to add high frequency decoupling as well as the bulk capacitance calculated above. An array of at least 20, 22µF, 1206 case ceramics is recommended. They should be as close to the CPU as possible.

With the output capacitors chosen, an upper bound can be established for the inductor value:

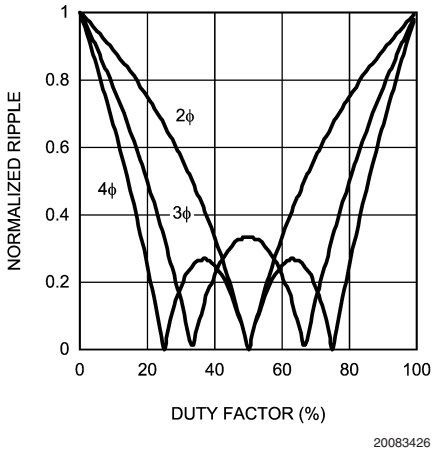


FIGURE 6. Normalized Pk-Pk Output Ripple As A Function Of Duty Factor and Number Of Phases

$$L < C_{OUT} \times (V_{IN\ (MIN)} - V_{OUT(MAX)}) \times ESR / \Delta I_{OUT}$$

This value inductor should be installed in each phase. Larger inductor values will result in a delay in the output voltage recovery to a load step. Smaller values will store less energy (lower cost) but will increase the output ripple. Since the peak switch currents will also be higher, the efficiency is likely to suffer somewhat with smaller inductors.

Assuming a minimum input voltage of 12V and 1.5V out with a 50A load step and the capacitors selected above,

$$L < 2340\mu F \times (12V - 1.5V) \times 0.833\ m\Omega/50A$$

$$L < 0.41\ \mu H$$

Something around 0.5µH will be the closest standard value and should prove adequate. Since this value is slightly greater than desired, dynamic performance will suffer slightly.

If this value will yield excessive ripple current at maximum input voltage (greater than about 40% of the single phase DC current), then a larger inductor should be considered and therefore, optimal dynamic performance will not be obtained. The tradeoff is typically efficiency vs. dynamic performance.

During a load-off transition, the extra energy stored in the inductors will end up in the output capacitors. This magnetic energy, $LI^2/2$, will be stored in the output capacitors as $CV^2/2$. The energy already in the output capacitor prior to the transient, and that left in the inductor after the event, must also be accounted for.

Therefore:

$$V_{MAX} = [(n \times L/C) \times ((I_{MAX}/n)^2 - (I_{MIN}/n)^2) + V_{init}^2]^{1/2}$$

Where V_{MAX} is the peak output voltage, n is the number of phases, I_{MAX} is the high load current , I_{MIN} is the low load current, C is the output capacitance, L is the per phase inductor value, and V_{init} is the output voltage prior to the load dump.

From our example assuming a 70A max load and a 50A step:

$$V_{MAX} = (4 \times 0.50\mu H \times ((70A / 4)^2 - 20 / 4)^2) / 2340\mu F + 1.4452)^{1/2}$$

Component Selection (Continued)

V_{MAX} = 1.526V

There will also be an initial step equal to ΔI_{OUT} x ESR, which in our example will be approximately 41mV. The two effects are not entirely additive since the voltage across the ESR is decreasing as the capacitor gets charged. Therefore, the actual peak voltage will be somewhat less than the 1.567V that simple addition would predict. In general, it's a good idea to provide pads for a couple of extra capacitors on the layout in case a little extra decoupling proves necessary.

The output ripple currents of multiphase regulators tend to cancel to some degree. This greatly reduces the demand on the output capacitors. *Figure 6* allows a simple estimate to be made of the total output ripple current based on the number of phases and the nominal duty cycle. Simply pick the worst case (highest ripple) operating point off the curve and multiply by the single channel pk-pk ripple current. The expected pk-pk output ripple voltage will be approximately:

Vrip = Irip x ESR

This simplified equation ignores the reactive term of the capacitor's impedance. With any kind of electrolytic capacitor it's generally safe to ignore the capacitive reactance term since it will prove to be negligible compared to the ESR.

CALCULATING THE INDUCTOR RIPPLE CURRENT

The LM27262 operates at a switching frequency of 300kHz per phase. The high side switch on time is therefore the period, 3.33µs, multiplied the duty factor, V_{OUT}/V_{IN}. During this time the inductor is connected between the input and the output, so inductor current ramps positive during this time. The peak-peak ripple current ΔI is approximately equal to:

$$\Delta I = 3.3\mu s \times (V_{OUT} - V_{OUT}^2 / V_{IN}) / L$$

Continuing our example and assuming a maximum input of 12V:

$$\Delta I = 3.3\mu s \times (1.5V - 1.5V^2 / 12V) / 0.50\mu H$$

$$\Delta I = 8.66A$$

$$I_{IN} = 1.5A$$

With a maximum phase current of 17.5A this is a bit higher than desired so a little larger inductor value may be in order. Assuming a 35% ripple current and 17.5A/phase:

$$L = 3.3\mu s \times (1.5V - 1.5V^2 / 12V) / 6.125$$

$$L = 0.71\mu H$$

If the larger value of inductor is used, it may be necessary to go back and recalculate some of the early assumptions.

The peak current seen by the inductors will be the maximum DC current plus one half of the ripple current. The maximum DC current should be assumed to be approximately 10% to 15% greater than the maximum anticipated load current to allow for short circuit current. The inductors must not hard saturate in a fault. Again from our example, 110% of 17.5A plus one half of the 6.125A peak-peak ripple current yields a peak inductor current of 22.3A. There will usually be two current ratings associated with an inductor. One is the average current rating and the second is the saturation current. Only the saturation current need be considered for short circuit limiting. The sustained DC current is the 110% of 17.5A or roughly 19A in this example. If over current latch off is employed, only the 17.5A steady state current need be considered since the inductor's steady state current rating is basically a thermal limitation.

MOSFET SELECTION

The choice of power FETs is driven primarily by efficiency or thermal considerations. There are two main loss components to consider, conduction losses and switching losses. The switching losses are primarily due to parasitics in the FETs and are very hard to estimate with any degree of accuracy. The conduction losses are much easier to characterize. The switching losses in the low-side FET are very low since it's essentially a zero-voltage switched device. However, the high-side device's switching losses are usually larger than its conduction losses. The primary contributor to high-side FET switching losses is related to the reverse recovery characteristics of the low-side FET's body diode. During the small dead band where both FETs are off every cycle, the low-side FET's body diode will carry the inductor current. The problem is that the body diode exhibits a significant reverse recovery time, trr. During this time, the FET looks like a short circuit. When the high-side FET is subsequently turned on, there is a shoot through path from the input supply to ground. A larger high-side FET will tend to exhibit a larger shoot through current. Therefore, it is undesirable to oversize the high-side device. Since the low-side device looks like a short, the entire supply voltage is impressed across the high–side device, along with a simultaneous high current. The result is very high momentary power dissipation. The total power lost is a direct function of the switching frequency.

As a starting point, assume that about ½ of the switcher's total losses will take place in the MOSFETs. If from our prior example, we assume a desired 90% efficiency at full load, the FET losses are therefore 5% of the full output power or 5.25W. Since we have four phases, that works out to 1.31W/phase. This is divided between the upper and lower FETs. Since the step down ratio is large, the low side FETs will be on for most of the period. The low-side FET conduction loss is I^2 x Rds(on) * (1-DF), where DF is the duty factor, V_{OUT}/V_{IN}. The worst-case dissipation occurs at high input line voltage. We've assumed 12V for our example. Allowing 50% of the total FET loss to the low-side switch gives us a dissipation of 0.66W x Rds(on) . This will usually result in a conservative design. Solving for Rds(on) :

$$Rds(on) = P_{dis}/(I^2 \times (1- V_{OUT}/V_{IN}))\ Rds(on) = 0.65W/(17 \times 5A^2 \times (1-1.5V/12V))$$

$$Rds(on) = 2.4m\Omega$$

A pair of Si7356 MOSFETs in parallel is very close to this. These are trench devices with excellent thermal characteristics as well.

The high-side FET on-resistance is calculated similarly, but allow one half of the dissipation to switching losses. Therefore the allowable conduction loss is approximately 0.325W.

$$Rds(on) = Pdis/(I2 \times (V_{OUT}/V_{IN}))$$

$$Rds(on) = 0.325W/(17x\ 5A^2 \times 1.5/12V))$$

$$Rds(on) = 8.5m\Omega$$

A pair of Si7392 FETs will meet this requirement.

GATE DRIVE RTEQUIREMENTS

Energy for the high side gate drives is stored in the boost capacitors, which in turn are powered by the 5V supply. The charge stored in each boost capacitor should be between 10 times and 20 times the Qg specified for the high-side FETs. For the example given, the specified maximum Qg is 15nC. There will be two of these devices in parallel so the combined gate charge is 30nC. Therefore, the charge stored on the boost capacitor should be a minimum of 300nC.

Component Selection (Continued)

Since Q = C x V and the capacitor will be charged to 5V, the minimum capacitance required is 0.06µF. A 0.1µF would be a good choice. In some instances, it's desirable to add small resistors between the bootstrap capacitors and the CBOOT pins of the drivers. This allows the high-side FET's turn-on to be slowed down a bit to minimize shoot through currents associated with the low–side FET's body diode reverse recovery time. This technique avoids slowing the high-side FET's turn off transition. A value of 1.0 to 5.0 ohms is usually adequate.

INPUT CAPACITOR SELECTION

The input capacitors are required to deliver the difference between the average and instantaneous currents to the regulator in an effort to control EMI at the input. In sensitive applications, a small inductor (typically only a few hundred nanoHenries) should be placed in the line between the input source and the input capacitors. This is not usually necessary in battery powered devices due to the low impedance of the power path and the relative insensitivity of the battery rail to the regulator's switching noise. The most critical specification for the input capacitors is their ripple current capability. In a multiphase regulator, there is a significant amount of input ripple current cancellation, hence a much lower input capacitor requirement than a comparable single-phase design. *Figure 7* shows the normalized input ripple current for a given number of phases and duty factor. The inductor ripple current is assumed to be 30% of full load current for this analysis. The ripple current percentage only affects the depth of the cusps in the curves. Be sure to examine the entire range of input voltage to determine the worst-case (maximum) ripple current. Multiply the full load output current by the factor obtained from *Figure 7* to determine the RMS input ripple current.

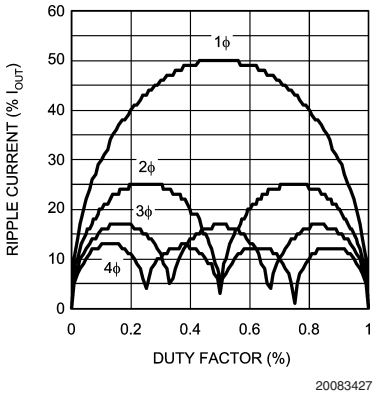


FIGURE 7. RMS Input Ripple as a Percentage of DC Outpout Current vs Duty Factor and Number of Phases

There should be at least one bulk input capacitor across the power FETs of each stage. If the ripple current calculation indicates that more capacitors than this minimum number are required, they should be distributed evenly across the input voltage power plane. The plane that interconnects the phase inputs should be as large as possible in an effort to ensure good current sharing between the input capacitors. Be sure and install a good quality ceramic capacitor across each phase's FETs for high frequency bypass.

Layout Considerations

Proper PCB layout is critical to having a high current DC-DC converter work correctly. The most important part of the layout is the power path. Start with the large, high current parts and lay them out in a logical power flow. Avoid using internal layers as the primary high current paths. It's best to connect power devices together directly with copper on the same layer the parts are to be mounted on. Avoid vias as the primary conductor in the high current paths. Inner layer copper can be used in parallel with top-side copper to good advantage. The vias that connect the layers should be allowed to solder fill. Small vias (10mil dia. or less), should be limited to approximately 1A, while those with internal diameters of 20mils or more may be able to handle 2A or a little more. In general, adding more vias between layers is better than fewer.

Once all of the power parts are placed and routed, the control IC can be placed and connected. Since the LM27262 uses external drivers, there are no large pulse currents in either V_{CC} or the ground connection. This allows the chip ground to be remotely connected to the load's local ground sense point. Keep this connection under a couple of inches in length and be sure it's a wide trace (0.05 in or more). Avoid locating the controller between the power switches and the load. This minimizes ground drops between the load and the controller. If the controller is located on the side opposite the CPU from the power stage, there will be essentially no DC drop across the area of ground plane between the CPU and the controller.

There should be a good quality ceramic bypass capacitor placed very close to the IC's V_{CC} and ground pins and connected with very short traces. All of the low level analog signals associated with the controller should be referenced back to the IC's local ground connection at Pin 23. A single point ground should be established at that pin. Run a ground trace to such things as the Softstart cap ground, Ilim divider and external reference if used, from the primary ground pin. The loop compensation components should be located as close to pins 34 and 35 as possible. Unlike a typical PWM controller, the voltage on the softstart capacitor is the actual reference voltage used by the error amplifier. As such, it is imperative that the SOFTCAP pin be kept as quite as possible. Again, the best approach is a dedicated analog ground, either in the form of a separate trace that daisy chains to all the grounded control components, or a small plane that connects to the main ground at the chip ground pin only.

Layout Considerations (Continued)

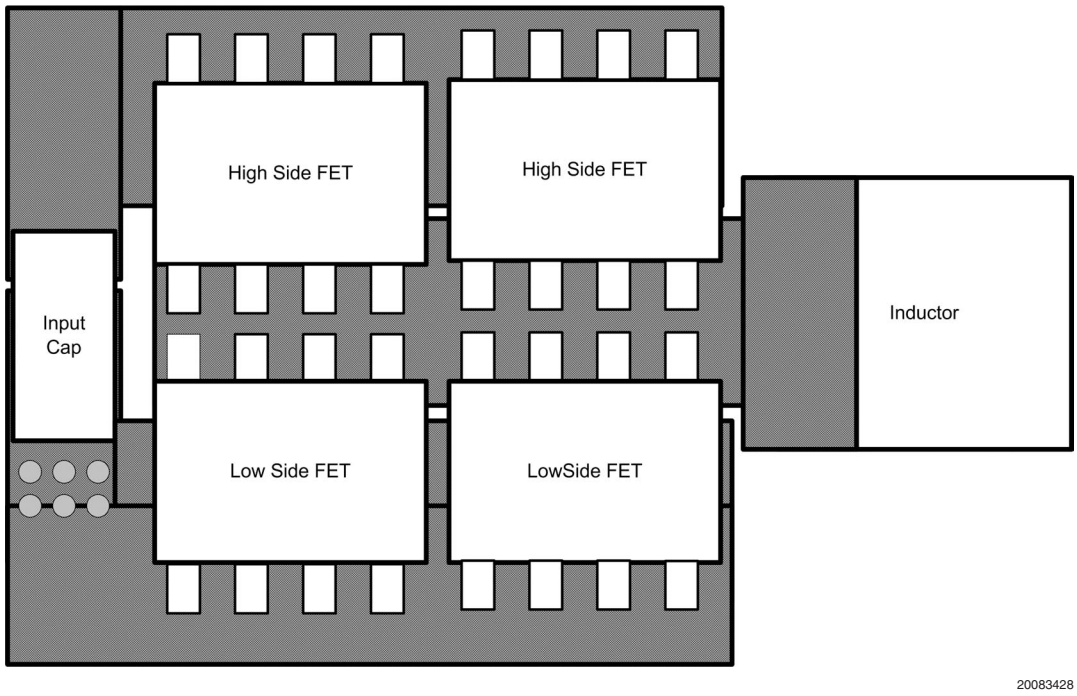
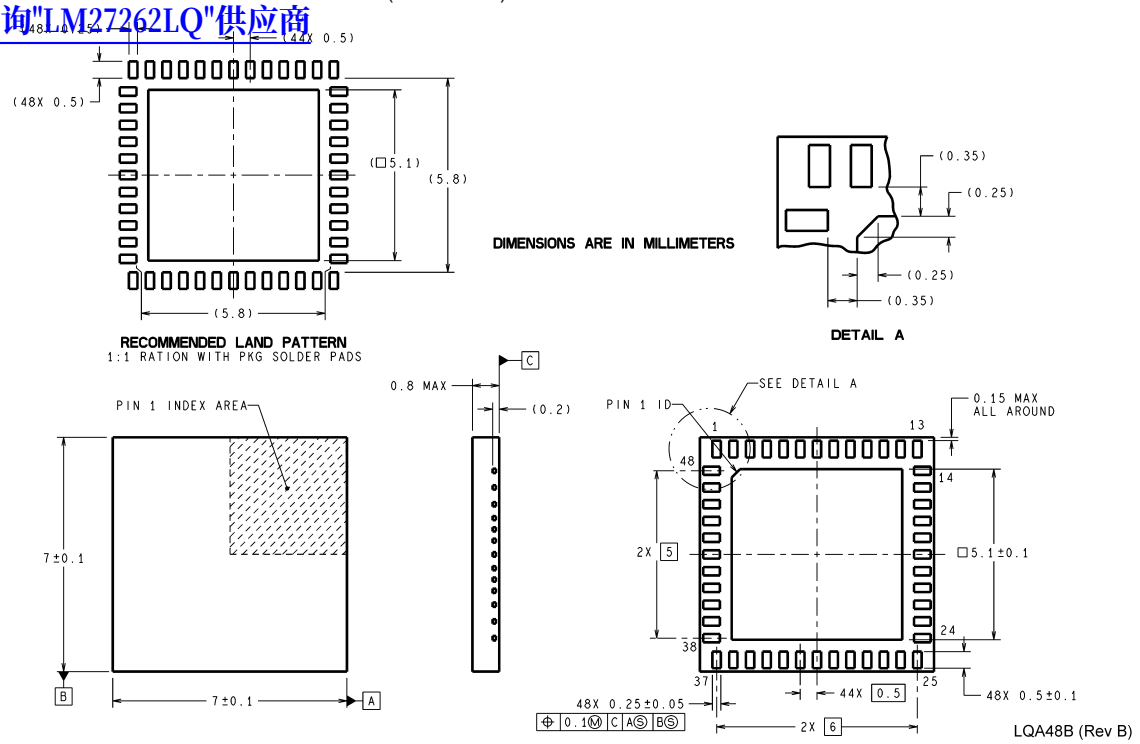
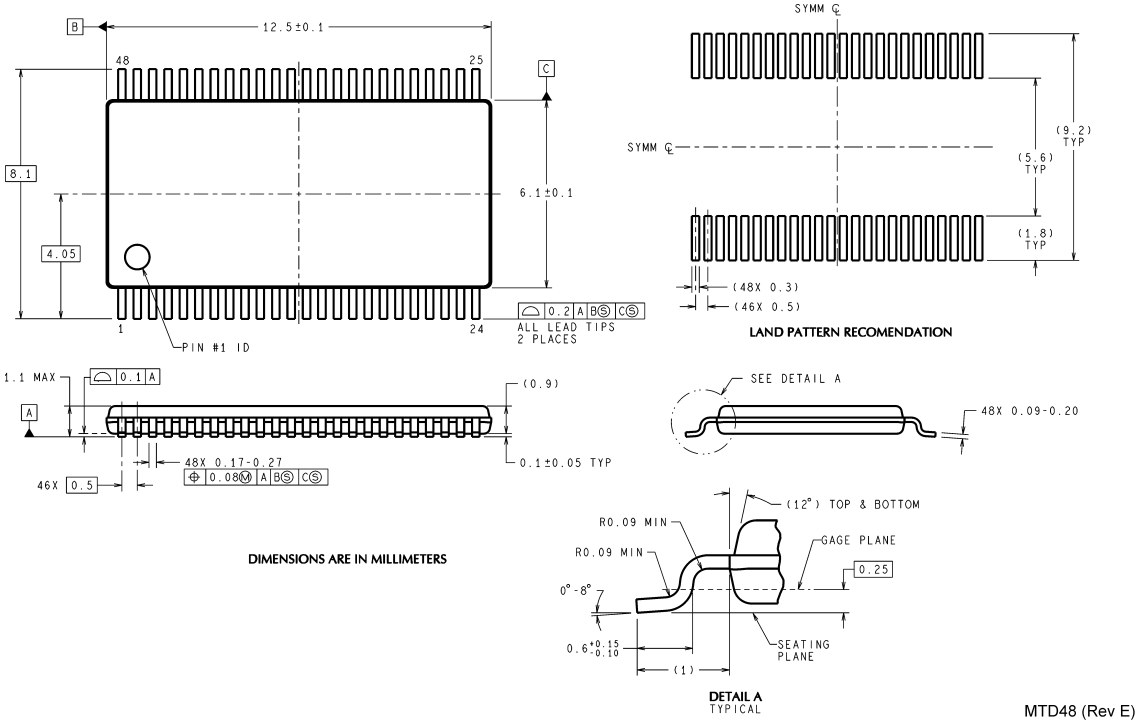


FIGURE 8. Power Path Layout

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead LLP Package
Order Number LM27262LQ
NS Package Number LQA48B



48-Lead TSSOP Package
Order Number LM27262MTD
NS Package Number MTD48

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