1.1 Scope.

This specification covers the detail requirements for a 12-bit monolithic CMOS multiplying digital-to-analog converter for use with 8-bit bus microprocessors. Data is loaded in two bytes, 8+4 (high/low byte), to input holding registers. The complete word is then transferred into the DAC register to update the DAC.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number[1]
–1	AD7548S(X)/883B
–2	AD7548T(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} (Pin 18) to DGND	+17V
V_{REF} (Pin 19) to AGND	±25V
V_{RFB} (Pin 20) to AGND	±25V
Digital Input Voltage (Pins 4–17) to DGND	−0.3V to V_{DD}
V_{PIN1}, to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-20 and E-20A
θ_{JA} = 120°C/W for Q-20 and E-20A

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Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +15V	Units
Resolution	RES	–1, 2	12					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits Over Temperature.	± LSB max
		–2	1/2	1	1/2	1/2		
Gain Error[2]	A_E	–1	6	6	6			± LSB max
		–2	3	6	3	3		
Gain Tempco	dA_E/dT	–1, 2	5					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2	0.02				ΔV_{DD} = ± 5%.	± %/% max
Output Leakage Current Pin 1	I_{OUT}	–1, 2	150	5	150		DAC Register Loaded with All 0's.	± nA max
Output Current Settling Time	t_{SL}	–1, 2	2				To ± 1/2LSB of Full Scale Range. I_{OUT} Load = 100Ω and 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error[3]	FTE	–1, 2	10				V_{REF} = ± 5V, 10kHz Sinewave. DAC Register Loaded with All 0's.	mV p-p max
Reference Input Resistance Pin 15	R_I	–1, 2	7	7	7			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	–1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	–1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	–1, 2	10	1	10		V_{IN} = 0V or V_{DD}.	± μA max
Digital Input Capacitance	C_I	–1, 2	7					pF max
Output Capacitance Pin 1	C_O	–1, 2	200				DAC Register Loaded with All 1's.	pF max
			100				DAC Register Loaded with All 0's.	
Supply Current from V_{DD}	I_{DD}	–1, 2	3	3	3		All Digital Inputs V_{IL} or V_{IH}.	mA max
			1	1	1		All Digital Inputs 0 or V_{DD}.	mA max
Data Valid Setup Time[4]	t_{DS}	–1, 2	230					ns min
Data Valid Hold Time[4]	t_{DH}	–1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$[4] to $\overline{WR}$ Setup Time	t_{CWS}	–1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$[4] to $\overline{WR}$ Hold Time	t_{CWH}[4]	–1, 2	25					ns min
$\overline{LDAC}$ to $\overline{WR}$ Setup Time[4]	t_{LWS}	–1, 2	50					ns min
$\overline{LDAC}$ to $\overline{WR}$ Hold Time[4]	t_{LWH}	–1, 2	25					ns min
Write Pulse Width[4]	t_{WR}	–1, 2	240					ns min

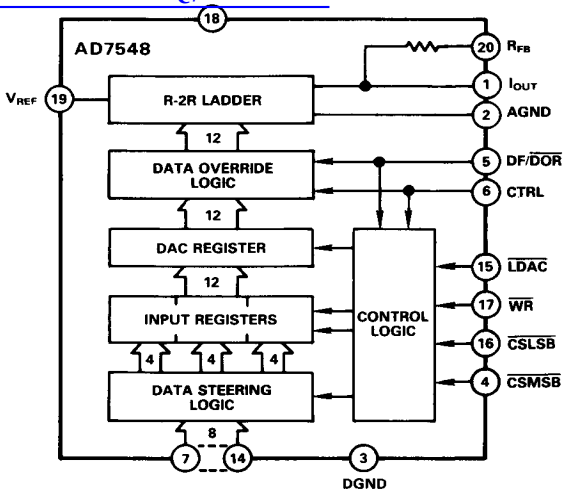
NOTES
[1]$V_{PIN1} = V_{PIN2} = 0V$, V_{REF} = +10V, unless otherwise noted.
[2]Measured using internal R_{FB} and includes effect of leakage current and gain TC.
[3]Feedthrough error can be reduced by connecting the metal lid to DGND.
[4]Timing per Figure 1.

Table 2.

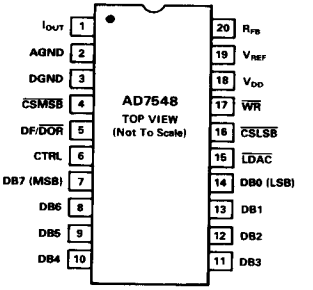
Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +5V	Units
Resolution	RES	–1, 2	12					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1	1	1	1		All Grades Guaranteed Monotonic to 12 Bits Over Temperature.	± LSB max
		–2	1/2	1	1/2	1/2		
Gain Error[2]	A_E	–1	6	6	6			± LSB max
		–2	3	6	3	3		
Gain Tempco	dA_E/dT	–1, 2	5					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2	0.02				ΔV_{DD} = ± 5%.	± %/% max
Output Leakage Current Pin 1	I_{OUT}	–1, 2	150	5	150		DAC Register Loaded with All 0's.	± nA max
Output Current Settling Time	t_{SL}	–1, 2	2				To ± 1/2LSB of Full Scale Range. I_{OUT} Load = 100Ω and 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	µs max
Feedthrough Error[3]	FTE	–1, 2	10				V_{REF} = ± 5V, 10kHz Sinewave. DAC Register Loaded with All 0's.	mV p-p max
Reference Input Resistance Pin 15	R_I	–1, 2	7	7	7			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	–1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	–1, 2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	–1, 2	10	1	10		V_{IN} = 0V or V_{DD}.	± µA max
Digital Input Capacitance	C_I	–1, 2	7					pF max
Output Capacitance Pin 1	C_O	–1, 2	200				DAC Register Loaded with All 1's.	pF max
			100				DAC Register Loaded with All 0's.	
Supply Current from V_{DD}	I_{DD}	–1, 2	2	2	2		All Digital Inputs V_{IL} or V_{IH}.	mA max
			300	300	300		All Digital Inputs 0 or V_{DD}.	µA max
Data Valid Setup Time[4]	t_{DS}	–1, 2	290					ns min
Data Valid Hold Time[4]	t_{DH}	–1, 2	70					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$[4] to $\overline{WR}$ Setup Time	t_{CWS}	–1, 2	50					ns min
$\overline{CSMSB}$ or $\overline{CSLSB}$[4] to $\overline{WR}$ Hold Time	t_{CWH}	–1, 2	25					ns min
$\overline{LDAC}$ to $\overline{WR}$ Setup Time[4]	t_{LWS}	–1, 2	50					ns min
$\overline{LDAC}$ to $\overline{WR}$ Hold Time[4]	t_{LWH}	–1, 2	25					ns min
Write Pulse Width[4]	t_{WR}	–1, 2	320					ns min

NOTES
[1] $V_{PIN1} = V_{PIN2} = 0V$; $V_{REF} = +10V$, unless otherwise stated.
[2] Measured using internal R_{FB} and includes effect of leakage current and gain TC.
[3] Feedthrough error can be reduced by connecting the metal lid to DGND.
[4] Timing per Figure 1.

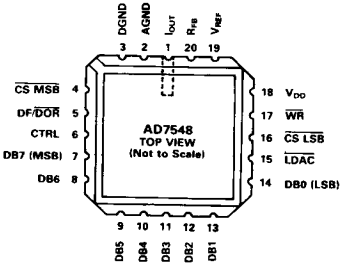
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package



E Package

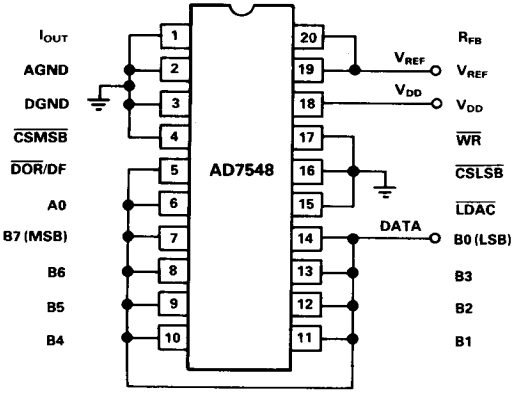


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



V_{DD} = +15V
DATA = V_{DD}
V_{REFB} = +10V

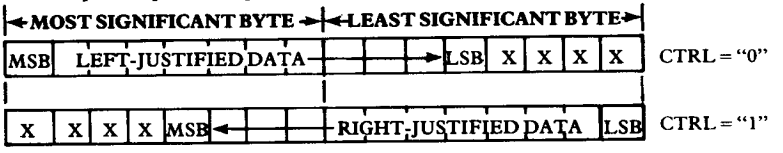
V_{DD} TURNS ON FIRST.

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	I_{OUT}	DAC current OUT bus. Normally terminated at virtual ground of output amplifier.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
5	DF/$\overline{DOR}$	Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held HIGH.

DF/$\overline{DOR}$	CTRL	FUNCTION
0	0	DAC register contents overridden by all 0's
0	1	DAC register contents overridden by all 1's
1	0	Left-justified input data selected
1	1	Right-justified input data selected

6	CTRL	Control Input. See pin 5 description.



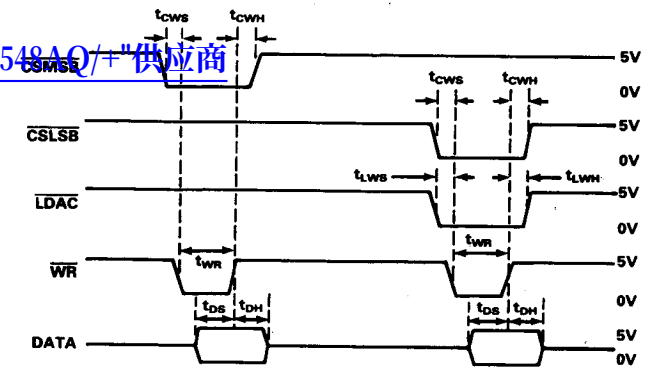
X = Don't care states.

7	DB7	Data Bit 7. Most Significant Bit (MSB).
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	Data Bit 0. Least Significant Bit (LSB).
15	$\overline{LDAC}$	Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
16	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
17	$\overline{WR}$	WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register.

Table 3.

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	FUNCTION
0	1	0	1	Load LS Byte to Input Register.
0	1	0	0	Load LS Byte to Input Register and DAC Register.
0	0	1	1	Load MS Byte to Input Register.
0	0	1	0	Load MS Byte to Input Register and DAC Register.
0	1	1	0	Load Input Register to DAC Register.
1	X	X	X	No Data Transfer

18	V_{DD}	+5V to +15V Supply Input.
19	V_{REF}	Reference Voltage Input.
20	R_{FB}	Feedback Resistor. Used for normal D/A conversion.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V.
   FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

Figure 1. Control Input Timing Diagram