

P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 12	0.022 at $V_{GS} = - 4.5$ V	- 8	26 nC
	0.028 at $V_{GS} = - 2.5$ V	- 8	
	0.036 at $V_{GS} = - 1.8$ V	- 8	

FEATURES

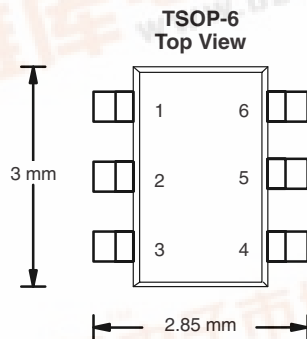
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch
- PA Switch



Marking Code

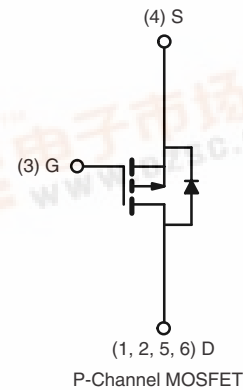
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Lot Traceability
and Date Code

Part # Code

Ordering Information: Si3473CDV-T1-E3 (Lead (Pb)-free)

Si3473CDV-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 12	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$ - 8 ^a	A
		$T_C = 70^\circ\text{C}$ - 8 ^a	
		$T_A = 25^\circ\text{C}$ - 8 ^{a, b, c}	
		$T_A = 70^\circ\text{C}$ - 6.5 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 20	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$ - 3.5	A
		$T_A = 25^\circ\text{C}$ - 1.67 ^{b, c}	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ 4.2	W
		$T_C = 70^\circ\text{C}$ 2.7	
		$T_A = 25^\circ\text{C}$ 2.0 ^{b, c}	
		$T_A = 70^\circ\text{C}$ 1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	55	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Foot (Drain)	R_{thJF}	25	30	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.d. Maximum under Steady State conditions is 110 $^\circ\text{C/W}$.

Si3473CDV

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**SPECIFICATIONS** $T_J = 25^\circ\text{C}$, unless otherwise noted

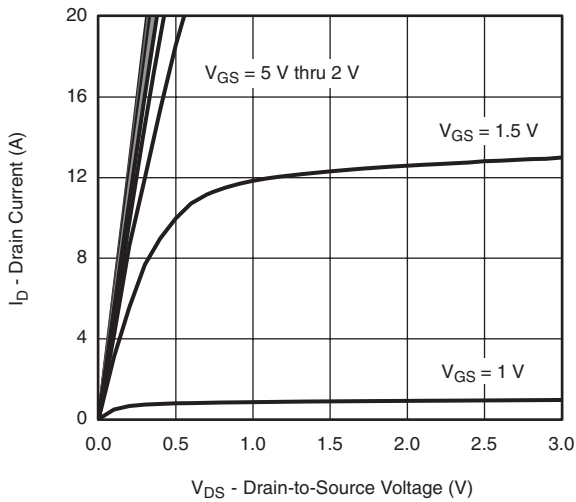
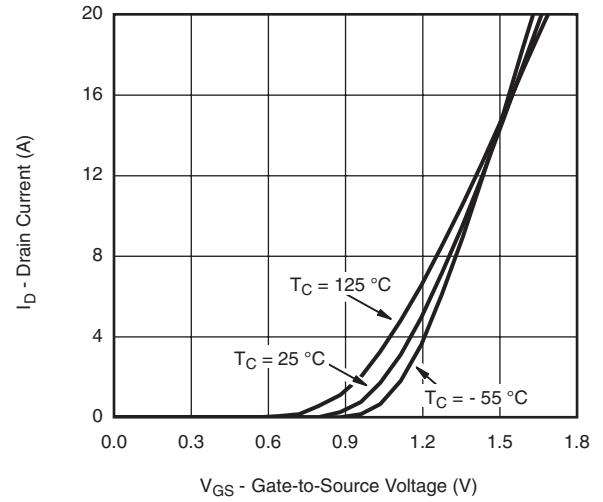
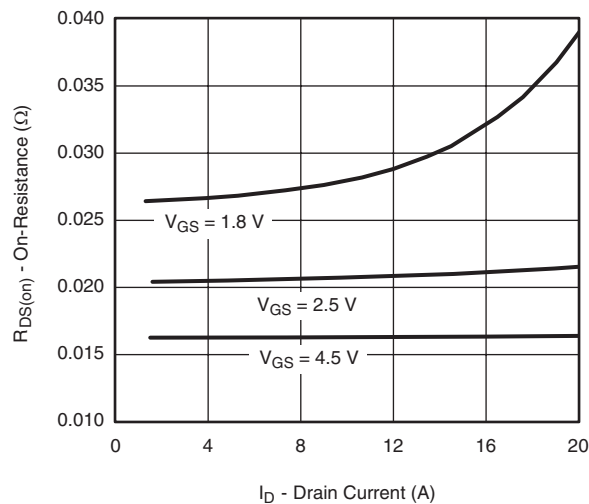
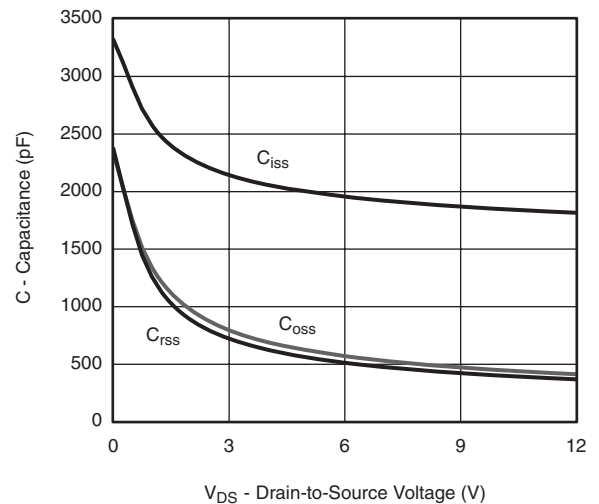
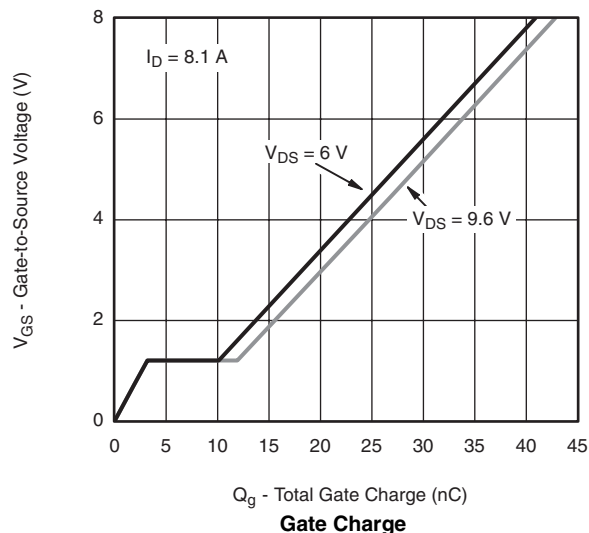
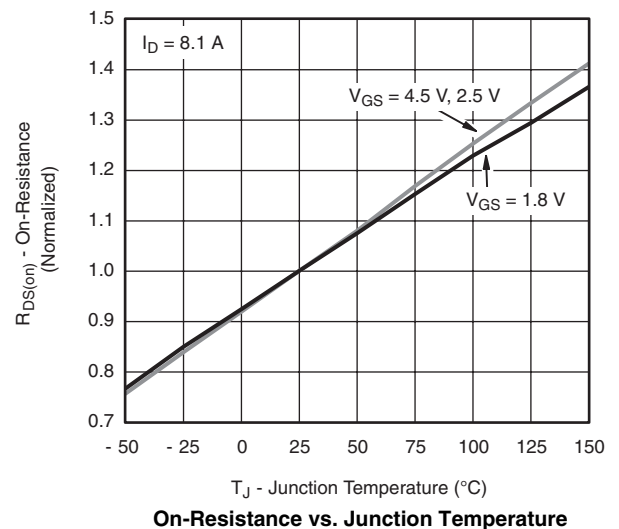
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 12			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 13		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 12 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 12 V, V _{GS} = 0 V, T _J = 85 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 8.1 A		0.016	0.022	Ω
		V _{GS} = - 2.5 V, I _D = - 7.1 A		0.021	0.028	
		V _{GS} = - 1.8 V, I _D = - 2.8 A		0.026	0.036	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 6 V, I _D = - 8.1 A		30		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 6 V, V _{GS} = 0 V, f = 1 MHz		2010		pF
Output Capacitance	C _{oss}			580		
Reverse Transfer Capacitance	C _{rss}			520		
Total Gate Charge	Q _g	V _{DS} = - 6 V, V _{GS} = - 8 V, I _D = - 8.1 A		43	65	nC
		V _{DS} = - 6 V, V _{GS} = - 4.5 V, I _D = - 8.1 A		26	40	
Gate-Source Charge	Q _{gs}			3.3		
Gate-Drain Charge	Q _{gd}			7.5		
Gate Resistance	R _g	f = 1 MHz		4.8		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.92 Ω I _D ≅ - 6.5 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			55	85	
Turn-Off Delay Time	t _{d(off)}			60	90	
Fall Time	t _f			40	60	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 6 V, R _L = 0.92 Ω I _D ≅ - 6.5 A, V _{GEN} = - 8 V, R _g = 1 Ω		10	15	
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			62	95	
Fall Time	t _f			35	55	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 3.5	A
Pulse Diode Forward Current ^a	I _{SM}				- 20	
Body Diode Voltage	V _{SD}	I _S = - 5.9 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 6.5 A, dI/dt = 100 A/μs, T _J = 25 °C		50	75	ns
Body Diode Reverse Recovery Charge	Q _{rr}			30	45	nC
Reverse Recovery Fall Time	t _a			18		ns
Reverse Recovery Rise Time	t _b			32		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

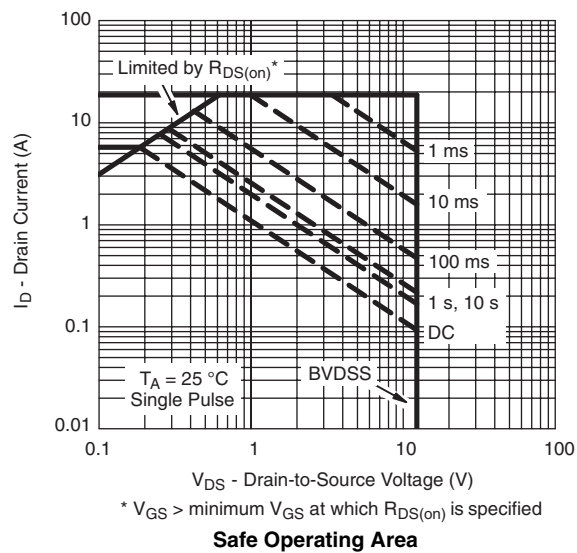
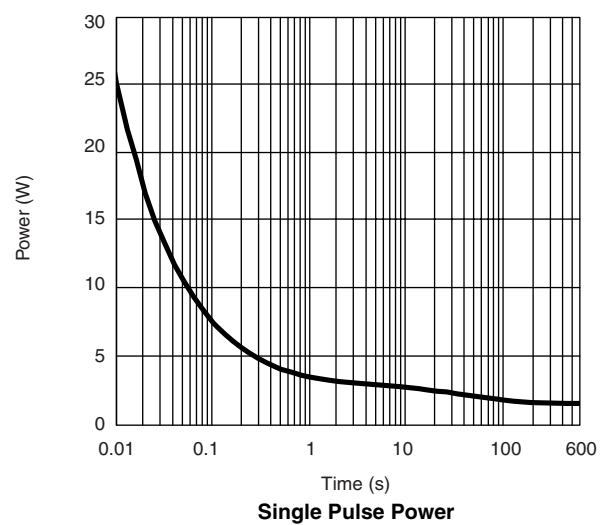
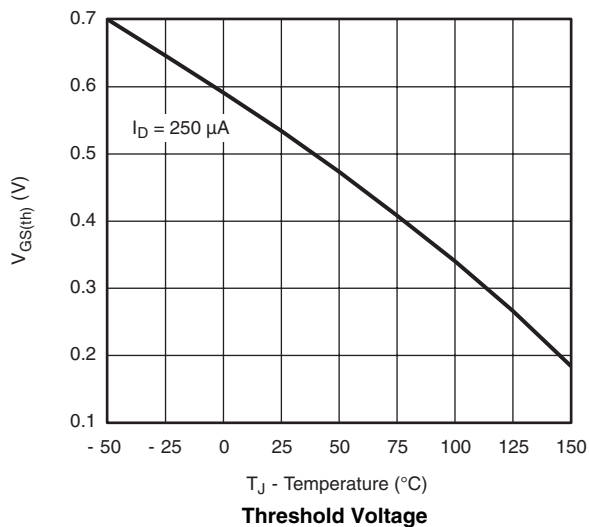
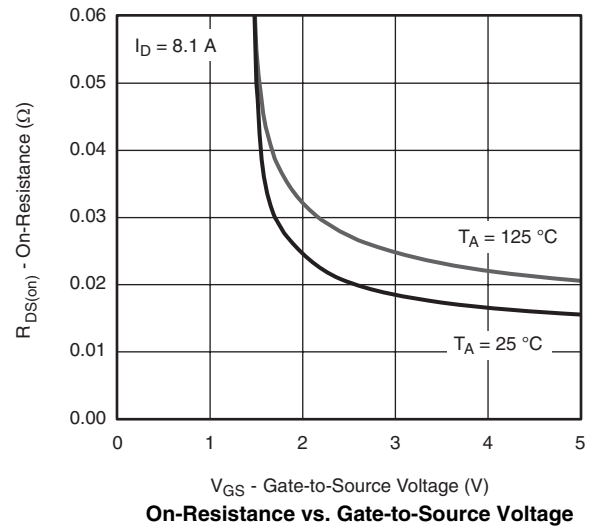
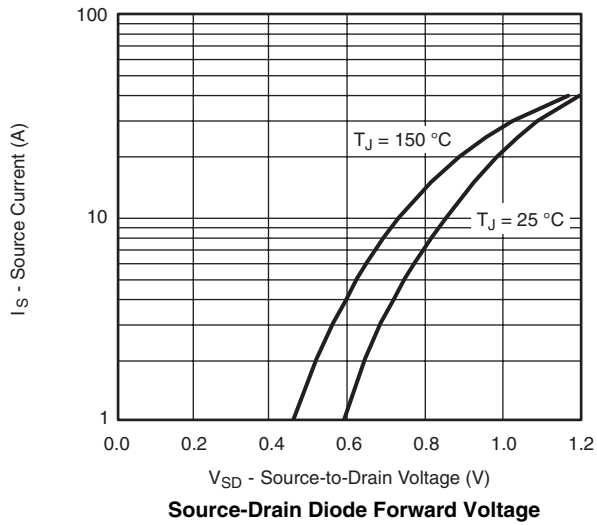
b. Guaranteed by design, not subject to production testing.

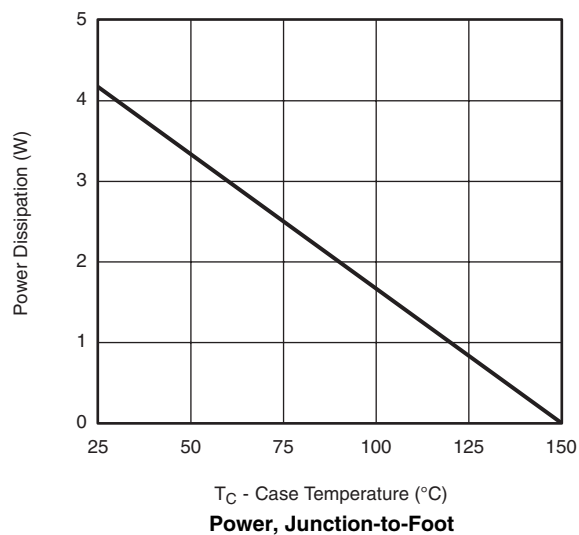
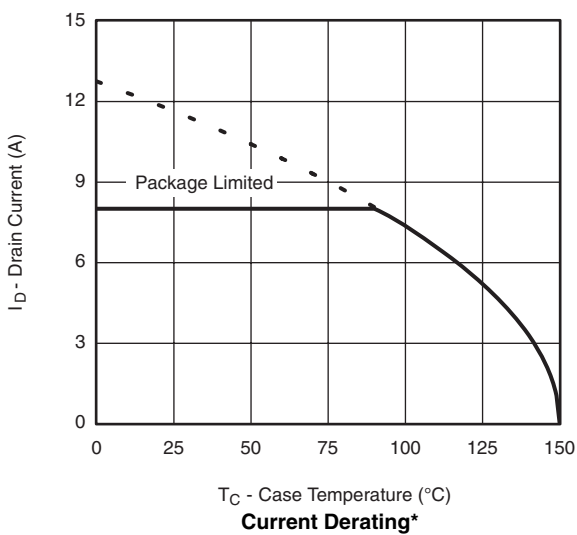
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

Si3473CDV

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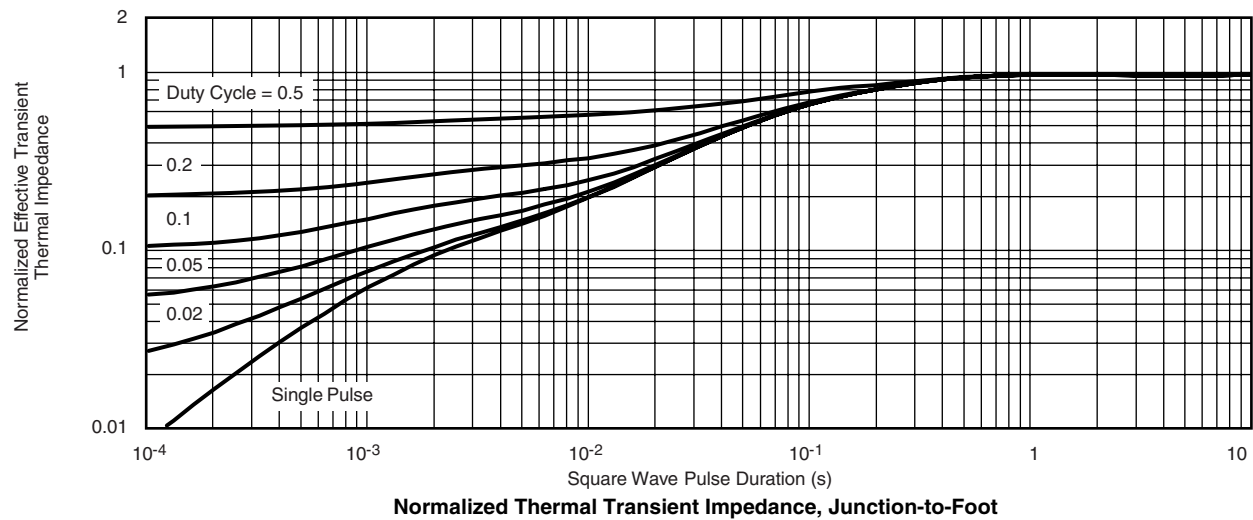
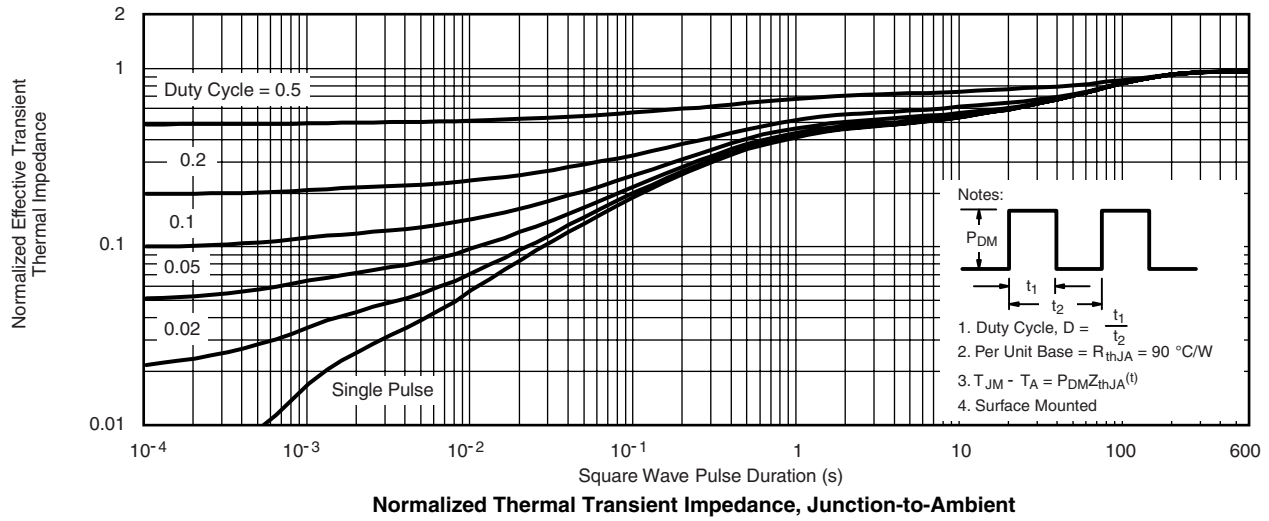
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

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