4 Micron CMOS Process Family

Process parameters

Process Parameters	4µm 10 volts	4µm 15 volts	Units
Metal I pitch (width/space)	4 / 4	4 / 4	µm
Metal II pitch (width/space)	3 / 4	3 / 4	µm
Poly pitch (width/space)	4 / 4	4 / 4	µm
Contact	4 x 4	4 x 4	µm
Via	3 x 3	3 x 3	µm
Gate geometry	4.0	4.0	µm
P-well junction depth	5.7	7.0	µm
N+ junction depth	1.5	1.4	µm
P+ junction depth	0.90	0.95	µm
Gate oxide thickness	640	800	Å
Inter poly oxide thick.	800	625	Å

Features

- Double Poly / Double Metal
- 8 µm Poly and Metal Pitch
- 10 Volts Maximum Operating Voltage
- 15 Volts High Voltage Option
- Isolated Vertical PNP Bipolar Module

Description

Dalsa Semiconductor's 4µm process is a double poly/double metal CMOS process with an operating voltage range of 5 to 10 volts. In addition, a high voltage option is also available in which a special drain structure allows the maximum operating voltage to be increased to 18 volts. No compromises are made with packing density since all high voltage gates are drawn at 4µm. Also, an Isolated Vertical PNP bipolar module with good gain characteristics and high BVceo can be implemented on both options.

MOSFET Electrical parameters

Electrical Parameters	4 MICRON - 10 volts						4 MICRON - 15 volts						Units	Conditions
	N Channel			P Channel			N Channel			P Channel				
	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.	min.	typ.	max.		
Vt (50x4µm)	0.4	0.7	0.9	0.4	0.7	0.9	0.6	0.9	1.2	0.8	1.1	1.4	V	saturation
Ids (50x4µm)		32			17			94			37		µA/µm	10V : Vds=Vgs= 3v 15V : Vds=Vgs=7.5v
Body factor		0.8			0.4			1.3			0.5		$\sqrt{v}$	
Bvdss	15	>20		15	>20		20	27		20	22		V	10V : Ids=1µA 15V : Ids=20nA
Subthres. slope		114			90			108			80		mV/dec.	Vds=0.1v
Field threshold	12	34		12	25		18	24		18	22		V	Ids = 14 µA
L effective		1.6			2.6			1.9			2.6		µm	L drawn = 4µm

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4 Micron CMOS Process Family (cont'd)

Resistances (Ω /sq.)

	4 µm - 10 volts			4 µm - 15 volts		
	min.	typ.	max.	min.	typ.	max.
Pwell		5200			3300	
Pfield in Pwell	1000	2000	3000	1000	2000	3000
N+	6	9	14	30	39	50
P+	70	94	110	75	90	125
Poly gate	14	21	26	16	20	28
Poly capacitor	30	43	80	20	28	50
Metal I		0.038			0.038	
Metal II		0.038			0.038	

Capacitances (fF/µm^2)

	4 µm - 10 volts			4 µm - 15 volts		
	min.	typ.	max.	min.	typ.	max.
Inter-poly	0.35	0.43	0.55	0.45	0.55	0.65
Gate oxide	0.51	0.54	0.58	0.41	0.43	0.46
N+ Junction		0.33			0.29	
P+ Junction		0.14			0.10	

Bipolar characteristics

		4 µm - 10 volts			4 µm - 15 volts		
		min.	typ.	max.	min.	typ.	max.
NPN vertical	Gain*		580			240	
	Bvceo (V)	70	90		70	90	
PNP vertical	Gain*	-	-	-	50	120	200
	Bvceo (V)	-	-	-	20	30	

*Test condition : Vce = 5 volts

Note: These values are for guidance only. Many of them can be adjusted to suit customer requirements. For full process specifications contact a Dalsa Semiconductor sales office or representative.

FIG 1: I-V Characteristics for a 50x4µm N-MOSFET (4µm High Voltage Process)

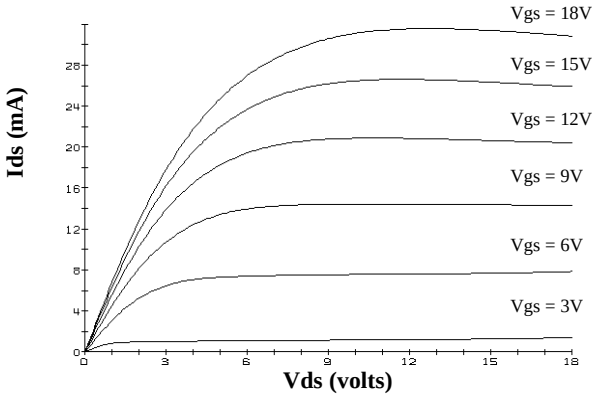

FIG 2 : I-V Characteristics for a 50x4µm P-MOSFET (4µm High Voltage Process)

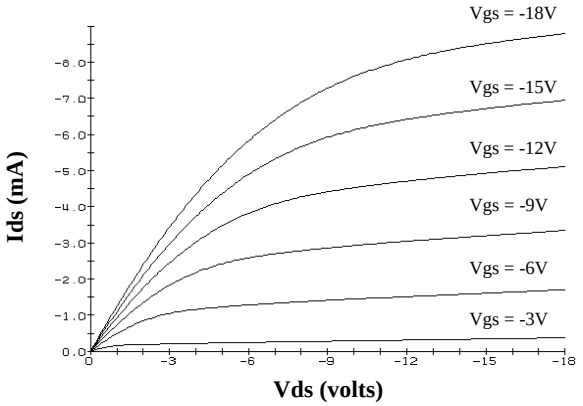

FIG 3:Substrate Current per Gate Width for a 50x4µm N-MOSFET (4µm High Voltage Process)

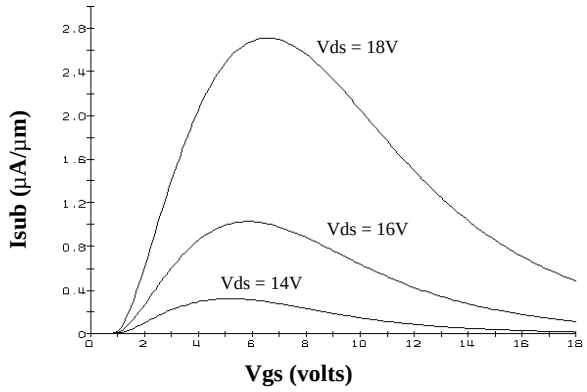

FIG 4 :Vertical PNP bipolar transistor