National Semiconductor

Not Intended For New Designs

T-66-31-51

100165
Universal Priority Encoder

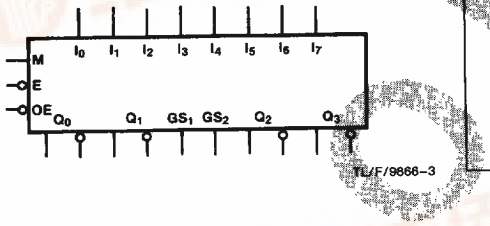
General Description

The 100165 contains eight input latches with a common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a single 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0–I_3. Q_2, Q_3 and GS_2 operate with I_4–I_7. A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol



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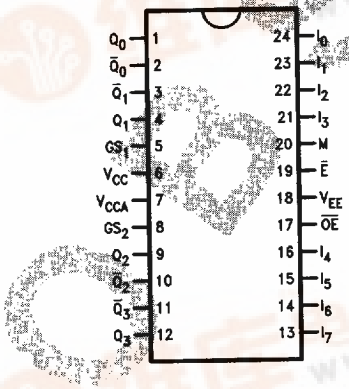
Pin Names	Description
I_0–I_7	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
M	Mode Control Input
GS_1–GS_2	Group Signal Outputs
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

Connection Diagrams

24-Pin DIP



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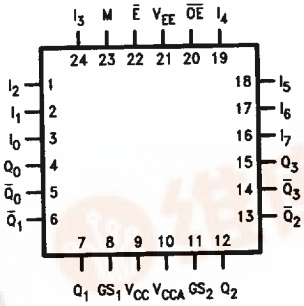
24-Pin Quad Cerpak



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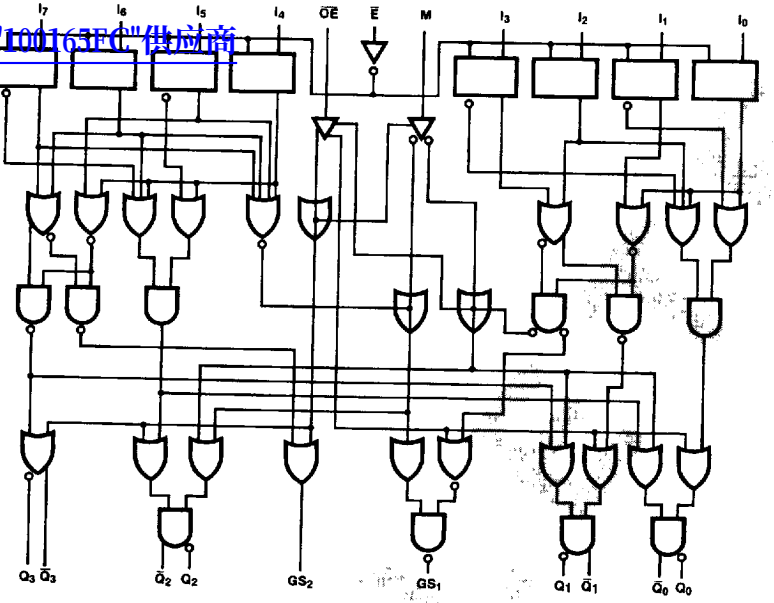
Logic Diagram



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Truth Table

Inputs										Outputs					
$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = H					

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			230	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−200	−140	−77	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	4.10	1.10	4.10	1.10	4.60	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.90	1.30	3.90	1.30	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	3.00	1.00	3.00	1.10	3.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.60	1.10	2.60	1.20	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.60	1.00	3.60	1.00	3.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.50	4.70	1.50	4.60	1.50	5.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 1, 2* and *3*
t_S	Setup Time I_0–I_7	1.00		0.90		1.00		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.20		1.20		1.20		ns	
$t_{pw(L)}$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

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Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	3.90	1.10	3.90	1.10	4.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.70	1.30	3.70	1.30	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	2.80	1.00	2.80	1.10	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.40	1.10	2.40	1.20	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.40	1.00	3.40	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.50	4.50	1.50	4.40	1.50	4.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1*, *2* and *3*
t_S	Setup Time I_0–I_7	0.90		0.80		0.90		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.10		1.10		1.10		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

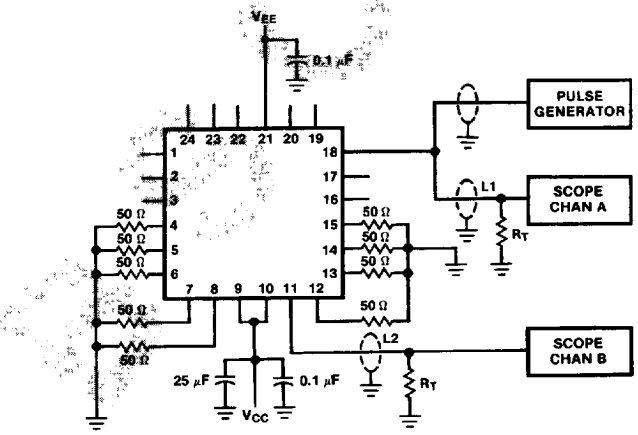

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FIGURE 1. AC Test Circuit

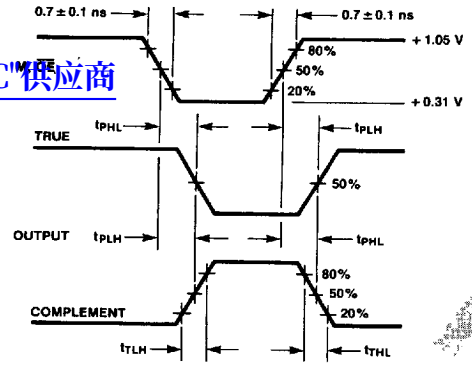

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FIGURE 2. Propagation Delay (M, $\overline{OE}$) and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

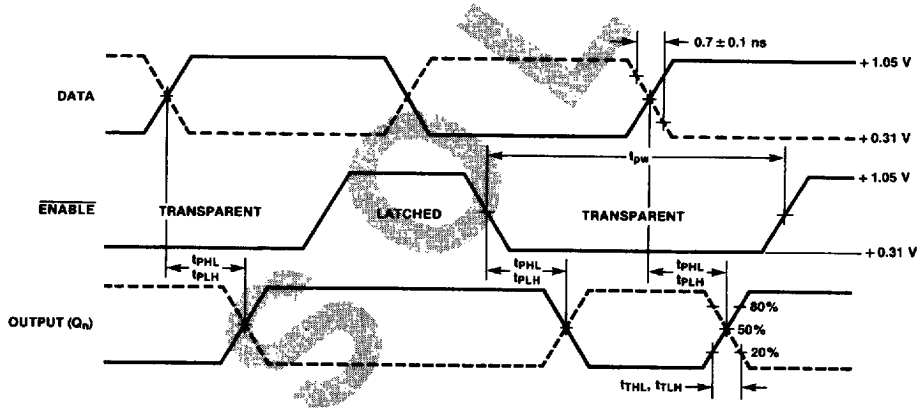

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FIGURE 3. Enable Timing

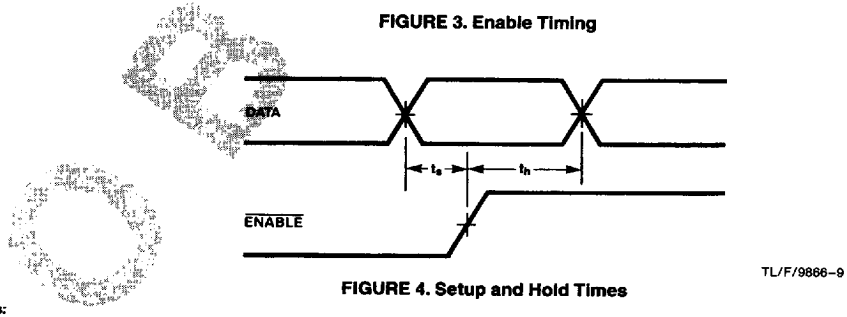

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FIGURE 4. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.