

3.3-V HIGH PERFORMANCE RAD-TOLERANT CLASS V, CLOCK SYNCHRONIZER AND JITTER CLEANER

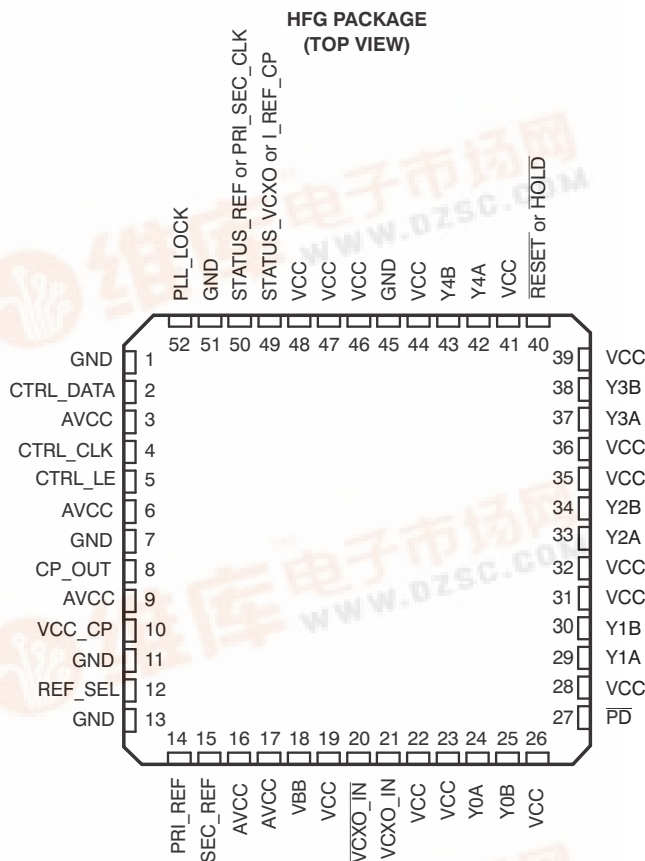
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FEATURES

- High Performance LVPECL and LVCMOS PLL Clock Synchronizer
- Two Reference Clock Inputs (Primary and Secondary Clock) for Redundancy Support With Manual or Automatic Selection
- Accepts LVCMOS Input Frequencies Up to 200 MHz
- VCXO_IN Clock is Synchronized to One of the Two Reference Clocks
- VCXO_IN Frequencies Up to 2 GHz (LVPECL)
- Outputs Can Be a Combination of LVPECL and LVCMOS (Up to Five Differential LVPECL Outputs or Up to 10 LVCMOS Outputs)
- Output Frequency is Selectable by x1, /2, /3, /4, /6, /8, /16 on Each Output Individually
- Efficient Jitter Cleaning From Low PLL Loop Bandwidth
- Low Phase Noise PLL Core
- Programmable Phase Offset (PRI_REF and SEC_REF to Outputs)
- Wide Charge Pump Current Range From 200 μ A to 3 mA
- Dedicated Charge Pump Supply (VCC_CP) for Wide Tuning Voltage Range VCOs
- Presets Charge Pump to VCC_CP/2 for Fast Center Frequency Setting of VC(X)O
- Analog and Digital PLL Lock Indication
- Provides VBB Bias Voltage Output for Single-Ended Input Signals (VCXO_IN)
- Frequency Hold Over Mode Improves Fail-Safe Operation
- Power-Up Control Forces LVPECL Outputs to 3-State at $V_{CC} < 1.5$ V
- SPI Controllable Device Setting
- 3.3-V Power Supply
- High-Performance 52 Pin Ceramic Quad Flat Pack (HFG)

- Rad-Tolerant : 50kRad (Si) TID
- QML-V Qualified, SMD 5962-07230
- Military Temperature Range
(–55°C to 125°C T_{case})

PIN ASSIGNMENTS



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CDCM7005-SP

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DESCRIPTION

The CDCM7005 is a high-performance, low phase noise and low skew clock synchronizer that synchronizes a VCXO (voltage controlled crystal oscillator) or VCO (voltage controlled oscillator) frequency to one of the two reference clocks. The programmable pre-divider M and the feedback-dividers N and P give a high flexibility to the frequency ratio of the reference clock to VC(X)O:

- $VC(X)O_IN / PRI_REF = (N \times P) / M$ or
- $VC(X)O_IN / SEC_REF = (N \times P) / M$

VC(X)O_IN clock operates up to 2 GHz. Through the selection of external VC(X)O and loop filter components, the PLL loop bandwidth and damping factor can be adjust to meet different system requirements.

The CDCM7005 can lock to one of two reference clock inputs (PRI_REF and SEC_REF), supports frequency hold-over mode and fast-frequency-locking for fail-safe and increased system redundancy. The outputs of the CDCM7005 are user definable and can be any combination of up to five LVPECL outputs or up to 10 LVCMOS outputs. The LVCMOS outputs are arranged in pairs (Y0A:Y0B, Y1A:Y1B, ...), so that each pair has the same frequency. But each output can be separately inverted and disabled. The built in synchronization latches ensure that all outputs are synchronized for low output skew.

All device settings, like outputs signaling, divider value, input selection, and many more, are programmable by SPI (3-wire serial peripheral interface). SPI allows individually control of the device settings.

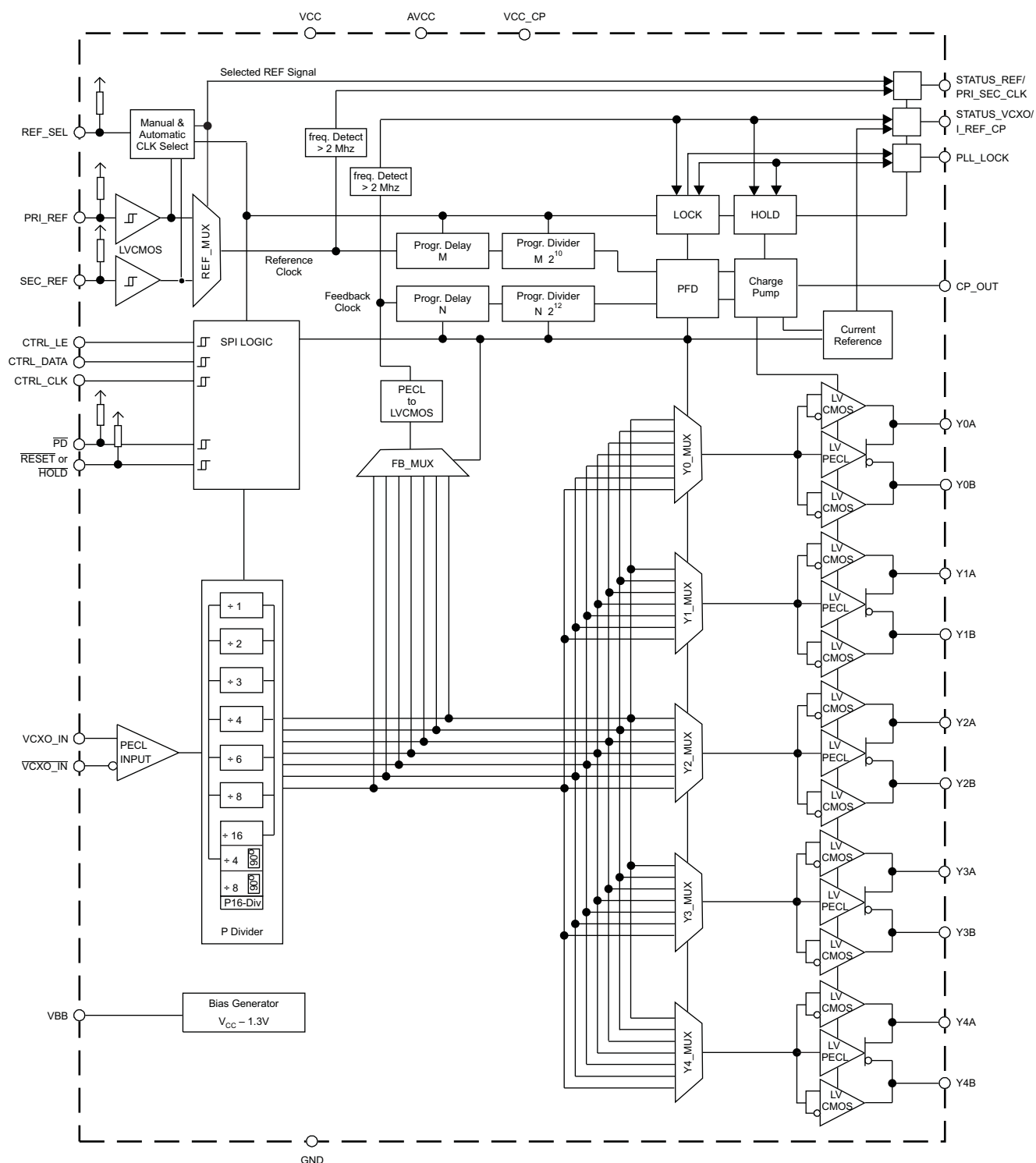
The device operates in a 3.3-V environment and is characterized for operation from -55°C to 125°C (T_{case}).

Table 1. ORDERING INFORMATION⁽¹⁾

TEMPERATURE	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C T_{case}	52 / HFG	5962-0723001VXC	5962-0723001VXC CDCM7005HFG-V

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



B0057-01

CDCM7005-SP

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Table 2. PIN ASSIGNMENT

TERMINAL		I/O	DESCRIPTION
NAME	HFG		
VCC	19, 22, 23, 26, 28, 31, 32, 35, 36, 39, 41, 44, 46, 47, 48	Power	3.3-V supply. V _{CC} and AV _{CC} should always have same supply voltage. It is recommended that AV _{CC} use its own supply filter.
GND	Thermal pad, and Pins: 1, 7, 11, 13, 45, 51	Ground	Ground
AVCC	3, 6, 9 16, 17	Analog Power	3.3-V analog power supply. There is no internal connection between AV _{CC} and V _{CC} . It is recommended that AV _{CC} use its own supply filter.
VCC_CP	10	Power	This is the charge pump power supply pin used to have the same supply as the external VCO. It can be set from 2.3 V to 3.6 V.
CTRL_LE	5	I	LVC MOS input, control latch enable for serial programmable Interface (SPI), with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-kΩ or larger pullup resistor to VCC.
CTRL_CLK	4	I	LVC MOS input, serial control clock input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-kΩ or larger pullup resistor to VCC.
CTRL_DATA	2	I	LVC MOS input, serial control data input for SPI, with hysteresis. Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-kΩ or larger pullup resistor to VCC.
$\overline{\text{PD}}$	27	I	LVC MOS input, asynchronous power down (PD) signal. This pin is low active and can be activated external or by the corresponding bit in the SPI register (in case of logic high, the SPI setting is valid). Switches the device into power-down mode. Resets M- and N-Divider, 3-states charge pump, STATUS_REF, or PRI_SEC_CLK pin, STATUS_VC XO or I_REF_CP pin, PLL_LOCK pin, VBB pin and all Yx outputs. Sets the SPI register to default value; has internal 150-kΩ pullup resistor. It is recommended to ramp up the $\overline{\text{PD}}$ with the same time as V _{CC} and AV _{CC} or later. The ramp up rate of the $\overline{\text{PD}}$ should not be faster than the ramp up rate of V _{CC} and AV _{CC} .
$\overline{\text{RESET}}$ or HOLD	40	I	This LVC MOS input can be programmed (SPI) to act as $\overline{\text{HOLD}}$ or $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ is the default function. This pin is low active and can be activated external or via the corresponding bit in the SPI register. In case of $\overline{\text{RESET}}$, the charge pump (CP) is switched to 3-state and all counters (N, M, P) are reset to zero (the initial divider settings are maintained in SPI registers). The LVPECL outputs are static low and high respectively and the LVC MOS outputs are all low or high if inverted. $\overline{\text{RESET}}$ is not edge triggered and should have a pulse duration of at least 5 ns. In case of $\overline{\text{HOLD}}$, the CP is switched in to 3-state mode only. After $\overline{\text{HOLD}}$ is released and with the next valid reference clock cycle the charge pump is switched back in to normal operation (CP stays in 3-state as long as no reference clock is valid). During HOLD, the P divider and all outputs Yx are at normal operation. This mode allows an external control of the frequency hold-over mode. The input has an internal 150-kΩ pullup resistor.
VC XO_IN	21	I	VC XO LVPECL input
$\overline{\text{VC XO_IN}}$	20	I	Complementary VC XO LVPECL input
PRI_REF	14	I	LVC MOS input for the primary reference clock, with an internal 150-kΩ pullup resistor and input hysteresis.
SEC_REF	15	I	LVC MOS input for the secondary reference clock, with an internal 150-kΩ pullup resistor and input hysteresis.
REF_SEL	12	I	LVC MOS reference clock selection input. In the manual mode the REF_SEL signal selects one of the two input clocks: REF_SEL [1]: PRI_REF is selected; REF_SEL [0]: SEC_REF is selected; The input has an internal 150-kΩ pullup resistor.
CP_OUT	8	O	Charge pump output

Table 2. PIN ASSINGMENT (continued)

TERMINAL		I/O	DESCRIPTION
NAME	HFG		
VBB	18	O	Bias voltage output to be used to bias unused complementary input $\overline{\text{VCXO_IN}}$ for single ended signals. The output of VBB is $V_{CC} - 1.3\text{ V}$. The output current is limited to about 1.5 mA.
STATUS_REF or PRI_SEC_CLK	50	O	<p>This output can be programmed (SPI) to provide either the STATUS_REF or PRI_SEC_CLK information. This pin is set high if one of the STATUS conditions is valid. STATUS_REF is the default setting.</p> <p>In case of STATUS_REF, the LVCMOS output provides the Status of the Reference Clock. If a reference clock with a frequency above 2 MHz is provided to PRI_REF or SEC_REF STATUS_REF will be set high.</p> <p>In case of PRI_SEC_CLK, the LVCMOS output indicates whether the primary clock [high] or the secondary clock [low] is selected.</p>
STATUS_VCXO or I_REF_CP	49	O	<p>This LVCMOS output can be programmed (SPI) to provide either the STATUS_VCXO information or serve as current path for the charge pump (CP). STATUS_VCXO is the default setting.</p> <p>In case of STATUS_VCXO, the LVCMOS output provides the status of the VCXO input (frequencies above 2 MHz are interpreted as valid clock; active high).</p> <p>In case of I_REF_CP, it provides the current path for the external reference resistor (12 kΩ \pm1%) to support an accurate charge pump current, optional. Do not use any capacitor across this resistor to prevent noise coupling via this node. If the internal 12 kΩ is selected (default setting), this pin can be left open.</p>
PLL_LOCK	52	I/O	<p>LVCMOS output for PLL_LOCK information. This pin is set high if the PLL is in lock (see feature description). This output can be programmed to be digital lock detect or analog lock detect (see feature description).</p> <p>The PLL is locked (set high), if the rising edge either of PRI_REF or SEC_REF clock and VCXO_IN clock at the phase frequency detector (PFD) are inside the lock detect window for a predetermined number of successive clock cycles.</p> <p>The PLL is out-of-lock (set low), if the rising edge of either the PRI_REF or SEC_REF) clock and VCXO_IN clock at the PFD are outside the lock detect window or if a cycle-slip occurs.</p> <p>Both, the lock detect window and the number of successive clock cycles are user definable (via SPI).</p>
Y0A:Y0B Y1A:Y1B Y2A:Y2B Y3A:Y3B Y4A:Y4B	24, 25, 29, 30, 33, 34, 37,38, 42, 43	O	The outputs of the CDCM7005 are user definable and can be any combination of up to five LVPECL outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI (Word 1, Bit 2-6). The power-up setting is all outputs are LVPECL.

ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V_{CC} , A_{VCC} , V_{CC_CP}	Supply voltage range ⁽²⁾	–0.5 V to 4.6 V
V_I	Input voltage range ⁽³⁾	–0.5 V to $V_{CC} + 0.5\text{ V}$
V_O	Output voltage range ⁽³⁾	–0.5 V to $V_{CC} + 0.5\text{ V}$
I_{OUT}	Output current for LVPECL/LVCMOS outputs ($0 < V_O < V_{CC}$)	$\pm 50\text{ mA}$
I_{IN}	Input current ($V_I < 0$, $V_I > V_{CC}$)	$\pm 20\text{ mA}$
T_{stg}	Storage temperature range	–65°C to 150°C
T_J	Maximum junction temperature	125°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All supply voltages have to be supplied at the same time.
- (3) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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Package Thermal Resistance for HFG Package ⁽¹⁾

PARAMETER		TEST CONDITIONS	TYP	UNIT
R _{θJA}	Junction-to-free-air thermal resistance	Board mounted, per JESD 51-5 methodology	21.813	°C/W
R _{θJC}	Junction-to-case thermal resistance	MIL-STD-883 test method 1012	0.849	°C/W

(1) Connected to GND with nine thermal vias (0,3 mm diameter).

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{CC} , AV _{CC}	Supply voltage	3	3.3	3.6	V
V _{CC_CP}		2.3		V _{CC}	
V _{IL}	Low-level input voltage LVCMOS, see ⁽¹⁾			0.3 V _{CC}	V
V _{IH}	High-level input voltage LVCMOS, see ⁽¹⁾	0.7 V _{CC}			V
I _{OH}	High-level output current LVCMOS (includes all status pins)			−8	mA
I _{OL}	Low-level output current LVCMOS (includes all status pins)			8	mA
V _I	Input voltage range LVCMOS	0		3.6	V
V _{INPP}	Input amplitude LVPECL (V _{VCXO_IN} − V _{VCXO_IN}) ⁽²⁾	0.5		1.3	V
V _{IC}	Common-mode input voltage LVPECL	1		V _{CC} −0.3	V
T _C	Operating case temperature	−55		125	°C

(1) V_{IL} and V_{IH} are required to maintain ac specifications; the actual device function tolerates a smaller input level of 1V, if an ac-coupling to V_{CC}/2 is provided.

(2) V_{INPP} minimum and maximum is required to maintain ac specifications; the actual device function tolerates at a minimum V_{INPP} of 150 mV.

TIMING REQUIREMENTS

over recommended ranges of supply voltage, load and operating free air temperature

PARAMETER		MIN	TYP	MAX	UNIT
PRI_REF/SEC_REF_IN REQUIREMENTS					
f _{REF_IN}	LVCMOS primary or secondary reference clock frequency ^{(1) (2)}	0		200	MHz
t _r /t _f	Rise and fall time of PRI_REF or SEC_REF signals from 20% to 80% of V _{CC}			4	ns
dutyREF	Duty cycle of PRI_REF or SEC_REF at V _{CC} /2	40%		60%	
VCXO_IN, VCXO_IN REQUIREMENTS					
f _{VCXO_IN}	VCXO clock frequency ⁽³⁾	0	2000		MHz
t _r /t _f	Rise and fall time 20% to 80% of VINPP at 80 MHz to 800 MHz ⁽⁴⁾			3	ns
dutyVCXO	Duty cycle of VCXO clock	40%		60%	
SPI/CONTROL REQUIREMENTS (see Figure 15)					
f _{CTRL_CLK}	CTRL_CLK frequency			20	MHz
t _{su1}	CTRL_DATA to CTRL_CLK setup time	10			ns
t _{h2}	CTRL_DATA to CTRL_CLK hold time	10			ns
t ₃	CTRL_CLK high duration	25			ns
t ₄	CTRL_CLK low duration	25			ns
t _{su5}	CTRL_LE to CTRL_CLK setup time	10			ns
t _{su6}	CTRL_CLK to CTRL_LE setup time	10			ns
t ₇	CTRL_LE pulse width	20			ns
t _r /t _f	Rise and fall time of CTRL_DATA CTRL_CLK, CTRL_LE from 20% to 80% of V _{CC}			4	ns

(1) At Reference Clock less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_REF signal to low. In this case, the status of the STATUS_REF is no longer relevant.

(2) f_{REF_IN} can be up to 250 MHz in typical operating mode (25°C / 3.3-V V_{CC}).

(3) If the Feedback Clock (derives from VCXO input) is less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_VCXO signal and PLL_LOCK signal to low. Both status signals are no longer relevant. This effects the HOLD-over function as well, as the PLL_LOCK signal is no longer valid!

(4) Use a square wave for lower frequencies (< 80 MHz).

TIMING REQUIREMENTS (continued)

over recommended ranges of supply voltage, load and operating free air temperature

PARAMETER	MIN	TYP	MAX	UNIT
PD, RESET, HOLD, REF_SEL REQUIREMENTS				
t_r / t_f Rise and fall time of the PD, RESET, HOLD, REF_SEL signal from 20% to 80% of V_{CC}			4	ns

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL						
I _{CC_LVPECL}	Supply current (I _{CC} over frequency see Figure 2 through Figure 5)	f _{VCXO} = 200 MHz, f _{REF_IN} = 25 MHz, PFD = 195.3125 kHz, I _{CP} = 2 mA, all outputs are LVPECL and Div-by-8 (load, see Figure 14)		210	260	mA
I _{CC_LVCMOS}		f _{VCXO} = 200 MHz, f _{REF_IN} = 25 MHz, PFD = 195.3125 kHz, I _{CP} = 2 mA, All outputs are LVCMOS and Div-by-8 (load, 10 pF)		120	160	mA
I _{CCPD}	Power-down current	f _{IN} = 0 MHz, V _{CC} = 3.6 V, AV _{CC} = 3.6 V, V _{CC_CP} = 3.6 V, V _I = 0 V or V _{CC}		100	300	μA
I _{OZ}	High-impedance state output current for Yx outputs	V _O = 0 V or V _{CC} – 0.8 V			±40	μA
		V _O = 0 V or V _{CC}			±100	μA
V _{I_REF_CP}	Voltage on I_REF_CP (external current path for accurate charge pump current)	12 kΩ to GND at pin 49	1.114	1.21	1.326	V
V _{BB}	Output reference voltage	V _{CC} = 3 V – 3.6 V; I _{BB} = –0.2 mA	V _{CC} –1.446	V _{CC} –1.3	V _{CC} –1.09	V
C _O	Output capacitance for Yx	V _{CC} = 3.3 V, V _O = 0 V or V _{CC}		3		pF
C _I	Input capacitance at PRI_REF and SEC_REF	V _I = 0 V or V _{CC} , V _I = 0 V or V _{CC}		3.6		pF
	Input capacitance at CTRL_LE, CTRL_CLOCK, CTRL_DATA	V _I = 0 V or V _{CC}		3		
LVCMOS						
f _{clk}	Output frequency (see ⁽²⁾ , ⁽³⁾ , Figure 7 , and Figure 8)	Load = 5 pF to GND, 1 kΩ to V _{CC} , 1 kΩ to GND		240		MHz
V _{IK}	LVCMOS input clamp voltage	V _{CC} = 3 V, I _I = –18 mA			–1.2	V
I _I	LVCMOS input current for CTRL_LE, CTRL_CLK, CTRL_DATA	V _I = 0 V or V _{CC} , V _{CC} = 3.6 V			±5	μA
I _{IH}	LVCMOS input current for <u>PD</u> , <u>RESET</u> , <u>HOLD</u> , REF_SEL, PRI_REF, SEC_REF, (see ⁽⁴⁾)	V _I = V _{CC} , V _{CC} = 3.6 V			5	μA
I _{IL}	LVCMOS input current for <u>PD</u> , <u>RESET</u> , <u>HOLD</u> , REF_SEL, PRI_REF, SEC_REF (see ⁽⁴⁾)	V _I = 0 V, V _{CC} = 3.6 V	–15		–35	μA
V _{OH}	High-level output voltage for LVCMOS outputs	V _{CC} = min to max, I _{OH} = –100 μA	V _{CC} –0.1			V
		V _{CC} = 3 V, I _{OH} = –6 mA	2.4			
		V _{CC} = 3 V, I _{OH} = –12 mA	2			
V _{OL}	Low-level output voltage for LVCMOS outputs	V _{CC} = min to max, I _{OL} = 100 μA			0.1	V
		V _{CC} = 3 V, I _{OL} = 6 mA			0.5	
		V _{CC} = 3 V, I _{OL} = 12 mA			0.8	
I _{OH}	High-level output current	V _{CC} = 3.3 V, V _O = 1.65 V	–50	–30	–20	mA
I _{OL}	Low-level output current	V _{CC} = 3.3 V, V _O = 1.65 V	20	30	50	mA

 (1) All typical values are at $V_{CC} = 3.3$ V, temperature = 25°C.

 (2) f_{clk} can be up to 400 MHz in the typical operating mode (25°C / 3.3-V V_{CC}).

(3) Operating the LVC MOS or LVPECL output above the maximum frequency will not cause a malfunction to the device, but the output signal swing may no longer meet the output specification.

(4) These inputs have an internal 150-kΩ pullup resistor.

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DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
tpho	Phase offset (REF_IN to Y output) ⁽⁵⁾	VREF_IN = V _{CC} /2, Y = V _{CC} /2, see Figure 12 , Load = 10 pF		2.7		ns
t _{sk(p)}	LVC MOS pulse skew, see Figure 11	Crosspoint to V _{CC} /2 load, see Figure 13		160		ps
t _{pd(LH)}	Propagation delay from VCXO_IN to Yx, see Figure 11	Crosspoint to V _{CC} /2, Load = 10 pF, see Figure 13 (PLL bypass mode)		2.8		ns
t _{pd(HL)}						
t _{sk(o)}	LVC MOS single-ended output skew, see ⁽⁶⁾ and Figure 11	All outputs have the same divider ratio		80		ps
		Outputs have different divider ratios		80		
Duty cycle	LVC MOS	V _{CC} /2 to V _{CC} /2	49%		51%	
t _{slew-rate}	Output rise/fall slew rate	20% to 80% of swing (load see Figure 13)		3.5		V/ns
LVPECL						
f _{clk}	Output frequency, see ⁽⁷⁾ and Figure 6	Load, see Figure 14	0	2000		MHz
I _I	LVPECL input current	V _I = 0 V or V _{CC}			±20	μA
V _{OH}	LVPECL high-level output voltage	Load, See Figure 14	V _{CC} –1.18		V _{CC} –0.81	V
V _{OL}	LVPECL low-level output voltage	Load, See Figure 14	V _{CC} –2		V _{CC} –1.55	V
V _{OD}	Differential output voltage	See Figure 10 and load, see Figure 14	500			mV
t _{pho}	Phase offset (REF_IN to Y output) ⁽⁶⁾	VREF_IN = V _{CC} /2 to cross point of Y, see Figure 12		250		ps
t _{pd(LH)}	Propagation delay time, VCXO_IN to Yx, see Figure 11	Cross point-to-cross point, load see Figure 14		615		ps
t _{pd(HL)}						
t _{sk(p)}	LVPECL pulse skew, see Figure 11	Cross point-to-cross point, load see Figure 14		15		ps
t _{sk(o)}	LVPECL output skew ⁽⁸⁾	Load see Figure 14 , all outputs have the same divider ratio		20		ps
		Load see Figure 14 , outputs have different divider ratios		50		
t _r / t _f	Rise and fall time	20% to 80% of V _{OUTPP} , see Figure 10		170		ps
C _I	Input capacitance at VCXO_IN, VCXO_IN			2.5		pF
LVC MOS-TO-LVPECL						
t _{sk(P_C)}	Output skew between LVC MOS and LVPECL outputs, see ⁽⁹⁾ and Figure 11	Cross point to V _{CC} /2; load, see Figure 13 and Figure 14		2	3.2	ns
PLL ANALOG LOCK						
I _{OH}	High-level output current	V _{CC} = 3.6 V, V _O = 1.8 V	–150	–110	–80	μA
I _{OL}	Low-level output current	V _{CC} = 3.6 V, V _O = 1.8 V	80	110	150	μA
I _{OZH LOCK}	High-impedance state output current for PLL LOCK output ⁽¹⁰⁾	V _O = 3.6 V ($\overline{\text{PD}}$ is set low)		45	65	μA
I _{OZL LOCK}	High-impedance state output current for PLL LOCK output ⁽¹⁰⁾	V _O = 0 V ($\overline{\text{PD}}$ is set low)			±5	μA
V _{IT+}	Positive input threshold voltage	V _{CC} = min to max		V _{CC} ×0.55		V
V _{IT–}	Negative input threshold voltage	V _{CC} = min to max		V _{CC} ×0.35		V
PHASE DETECTOR						
f _{CPmax}	Maximum charge pump frequency	Default PFD pulse width delay		100		MHz
CHARGE PUMP						
I _{CP}	Charge pump sink/source current range ⁽¹¹⁾	V _{CP} = 0.5 V _{CC_CP}	±0.2		±3.9	mA

(5) This is valid only for the same frequency of REF_IN clock and Y output clock. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).

(6) The t_{sk(o)} specification is only valid for equal loading of all outputs.

(7) Operating the LVC MOS or LVPECL output above the maximum frequency will not cause a malfunction to the device, but the output signal swing may no longer meet the output specification.

(8) The t_{sk(o)} specification is only valid for equal loading of all outputs.

(9) The phase of LVC MOS is lagging in reference to the phase of LVPECL.

(10) Lock output has an 80-kΩ pulldown resistor.

(11) Defined by SPI settings.

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I_{CP3St} Charge pump 3-state current	Temperature = 25°C, $0.5\text{ V} < V_{CP} < V_{CC_CP} - 0.5\text{ V}$	-10		10	nA
	Temperature = -55°C to 125°C, $0.5\text{ V} < V_{CP} < V_{CC_CP} - 0.5\text{ V}$	-50		50	
I_{CPA} ICP absolute accuracy	$V_{CP} = 0.5 V_{CC_CP}$, internal reference resistor, SPI default settings	-20%	10%	20%	
	$V_{CP} = 0.5 V_{CC_CP}$, external reference resistor 12 k Ω (1%) at I_{REF_CP} , SPI default settings		5%		
I_{CPM} Sink/source current matching	$0.5\text{ V} < V_{CP} < V_{CC_CP} - 0.5\text{ V}$, SPI default settings	-7%	2.5%	7%	
I_{VCPM} ICP vs VCP matching	$0.5\text{ V} < V_{CP} < V_{CC_CP} - 0.5\text{ V}$	-10%	5%	10%	

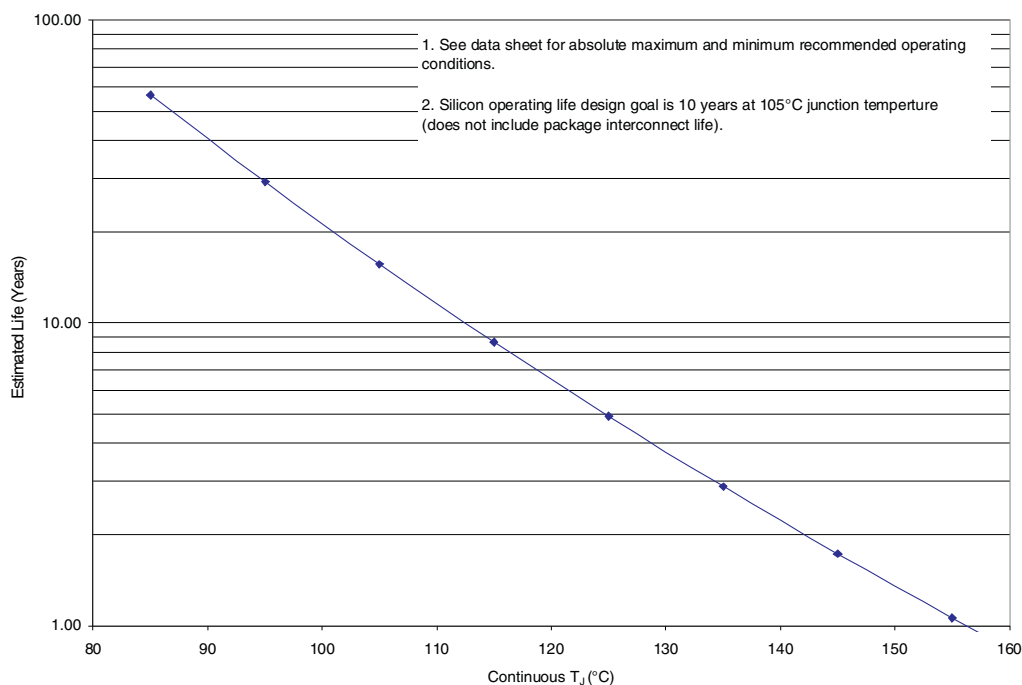
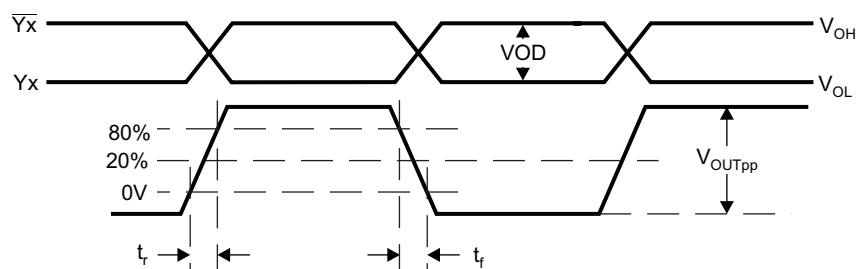


Figure 1. CDCM7005HFG-V - 52/HFG Package Operating Life Derating Chart

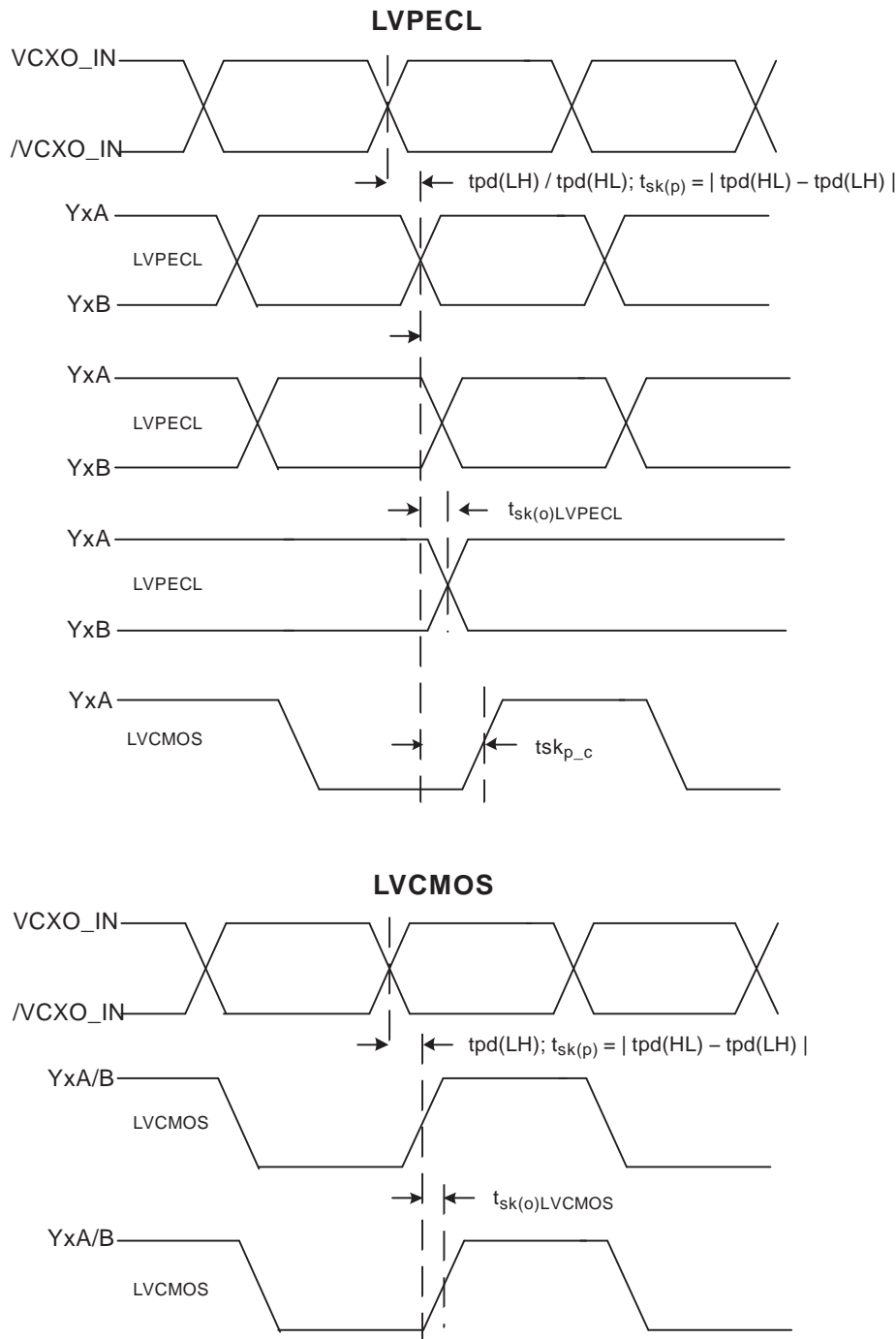
TYPICAL CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

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Figure 10. LVPECL Differential Output Voltage and Rise/Fall Time

PARAMETER MEASUREMENT INFORMATION (continued)



- A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
 The difference between the fastest and the slowest $t_{pd}(LH)_n$ ($n = 0 \dots 4$)
 The difference between the fastest and the slowest $t_{pd}(HL)_n$ ($n = 0 \dots 4$)
- B. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd}(HL)$) and the low-to-high ($t_{pd}(LH)$) propagation delays when a single switching input causes one or more outputs to switch,
 $t_{sk(p)} = |t_{pd}(HL) - t_{pd}(LH)|$. Pulse skew is sometimes referred to as *pulse width distortion* or *duty cycle skew*.

Figure 11. Output Skew

PARAMETER MEASUREMENT INFORMATION (continued)

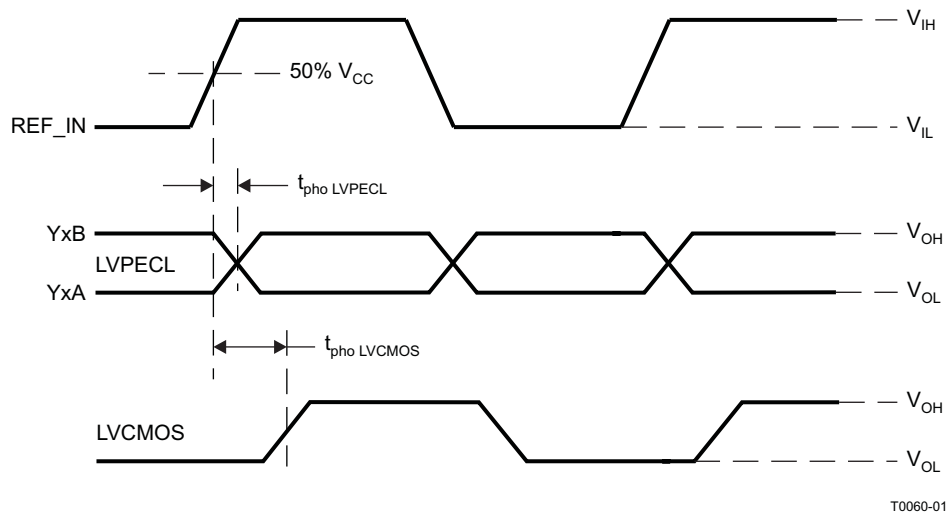


Figure 12. Phase Offset

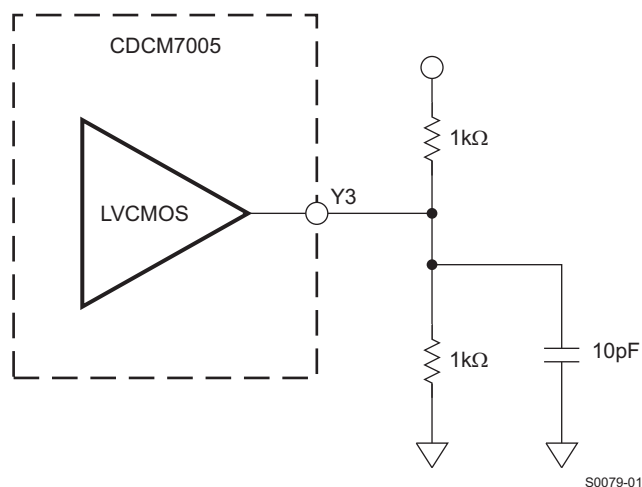
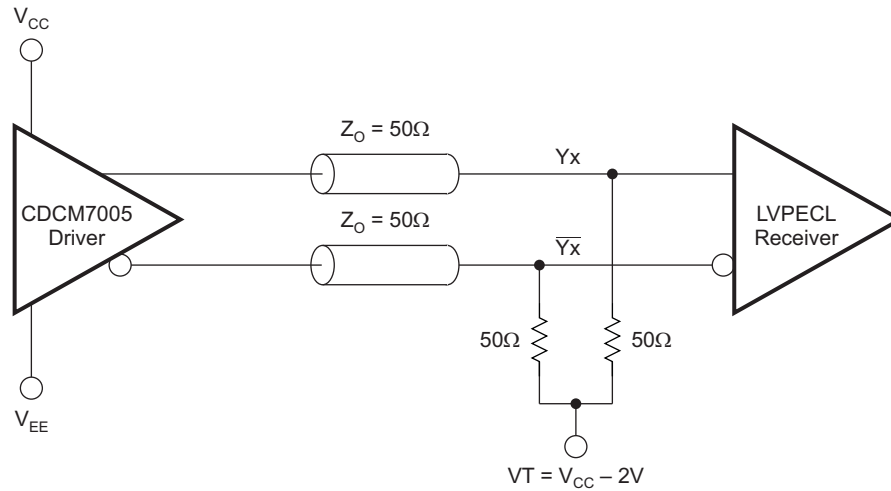


Figure 13. LVCMOS Output Loading During Device Test

PARAMETER MEASUREMENT INFORMATION (continued)

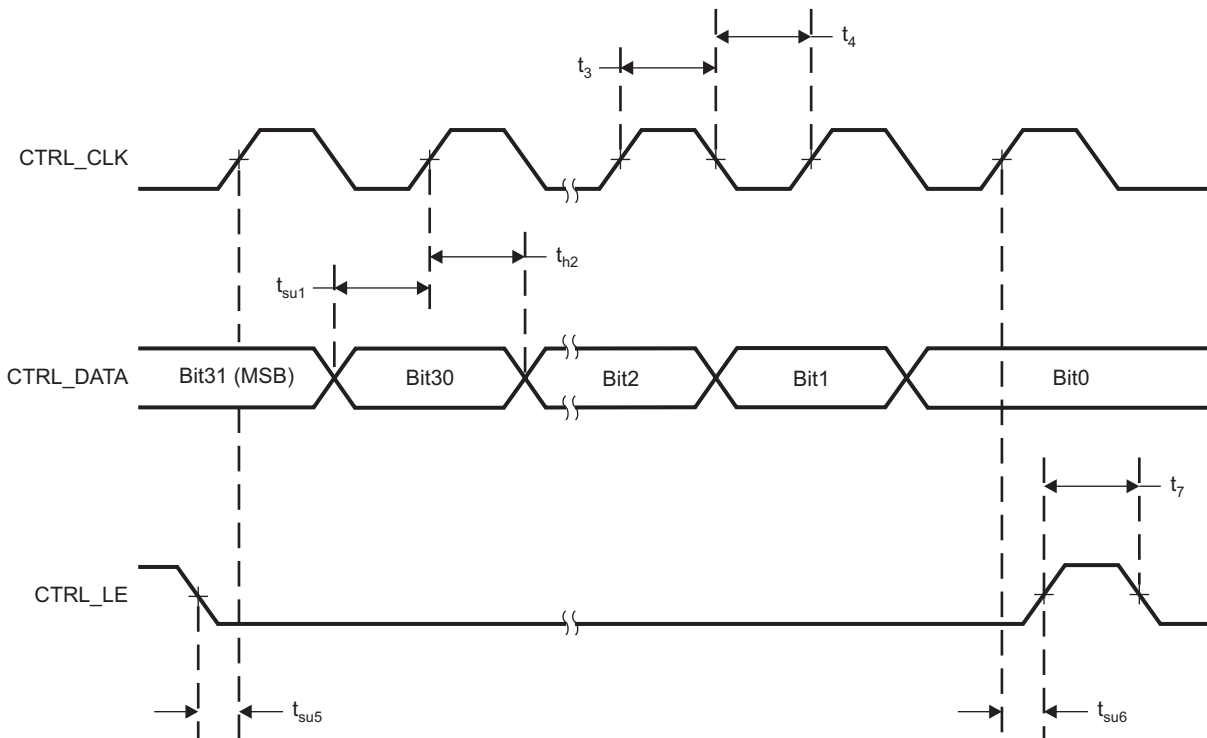


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Figure 14. LVPECL Output Loading During Device Test

SPI CONTROL INTERFACE

The serial interface of the CDCM7005 is a simple SPI-compatible interface for writing to the registers of the device and consists of three control lines: CTRL_CLK, CTRL_DATA, and CTRL_LE. There are four 32 bit wide registers, which can be addressed by the two LSBs of a transferred word (bit 0 and bit 1). Every transmitted word must have 32 bits, starting with MSB first. Each word can be written separately. Bit 7, 8, 10, and Bit 12 to 31 of Word 3 are reserved for factory test purposes and must be filled with zeros. The transfer is initiated with the falling edge of CTRL_LE; as long as CTRL_LE is high, no data can be transferred. During CTRL_LE, low data can be written. The data has to be applied at CTRL_DATA and has to be stable before the rising edge of CTRL_CLK. The transmission is finished by a rising edge of CTRL_LE. With the rising edge of CTRL_LE, the new word is asynchronously transferred to the internal register (e.g., N, M, P, ...). Each word has to be separately transmitted by this procedure. Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-kΩ or larger pullup resistor to VCC.

PARAMETER MEASUREMENT INFORMATION (continued)

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Figure 15. Timing Diagram SPI Control Interface

The SPI serial protocol accepts word Write operation only. There is neither a read, acknowledge, nor a handshake operation.

The following four words include the register settings of the programmable functions of the CDCM7005. It can be modified to the customer application by changing one or more bits. It comes up with a default register setting after power up or if the power down (\overline{PD}) control signal is applied. The default setting is shown in column five of the following words.

It is recommended to program Word 0, Word 1, Word 2 and Word 3 right after power up and \overline{PD} becomes HIGH.

A low active function is shown as [0] and a high active function is shown as [1].

PARAMETER MEASUREMENT INFORMATION (continued)

Word 0

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PINS AFFECTED
0	C0		Register Selection	0	
1	C1		Register Selection	0	
2	M0	Reference Divider M	Reference Divider M Bit 0	1	
3	M1		Reference Divider M Bit 1	1	
4	M2		Reference Divider M Bit 2	1	
5	M3		Reference Divider M Bit 3	1	
6	M4		Reference Divider M Bit 4	1	
7	M5		Reference Divider M Bit 5	1	
8	M6		Reference Divider M Bit 6	1	
9	M7		Reference Divider M Bit 7	0	
10	M8		Reference Divider M Bit 8	0	
11	M9		Reference Divider M Bit 9	0	
12	N0	VC(X)O Divider N ⁽¹⁾	VCXO Divider N Bit 0	1	
13	N1		VCXO Divider N Bit 1	1	
14	N2		VCXO Divider N Bit 2	1	
15	N3		VCXO Divider N Bit 3	1	
16	N4		VCXO Divider N Bit 4	1	
17	N5		VCXO Divider N Bit 5	1	
18	N6		VCXO Divider N Bit 6	1	
19	N7		VCXO Divider N Bit 7	0	
20	N8		VCXO Divider N Bit 8	0	
21	N9		VCXO Divider N Bit 9	0	
22	N10		VCXO Divider N Bit 10	0	
23	N11		VCXO Divider N Bit 11	0	
24	DLYM0	Progr. Delay M	Reference Phase Delay M Bit 0	0	
25	DLYM1		Reference Phase Delay M Bit 1	0	
26	DLYM2		Reference Phase Delay M Bit 2	0	
27	DLYN0	Progr. Delay N	Feedback Phase Delay N Bit 0	0	
28	DLYN1		Feedback Phase Delay N Bit 1	0	
29	DLYN2		Feedback Phase Delay N Bit 2	0	
30	MANAUT	Manual or Auto Ref.	Manual Reference Clock Selection [0] Automatic Reference Clock Selection [1]	0	14, 15
31	REFDEC	Freq. Detect	Reference Frequency Detection on [0], off [1] ⁽²⁾	0	50

(1) The frequency applied to the Divider N must be smaller than 250 MHz. A sufficient P Divider must be selected with the FB_MUX to maintain this criteria.

(2) If set to low, STATUS_REF will be in normal operation. If set to high, STATUS_REF will be high, even if no valid clock is detected (<2 MHz). This is useful for reference inputs frequencies less than 2 MHz where the frequency detection circuitry normally resets the STATUS_REF signal to low.

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Word 1

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PINS AFFECTED
0	C0		Register Selection	1	
1	C1		Register Selection	0	
2	OUTSEL0	Output (Yx) Signaling Selection	For Output Y0A, Y0B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	24, 25
3	OUTSEL1		For Outputs Y1A, Y1B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	29, 30
4	OUTSEL2		For Outputs Y2A, Y2B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	33, 34
5	OUTSEL3		For Outputs Y3A, Y3B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	37, 38
6	OUTSEL4		For Outputs Y4A, Y4B: LVPECL = enabled [1]; LVCMOS = enabled [0];	1	42, 43
7	OUT0A0	Output Y0 Mode	Output Y0A Mode Bit 0	0	24
8	OUT0A1		Output Y0A Mode Bit 1	0	24
9	OUT0B0		Output Y0B Mode Bit 0	0	25
10	OUT0B1		Output Y0B Mode Bit 1	0	25
11	OUT1A0	Output Y1 Mode	Output Y1A Mode Bit 0	0	29
12	OUT1A1		Output Y1A Mode Bit 1	0	29
13	OUT1B0		Output Y1B Mode Bit 0	0	30
14	OUT1B1		Output Y1B Mode Bit 1	0	30
15	OUT2A0	Output Y2 Mode	Output Y2A Mode Bit 0	0	33
16	OUT2A1		Output Y2A Mode Bit 1	0	33
17	OUT2B0		Output Y2B Mode Bit 0	0	34
18	OUT2B1		Output Y2B Mode Bit 1	0	34
19	OUT3A0	Output Y3 Mode	Output Y3A Mode Bit 0	0	37
20	OUT3A1		Output Y3A Mode Bit 1	0	37
21	OUT3B0		Output Y3B Mode Bit 0	0	38
22	OUT3B1		Output Y3B Mode Bit 1	0	38
23	OUT4A0	Output Y4 Mode	Output Y4A Mode Bit 0	0	42
24	OUT4A1		Output Y4A Mode Bit 1	0	42
25	OUT4B0		Output Y4B Mode Bit 0	0	43
26	OUT4B1		Output Y4B Mode Bit 1	0	43
27	SREF	Status Ref.	Displays the status of the reference clock at the STATUS_REF output [0] Displays the selected clock (high for PRI_REF and low for SEC_REF clock) at the STATUS_REF output [1]	0	50
28	SXOIREF	Status VCXO or I_REF_CP	Selects STATUS_VCXO [0] Selects I_REF_CP [1] which enable external reference resistor used for charge pump current and analog PLL lock detect output current.	0	49, 52
29	ADLOCK	Analog or Digital Lock	Selects Digital PLL_LOCK [0] Selects Analog PLL_LOCK [1]	0	52
30	90DIV4	90 degree shift div-4	90 degree output phase shift in div-4 mode on [1]; off [0] ⁽¹⁾	0	Yx

- (1) The P 16-Div has to be selected to obtain the 90 degree phase shift. If bit 30 or bit 31 is set, the Div-by-16 mode is no longer available. The outputs are switched in pairs. Only one bit can be set at a time. If both bits set to [1] at the same time, no 90 degree phase shift mode is selected (equal to off-mode setting).

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PINS AFFECTED
31	90DIV8	90 degree shift div-8	90 degree output phase shift in div-8 mode on [1]; off [0] ⁽¹⁾	0	Yx

Word 2

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PINS AFFECTED
0	C0		Register Selection	0	
1	C1		Register Selection	1	
2	CP_DIR	CP Direction	Determines in which direction CP current regulates (Reference Clock leads to Feedback Clock – see Figure 24) – positive CP output current [0]; – negative CP output current [1];	0	8
3	PRECP		Preset charge pump output voltage to VCC_CP/2, on [1], off [0]	0	8
4	CP0	CP Current	CP Current Setting Bit 0	0	8
5	CP1		CP Current Setting Bit 1	1	8
6	CP2		CP Current Setting Bit 2	0	8
7	CP3		CP Current Setting Bit 3	1	8
8	PFD0	PFD Pulse Width	PFD Pulse Width PFD Bit 0	0	8
9	PFD1		PFD Pulse Width PFD Bit 1	0	8
10	FBMUX0	FB_MUX	Feedback MUX Select Bit 0	1	
11	FBMUX1		Feedback MUX Select Bit 1	0	
12	FBMUX2		Feedback MUX Select Bit 2	1	
13	Y0MUX0	Y0_MUX	Output Y0x Select Bit 0	1	24, 25
14	Y0MUX1		Output Y0x Select Bit 1	0	24, 25
15	Y0MUX2		Output Y0x Select Bit 2	1	24, 25
16	Y1MUX0	Y1_MUX	Output Y1x Select Bit 0	1	29, 30
17	Y1MUX1		Output Y1x Select Bit 1	0	29, 30
18	Y1MUX2		Output Y1x Select Bit 2	1	29, 20
19	Y2MUX0	Y2_MUX	Output Y2x Select Bit 0	1	33, 34
20	Y2MUX1		Output Y2x Select Bit 1	0	33, 34
21	Y2MUX2		Output Y2x Select Bit 2	1	33, 34
22	Y3MUX0	Y3_MUX	Output Y3x Select Bit 0	1	37, 38
23	Y3MUX1		Output Y3x Select Bit 1	0	37, 38
24	Y3MUX2		Output Y3x Select Bit 2	1	37, 38
25	Y4MUX0	Y4_MUX	Output Y4x Select Bit 0	1	42, 43
26	Y4MUX1		Output Y4x Select Bit 1	0	42, 43
27	Y4MUX2		Output Y4x Select Bit 2	1	42, 43
28	$\overline{\text{PD}}$		Power Down mode on [0], off [1]	1	Yx
29	RESHOL		$\overline{\text{RESET}}$ or $\overline{\text{HOLD}}$ Pin definition: $\overline{\text{RESET}}$ [0] or $\overline{\text{HOLD}}$ [1]	0	40
30	$\overline{\text{RESET}}$		Resets all dividers [0] - (equal to $\overline{\text{RESET}}$ pin function)	1	
31	$\overline{\text{HOLD}}$		3-state charge pump [0] - (equal to $\overline{\text{HOLD}}$ pin function)	1	8

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Word 3

BIT	BIT NAME		DESCRIPTION/FUNCTION	POWER UP CONDITION	PINS AFFECTED
0			Register selection	1	
1			Register selection	1	
2	LOCKW 0	Lock Window	Lock-detect window Bit 0	1	52
3	LOCKW 1		Lock-detect window Bit 1	0	52
4	LOCKC0	Lock Cycles	Number of coherent lock events Bit 0	0	52
5	LOCKC1		Number of coherent lock events Bit 1	1	52
6	CSLIP	Cycle Slip	Cycle slip mode only for out-of-lock detection on [1] or off [0] ⁽¹⁾	0	52
7	RES		RESERVED	0	RES
8	RES		RESERVED	0	RES
9	HOLDF	HOLD Function	Enables the frequency hold-over function on [1], off [0]	0	
10			RESERVED	0	RES
11	HOLDTR	HOLD Trigger Condition	HOLD function always activated [1]; ⁽²⁾ Triggered by analog PLL lock detect outputs [0] (if analog PLL Lock signal is set then HOLD is activated; if analog PLL lock signal is reset then HOLD is de-activated).	0	
12	RES		RESERVED	0	RES
13	RES		RESERVED	0	RES
14	RES		RESERVED	0	RES
15	RES		RESERVED	0	RES
16	GTME		General Test Mode Enable. Test Mode is only enabled if this bit is set to 1.	0	
17	RES		RESERVED	0	RES
18	RES		RESERVED	0	RES
19	RES		RESERVED	0	RES
20	RES		RESERVED	0	RES
21	RES		RESERVED	0	RES
22	RES		RESERVED	0	RES
23	RES		RESERVED	0	RES
24	RES		RESERVED	0	RES
25	RES		RESERVED	0	RES
26	RES		RESERVED	0	RES
27	RES		RESERVED	0	RES
28	PFD FC		PFD Frequency Control. Data provided to the PFD are feed through to the corresponding STATUS pins. ⁽³⁾	0	49
29	RES		RESERVED	0	RES
30	RES		RESERVED	0	RES
31	RES		RESERVED	0	RES

(1) If Cycle Slip mode only for out-of-lock detection is on, the selected lock detect window is valid for lock detect. Independent from this, out of lock is detected if a cycle slip occurs.

(2) HOLD function always activated is recommended for test purposes only.

(3) The maximum frequency for the STATUS_VCXO pin is 100 MHz.

FUNCTIONAL DESCRIPTION OF THE LOGIC

Reference Divider M (Word 0)⁽⁴⁾

M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Div by	Default
0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	1	2	
0	0	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	1	1	4	
					• • •						
0	0	0	1	1	1	1	1	1	1	128	Yes
					• • •						
1	1	1	1	1	1	1	1	0	1	1022	
1	1	1	1	1	1	1	1	1	0	1023	
1	1	1	1	1	1	1	1	1	1	1024	

(4) If the divider value is Q, then the code will be the binary value of (Q–1).

VC(X)O Feedback Divider N (Word 0)^{(1) (2)}

N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	Div by	Default
0	0	0	0	0	0	0	0	0	0	0	0	1	
0	0	0	0	0	0	0	0	0	0	0	1	2	
0	0	0	0	0	0	0	0	0	0	1	0	3	
0	0	0	0	0	0	0	0	0	0	1	1	4	
						• • •							
0	0	0	0	0	1	1	1	1	1	1	1	128	Yes
						• • •							
1	1	1	1	1	1	1	1	1	1	0	1	4094	
1	1	1	1	1	1	1	1	1	1	1	0	4095	
1	1	1	1	1	1	1	1	1	1	1	1	4096	

(1) If the divider value is Q, then the code will be the binary value of (Q–1).

(2) The frequency applied to the Divider N must be smaller than 250 MHz. A sufficient P Divider must be selected with the FB_MUX to maintain this criteria.

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Output Mode Selection for LVCMOS and LVPECL Outputs: Y0A, Y0B, Y1A ...Y4B (Word 1)⁽¹⁾

	OUTSELx	OUTxB1	OUTxB0	LVCMOS [YxB]	OUTxA1	OUTxA0	LVCMOS [YxA]	Default
LVCMOS	0	0	0	Active	0	0	Active	
	0	0	1	3-state	0	1	3-state	
	0	1	0	Inverting	1	0	Inverting	
	0	1	1	Low	1	1	Low	
	OUTSELx	OUTxB1	OUTxB0		OUTxA1	OUTxA0	LVCMOS [YxA]	Default
LVPECL	1	x	x		x	0	Active	Yx
	1	x	x		x	1	3-state	

(1) If the differential LVPECL output e.g. Y0A:Y0B is selected (bit 2 of word 1), then only bit 7 of word 1 defines the output mode for Y0A:Y0B. The settings of bit 8, bit 9, and bit 10 of word 1 are therefore not relevant to the Y0A:Y0B. This applies for the other LVPECL outputs as well.

Reference Delay M (PRI_REF or SEC_REF) and Feedback Delay N (VCXO) Phase Adjustment (Word 0)⁽¹⁾

DLYM2 / DLYN2	DLYM1 / DLYN1	DLYM0 / DLYN0	Phase Offset	Default
0	0	0	0 ps	Yes
0	0	1	±160 ps	
0	1	0	±320 ps	
0	1	1	±480 ps	
1	0	0	±830 ps	
1	0	1	±1130 ps	
1	1	0	±1450 ps	
1	1	1	±1750 ps	

(1) If Progr. Delay M is set, all Yx outputs are lagging to the reference clock according to the value set. If Progr. Delay N is set; all Yx outputs are leading to the reference clock according to the value set. Above are typical values at $V_{CC} = 3.3\text{ V}$, Temp = 25°C, PECL-output relate to Div4 mode.

PFD Pulse Width Delay (Word 2)

PFD1 ⁽¹⁾	PFD0 ⁽¹⁾	PFD Pulse Width ^{(1) (2)}	Default ⁽¹⁾
0	0	1.5 ns	Yes
0	1	3 ns	
1	0	4.5 ns	
1	1	6 ns	

(1) The PFD pulse width delay gets around the dead zone of the PFD transfer function and reduces phase noise and reference spurs.

(2) Typical values at $V = 3.3\text{ V}_{CC}$, Temp = 25°C .

Lock-Detect Window (Word 3)

LOCKW1	LOCKW0	Phase-Offset at PFD Input ⁽¹⁾	Default
0	0	3.5 ns	
0	1	8.5 ns	Yes
1	0	18.5 ns	
1	1	Cycle slip ⁽²⁾	

(1) Typical Values at $V_{CC} = 3.3\text{ V}$, Temp = 25°C.

(2) Cycle slip occurs when the phase shift at the PFD is greater than one period of the frequency. It is a complete (integer number) cycle jump, i.e., cause by a loss-of-lock of the PLL.

Number of Successive Lock Events Inside the Lock Detect Window (Word 3)

LOCKC1 ⁽¹⁾	LOCKC0 ⁽¹⁾	No. of Successive Lock Events ⁽¹⁾	Default ⁽¹⁾
0	0	1	
0	1	16	
1	0	64	Yes
1	1	256	

(1) This does not apply to Out-of-Lock condition.

Charge Pump Current (Word 2)

CP3	CP2	CP1	CP0	Typical Charge Pump Current	Default
0	0	0	0	0 μ A (3-state)	
0	0	0	1	200 μ A	
0	0	1	0	400 μ A	
0	0	1	1	600 μ A	
0	1	0	0	800 μ A	
0	1	0	1	1 mA	
0	1	1	0	1.2 mA	
0	1	1	1	1.4 mA	
1	0	0	0	1.6 mA	
1	0	0	1	1.8 mA	
1	0	1	0	2.0 mA	Yes
1	0	1	1	2.2 mA	
1	1	0	0	2.4 mA	
1	1	0	1	2.6 mA	
1	1	1	0	2.8 mA	
1	1	1	1	3 mA	

FB_MUX Selection (Word 2)

FBMUX2	FBMUX1	FBMUX0	Selected VC(X)O Signal for the Phase Discriminator	Default
0	0	0	Div by 1	
0	0	1	Div by 2	
0	1	0	Div by 3	
0	1	1	Div by 4	
1	0	0	Div by 6	
1	0	1	Div by 8	Yes
1	1	0	Div by 16 ⁽¹⁾	
1	1	1	Div by 8	

(1) This divider setting depends on the selected P-divider mode for the "Div-by-16" divider. In the default mode (after power up), Div-by-16 is selected. But if bit 30 or bit 31 of word 1 is set to [1], then the Div-by-4 and 90 degree phase shift or Div-by-8 and 90 degree phase shift is selected.

Yx_MUX – Output Divider Selection for Y0, Y1, Y2, Y3, Y4 (Word 2)

YxMUX2	YxMUX1	YxMUX0	Selected Divided V(C)XO Signal for the Yx Outputs	Default
0	0	0	Div by 1	
0	0	1	Div by 2	
0	1	0	Div by 3	
0	1	1	Div by 4	

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YxMUX2	YxMUX1	YxMUX0	Selected Divided V(C)XO Signal for the Yx Outputs	Default
1	0	0	Div by 6	all Yx
1	0	1	Div by 8	
1	1	0	Div by 16 ⁽¹⁾	
1	1	1	Div by 8	

(1) This divider setting depends on the selected P-divider mode for the "Div-by-16" divider. In the default mode (after power up), Div-by-16 is selected. But if bit 30 or bit 31 of word 1 is set to [1], then the Div-by-4 and 90 degree phase shift or Div-by-8 and 90 degree phase shift is selected.

FEATURE DESCRIPTION

Automatic/Manual Reference Clock Switching

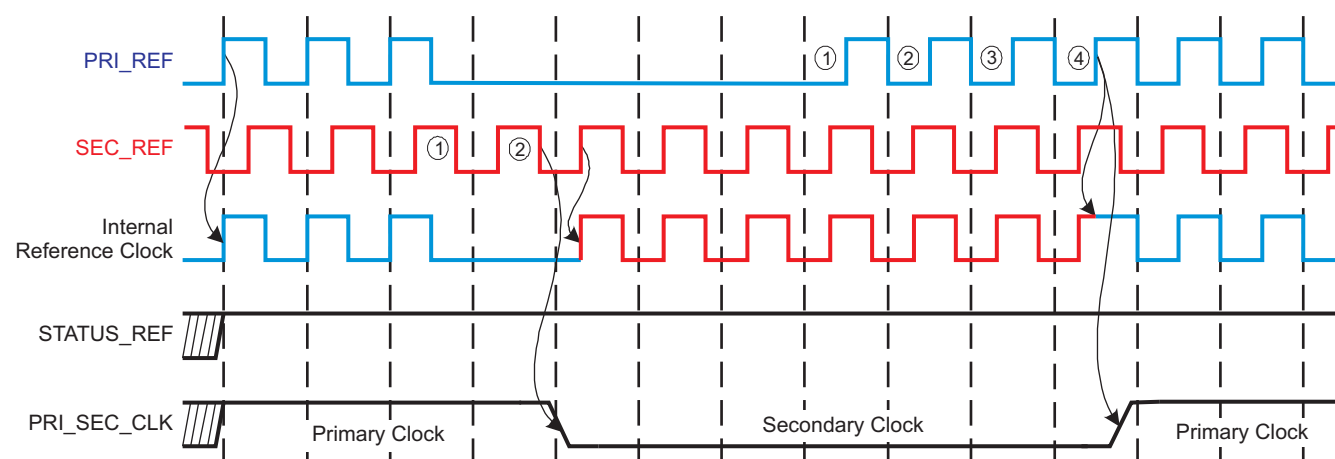
The CDCM7005 supports two reference clock inputs, the primary clock input, PRI_REF, and the secondary clock input, SEC_REF. The clocks can be selected manually or automatically. The respective mode is selected by the dedicated SPI register bit (Word 0, Bit 30).

In the manual mode, the external REF_SEL signal selects one of the two input clocks:

REF_SEL [1] -> primary clock is selected

REF_SEL [0] -> secondary clock is selected

In the automatic mode, the primary clock is selected by default even if both clocks are available. In case the primary clock is not available or fails, then the input switches to the secondary clock as long until the primary clock is back. Figure 16 shows the automatic clock selection.



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NOTE: PRI_REF is the preferred clock input.

Figure 16. Behavior of STATUS_REF and PRI_SEC_CLK

In the automatic mode, the frequencies of both clock signals have to be similar, but may differ by up to 20%. The phase of the clock signal can be any.

The clock input circuitry is design to suppress glitches during switching between the primary and secondary clock in the manual and automatic mode. This avoids an undefined switching of the following circuitries.

The phase of the output clock slowly follows the new input phase. There will be no phase jump at the output. How quick the phase adjustment is done depends on the selected loop parameter, i.e., at a loop bandwidth of <100 Hz; the phase adjustment can take several ms. There is no phase build-out function supported (like in SONET/SDH applications).

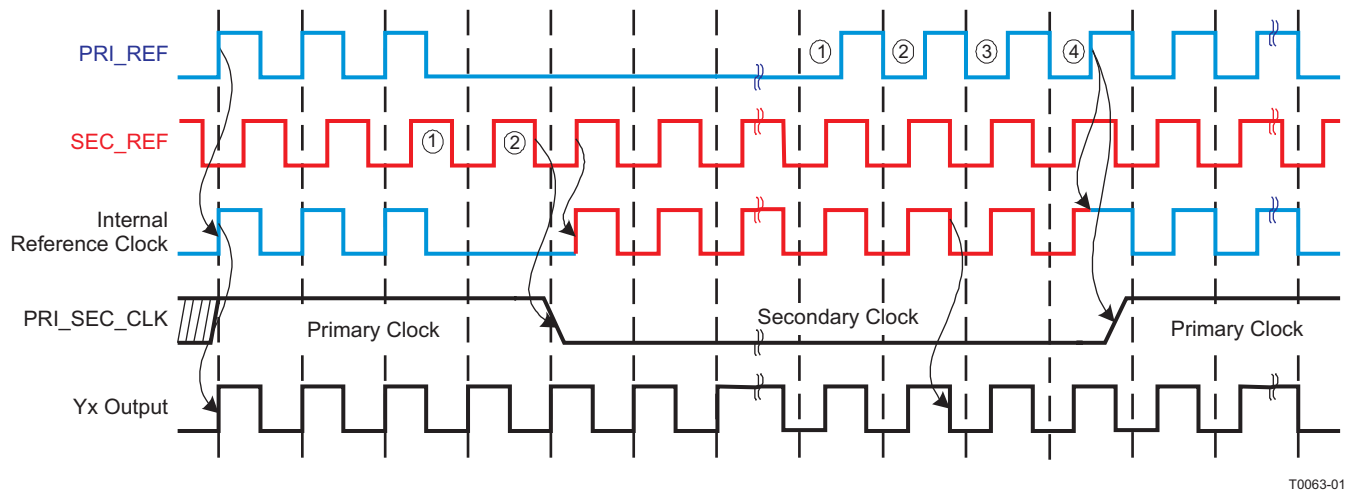


Figure 17. Phase Approach of Output to New Reference Clock

PLL Lock for Analog and Digital Detect

The CDCM7005 supports two PLL lock indications: the digital lock signal or the analog lock signal. Both signals indicate logic high-level at PLL_LOCK if the PLL locks according the selected lock condition.

PLL Lock/Out-of-Lock Definition

The PLL is locked (set high), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD (phase frequency detect) are inside a predefined lock detect window, or if no cycle-slip appears, for a pre-defined number of successive clock cycles.

The PLL is out-of-lock (set low), if the rising edge of the Reference Clock (PRI_REF or SEC_REF clock) and Feedback Clock (VCXO_IN clock) at the PFD are outside the predefined lock detect window or if a cycle-slip appears.

Both, the lock detect window and the number of successive clock cycles are user definable (Word 3, Bit 2-6).

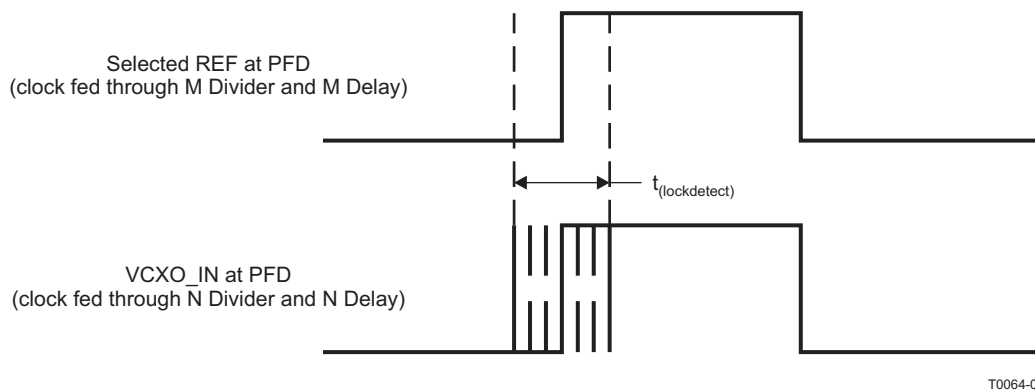


Figure 18. Lock Detect Window

The lock detect window describes the maximum allowed time difference for lock detect between the rising edge of PRI_REF or SEC_REF and VCXO_IN. The time difference is detected at the phase frequency detector. The rising edge of PRI_REF or SEC_REF is taken as reference. The rising edge of VCXO_IN is outside the lock detect window if there is a phase displacement of more than $+0.5 \times t_{(lockdetect)}$ or $-0.5 \times t_{(lockdetect)}$.

Figure 19 and Figure 20 show the circuit for the digital and analog lock. The analog lock operates with an external load capacitor.

When selecting the digital PLL lock option, PLL_LOCK will possibly jitter several times between lock and out of lock until a stable lock is detected. A single low-to-high step can be reached with a wide lock detect window and high number of successive clock cycles. PLL_LOCK returns to out of lock if just one cycle is outside the lock detect window or a cycle slip occurs.



Figure 19. Digital Lock-Detect

When selecting the analog PLL Lock option, the high-pulses load the external capacitor via the internal 110- μ A current source until logic high-level is reached. Therefore, more time is needed to detect logic high level, but jittering of PLL_LOCK will be suppressed in case of digital lock. The time PLL_LOCK needs to return to out of lock depends on the level of $V_{Q_{int}}$, when the current source starts to unload the external capacitor.



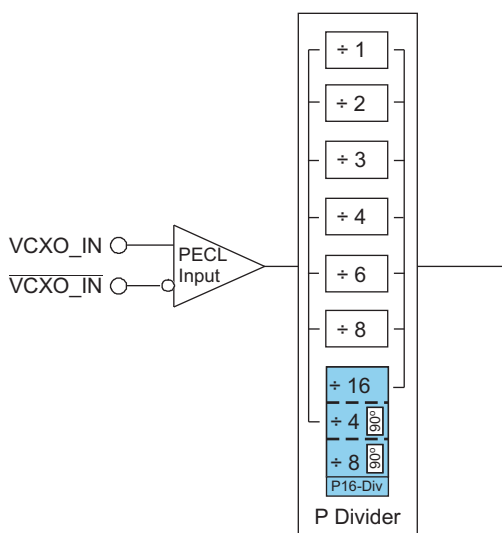
Figure 20. Analog Lock-Detect

Differential LVPECL Outputs and Single-Ended LVCMOS Outputs

The CDCM7005 supports up to 5 × LVPECL outputs or 10 × LVCMOS/LVTTL outputs or any combination of these. The single ended LVCMOS outputs are arranged in pairs which mean both outputs of a LVCMOS pair have the same frequency but can separately be disabled or inverted. The power up output arrangement is five LVPECL (default setting).

The LVPECL outputs are designed to terminate in to a 50-Ω load to $V_{CC} - 2\text{ V}$. The LVCMOS outputs supports the standard LVCMOS load (see Figure 13). The LVPECL and LVCMOS outputs can be enabled (normal operation) or disabled (3-state).

In addition, the output phase can be shifted by 90 degrees when using the additional div-by-4 or div-by-8 mode of the P16-Div (see Figure 21). In the default mode (after power up), the div-by-16 mode of the P16-Div is active. To change it to a 90 degree phase shift, bit 30 or bit 31 of word 1 has to be programmed accordingly. The P 16-Div has to be selected via the dedicated YxMUX to obtain the 90 degree phase shift. The outputs are switched in pairs. When selecting the 90 degree phase shift mode, the div-by-16 functions will no longer be available. The 90 degree phase shifted signal is lagging to the non-shifted signal.



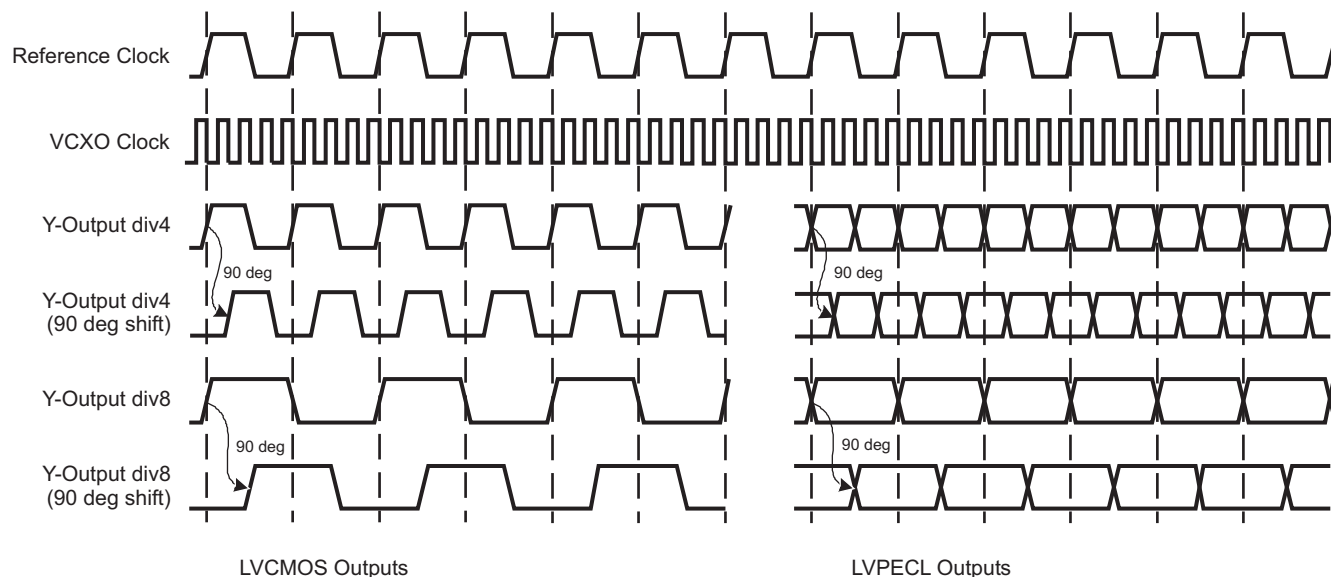
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Figure 21. 90 Degree Phase Shift Option of P-Divider

The following diagram shows the LVCMOS and LVPECL output signal when 90 degree phase shift is on.

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Figure 22. Output Switching Diagram

In addition, the LVCMOS supports disabled-to-low and 180° output phase shift for each output individually. When selecting the 180° phase shift together with the 90° phase shift, the respective outputs has a total phase shift of 270° (see [Table 3](#)).

Table 3. LVCMOS Phase Shift Options

Phase	P-Divider	180°Phase-Shift	P16-Div - Function
0°	Any P-Divider	No	div-by-16
90°	P16-Div	No	div-by-4 or div-by-8
180°	Any P-Divider	Yes	div-by-16
270°	P16-Div	Yes	div-by-4 or div-by-8

If the P16-Div is selected by the FB_MUX and div-by-4 or div-by-8 is active, the 90° phase shifted clock will be synchronized to PRI_REF or SEC_REF. This means all outputs Yxx, which are switched to div-by-4 or div-by-8, are in phase to PRI_REF or SEC_REF. All other outputs are 90° phase shifted with leading phase.

Frequency Hold-Over Mode

The HOLD function is a useful feature which helps the designer to improve the system reliability. The HOLD function holds the output frequency in case the input reference clock fails or is disrupted. During HOLD, the charge pump is switched off (3-state) freezing the last valid output frequency. The hold function will be released after a valid reference clock is back. For proper HOLD function, the analog PLL lock detect mode has to be active.

The following register settings are involved with the HOLD function:

- Lock Detect Window (Word 3, Bit 2, 3, 6):** Defines the window in ns inside the lock is valid. The size is 3.5 ns, 8.5 ns, 18.5 ns, or a complete cycle-slip. Lock is set if reference clock and the feedback clock are inside this predefined lock-detect window for a pre-selected number of successive cycles or if a cycle-slip no longer occurs.
- Out-of-Lock:** Defines the out-of-lock condition: If the reference clock and the feedback clock at the PFD are outside the predefined Lock Detect Window or if a cycle-slip occurs.
- Cycle-Slip (Word 3, Bit 6):** Cycle-slip occurs when the phase shift at the PFD is greater than one period of the frequency. It is a complete (integer number) cycle jump, i.e. caused by an out-of-lock of the PLL. Cycle-slip is equivalent to the PLL pull-in time.
- Number of Clock Cycles (Word 3, Bit 4, 5):** Defines the number of successive PFD cycles which have to

occur inside the lock window to set Lock detect. This applies not for out-of-lock condition.

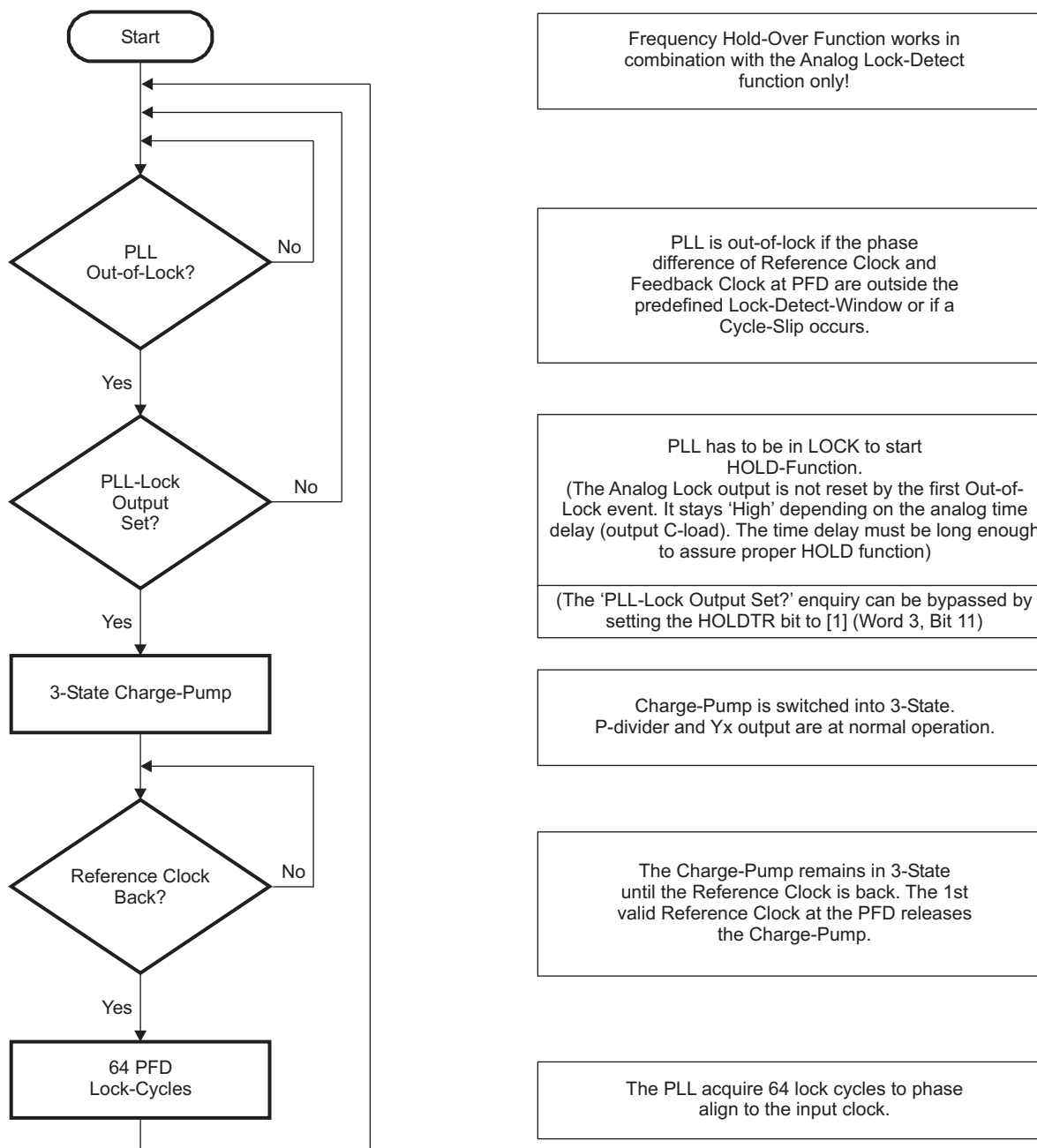
- *Hold-Function (Word 3, Bit 9)*: Selects HOLD function (see more details below).
- *Hold-Trigger (Word 3, Bit 11)*: Defines whether the HOLD function is always activated (Bit 11 = [1]) or whether it is dependent on the state of the analog PLL lock detect output (Bit 11 = [0]). In the latter case, HOLD is activated, if lock is set (high) and de-activated if Lock is reset (low).
- *Analog PLL Lock Detect (Word 1, Bit 29)*: Analog lock output charges or discharges an external capacitor with every valid lock cycle. The time constant for Lock detect can be set by the value of the capacitor.

The CDCM7005 supports two types of HOLD functions, one external controllable $\overline{\text{HOLD}}$ mode and one internal mode, HOLD.

With the *external $\overline{\text{HOLD}}$ function* the charge pump can directly be switched into 3-state (pin 40 can be programmed for HOLD [Word 2, Bit 29]). This function is also available via SPI register (Word 2, Bit 31).

If logic low is applied to the $\overline{\text{HOLD}}$ pin, the charge pump will be switched to 3-state. After the $\overline{\text{HOLD}}$ pin is released, the charge pump is switched back in to normal operation with the next valid reference clock cycle at PRI_REF or SEC_REF and the next valid feedback clock cycle at the PFD. During HOLD, the P divider and all outputs Yx are at normal operation.

HOLD-Over-Function: The PLL has to be in lock to start the HOLD function. It switches the charge pump in to 3-State when an out-of-lock event occurs. It leaves the 3-state charge pump state when the reference clock is back. Then it starts a locking sequence of 64 cycles before it goes back to the beginning of the HOLD-over loop. The dedicated looking sequence and a digital phase alignment enable a fast lock.



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Figure 23. Frequency HOLD-Over Function

Charge Pump Preset to $V_{CC_CP/2}$

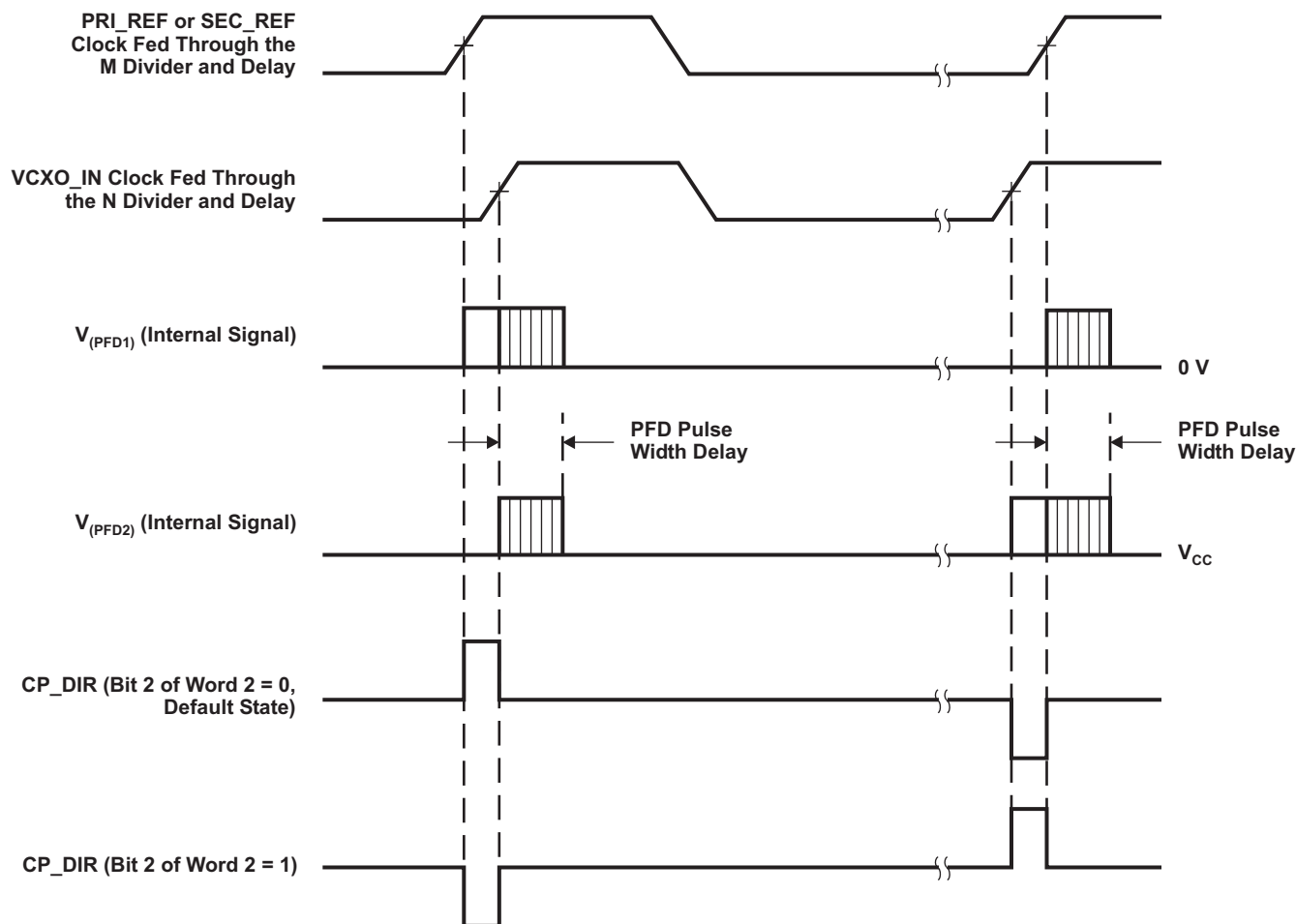
The preset charge pump to $V_{CC_CP/2}$ is a useful feature to quickly set the center frequency of the VC(X)O after powerup or reset. The adequate control voltage for the VC(X)O will be provided to the charge-pump output by an internal voltage divider of 1 k Ω /1 k Ω to V_{CC_CP} and GND ($V_{CC_CP/2}$).

This feature helps to get the initial frequency accuracy, i.e. required at common public radio interface (CPRI) or open base station architecture initiative (OBSAI).

The preset charge pump to $V_{CC_CP/2}$ can be set and reset by SPI register (word 2, bit 3). This feature must be disabled for PLL locking.

Charge Pump Current Direction

The direction of the charge pump (CP) current pulse can be changed by the SPI register (word 2, bit 2). It determines in which direction the CP current regulates (reference clock leads to feedback clock). Most applications use the positive CP output current (power-up condition) because of the use of a passive loop filter. The negative CP current is useful when using an active loop filter concept with inverting operational amplifier. Figure 24 shows the internal PFD signal and the corresponding CP current.



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NOTE: The purpose of the PFD pluse width delay is to improve spurious suppression.

Figure 24. Charge Pump Current Direction (VCXO and VCO Support)

APPLICATION INFORMATION

Phase Noise Reference Circuit

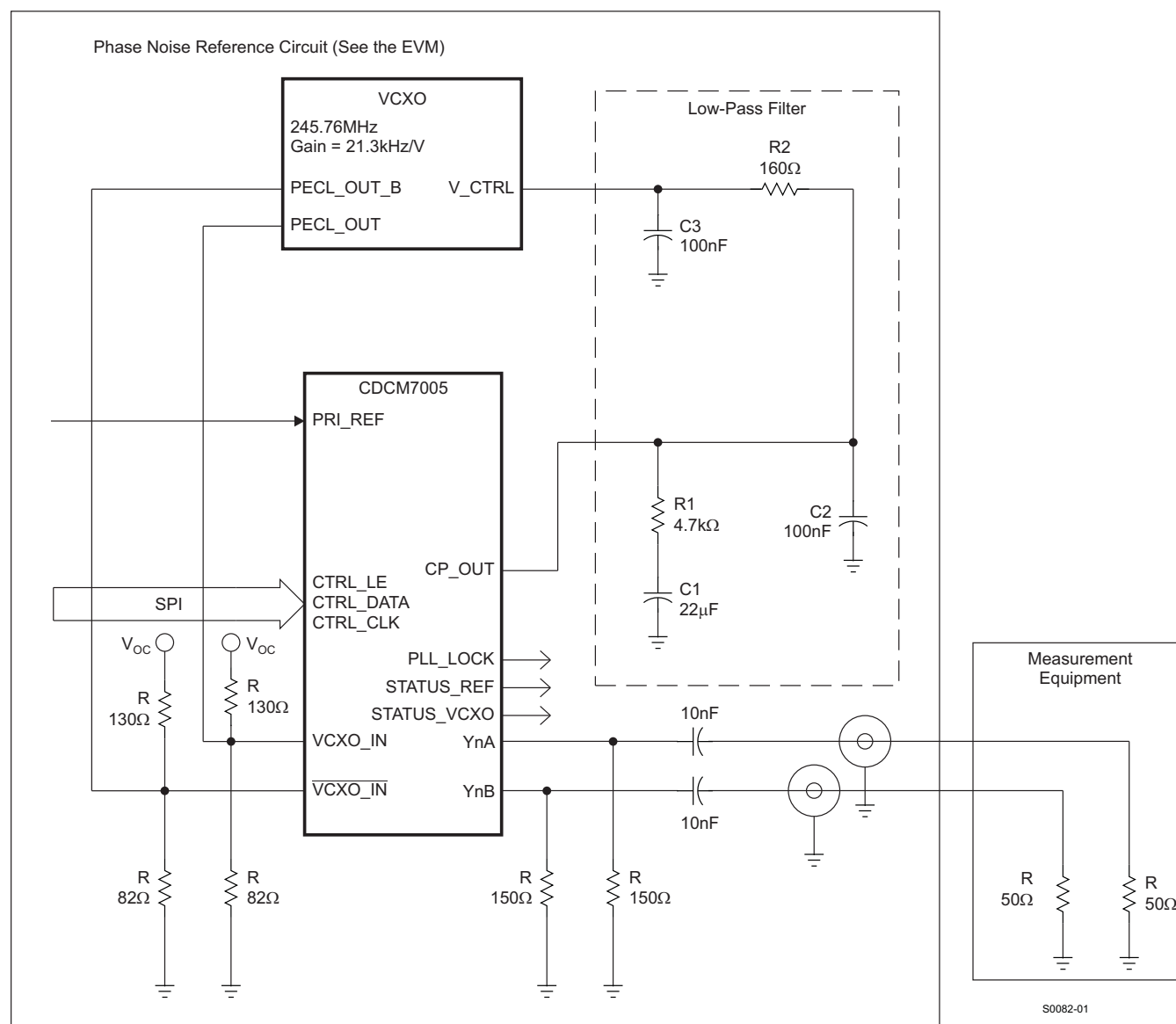


Figure 25. Typical Applications Diagram With Passive Loop Filter

Phase Noise Performance

PARAMETER ⁽¹⁾		TEST CONDITIONS	REF_IN PHASE NOISE AT 30.72 MHz	VCXO PHASE NOISE AT 245.76 MHz	Yx PHASE NOISE AT 30.72 MHz		UNIT
					LVC MOS	LVPECL	
					TYP ⁽²⁾	TYP ⁽²⁾	
phn10	Phase noise at 10 Hz	Y = 30.72 MHz; f _{PFD} = 200 kHz, Loop BW = 20 Hz, Feedback Divider = 8 x 128 (N x P), f _{REF_IN} = 30.72 MHz, M-Divider = 128, I _{CP} = 2 mA	-109	-75	-104	-100	dBc/Hz
phn100	Phase noise at 100 Hz		-125	-97	-116	-116	dBc/Hz
phn1k	Phase noise at 1 kHz		-134	-117	-140	-140	dBc/Hz
phn10k	Phase noise at 10 kHz		-136	-138	-153	-152	dBc/Hz
phn100k	Phase noise at 100 kHz		-138	-148	-156	-153	dBc/Hz
phn1Mk	Phase noise at 1 MHz		-144	-148	-156	-153	dBc/Hz
phn10M	Phase noise at 10 MHz		-144	-148	-156	-153	dBc/Hz
PLL Stabilization Time							
tstabi	PLL stabilization time ⁽³⁾	Y = 30.72 MHz, f _{PFD} = 200 kHz, Loop BW = 20 Hz, Feedback Divider = 8 x 128 (N x P), f _{REF_IN} = 30.72 MHz, M-Divider = 128, I _{CP} = 2 mA			400		ms

- (1) Output phase noise is dependent on the noise of the REF_IN clock and VCXO clock noise floor. The phase noise measurements were taken with the CDCM7005 EVM and CDCM7005 SPI default settings.
- (2) The typical stabilization time is based on the above application example. The stabilization criterion was a stable high level of PLL_LOCK.
- (3) For further explanations, as well as phase noise/jitter test results using various VCXOs, see application note [SCAA067](#).

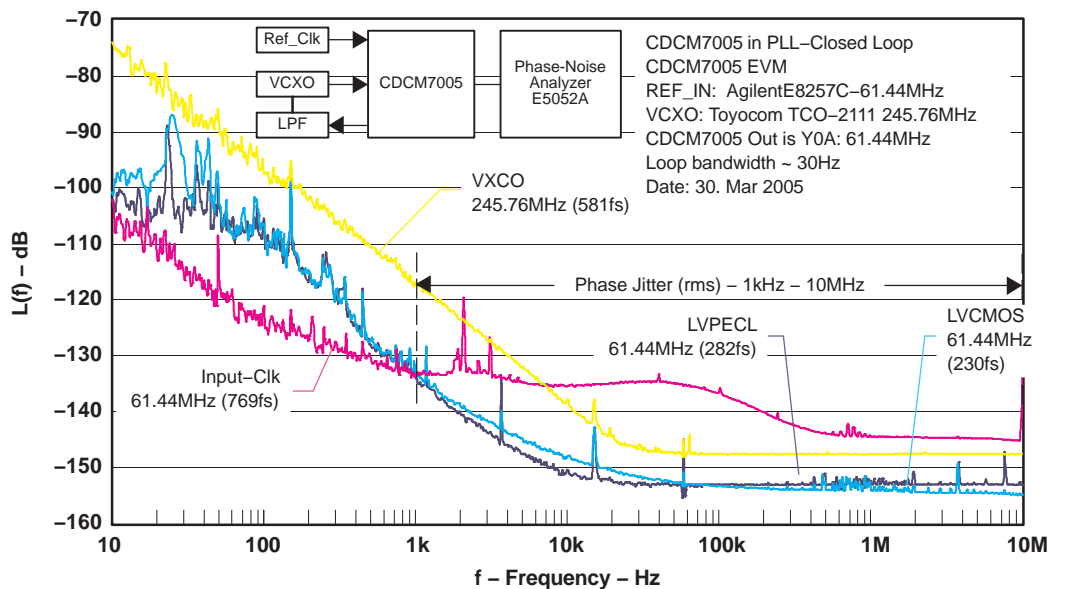


Figure 26. Phase Noise (61.44-MHz REF_IN and 61.44-MHz Output Frequency)

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In-Band Noise Performance

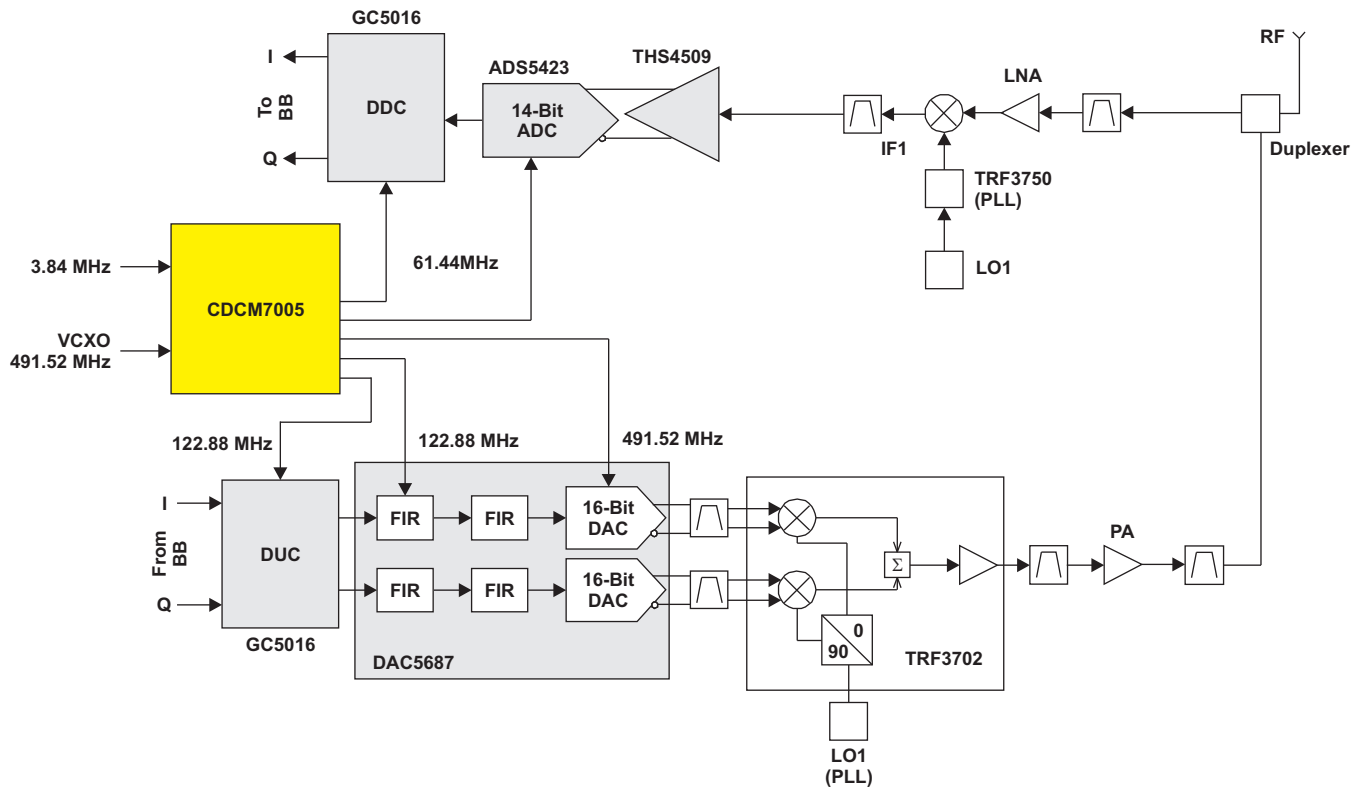
Table 4.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$pn_{in-band}$	In-band phase noise test conditions	Y = 900 MHz, f_{PFD} = 400 kHz, Loop BW = 27 kHz, Feedback Divider = 8 x 282 (N x P), f_{REF_IN} = 10 MHz; M-Divider = 25, I_{CP} = 3 mA		-95		dBc/Hz
pn_{f400}	Phase noise floor at 400 kHz f_{PFD} , in-band noise – 20log(feedback div) ⁽¹⁾			-162		dBc/Hz
pn_{f1}	Phase noise floor at 1 Hz f_{PFD} , in-band noise – 20log(feedback div) – 10log(f_{PFD}) ⁽²⁾			-218		dBc/Hz

- (1) The synthesizer phase noise floor can be estimated by measuring the in-band noise at the output of the CDCM7005 and subtracting 20log(Feedback Divider) N (in case of CDCM7005 it is the N+P divider). The calculated phase noise floor still based on the PFD update frequency, in the above specification, is 400 kHz.
- (2) The in-band noise can also be normalized to a comparison frequency of 1 Hz. The resulting phase noise floor is: $pn_{floor} = PN_{measured} - 20log(N+P) - 10log(f_{PFD})$
where:
 pn_{Nfloor} = normalized phase noise floor in dBc/Hz
 $PN_{measured}$ = in-band phase noise measurement in dBc/Hz
20log(N+P) = divider ratio of feedback loop
10log(f_{PFD}) = PFD update frequency in Hz

APPLICATION INFORMATION ON THE CLOCK GENERATION FOR INTERPOLATING DACS WITH THE CDCM7005

The CDCM7005, with its specified phase noise performance, is an ideal sampling clock generator for high speed ADCs and DACs. The CDCM7005 is especially of interest for the new high speed DACs, which have integrated interpolation filter. Such DACs achieve sampling rates up to 500 MSPS. This high data rate can typically not be supported from the digital side driving the DAC (e.g., DUC, digital up-converter). Therefore, one approach to interface the DUC to the DAC is the integration of an interpolation filter within the DAC to reduce the data rate at the digital input of the DAC. In 3G systems, for example, a common sampling rate of a high speed DAC is 491.52 MSPS. With a four times interpolation of the digital data, the required input data rate results into 122.88 MSPS, which can be supported easily from the digital side. The DUC GC5016, which supports up to four WCDMA carriers, provides a maximum output data rate of 150 MSPS. An example is shown in [Figure 27](#), where the CDCM7005 supplies the clock signal for the DUC/DDC and ADC/DAC.



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Figure 27. CDCM7005 as a Clock Generator for High Speed ADCs and DACs

The generation of the two required clock signals (data input clock, clock for DAC) for such an interpolating DAC can be done in different ways. The recommended way is to use the CDCM7005, which generates the fast sampling clock for the DAC from the data input clock signal. The DAC5687 demands that the edges of the two input clocks must be phase aligned within ± 500 ps for latching the data properly. This phase alignment is well achieved with the CDCM7005, which assures a maximum skew of 70 ps of the different different outputs to each other.

AC-Coupled Interface to ADC/DAC

Another advantage of this clock solution is that the ADC or DAC can be driven directly in an ac-coupling interface as shown in [Figure 28](#), with an external termination in a differential configuration. There is no need for a transformer to generate a differential signal from a single-ended clock source.

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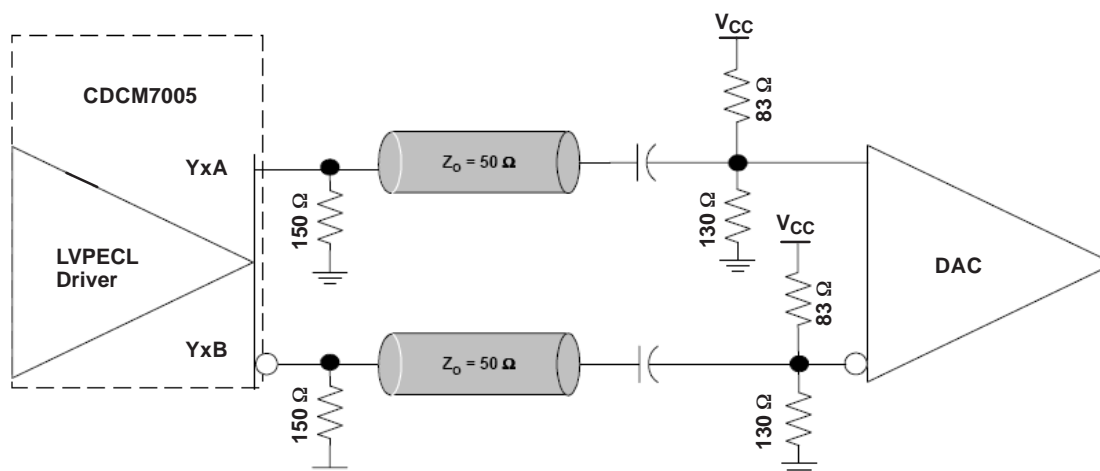


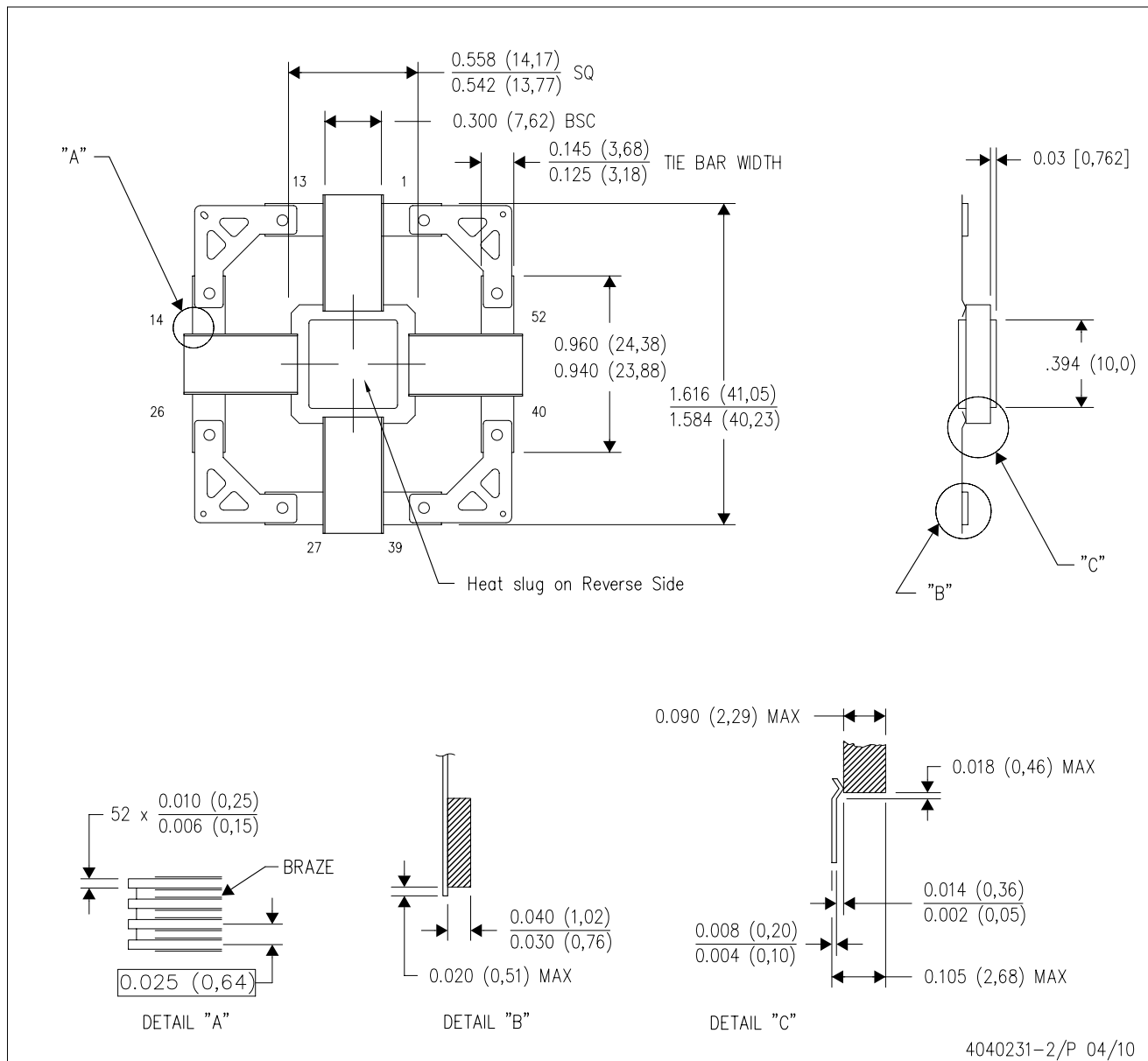
Figure 28. Driving DAC or ADC With PECL Output of the CDCM7005

Changes from Revision B (December 2009) to Revision C
Page

• Changed the VCC pin text - From: There is no internal connection between V_{CC} and AV_{CC} To: V_{CC} and AV_{CC} should always have same supply voltage	4
• Added to the CTRL_LE - Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-k Ω or larger pullup resistor to VCC	4
• Added to the CTRL_CLK pin - Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-k Ω or larger pullup resistor to VCC	4
• Added to the CTRL_DATA pin - Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-k Ω or larger pullup resistor to VCC	4
• Added to the PD pin text - It is recommended to ramp up the... ..	4
• Added to the SPI CONTROL INTERFACE section - Unused or floating inputs must be tied to proper logic level. It is recommended to use a 20-k Ω or larger pullup resistor to VCC	13
• Added to the SPI CONTROL INTERFACE section - It is recommended to program Word 0, Word 1, Word 2 and Word 3 right after power up and PD becomes HIGH	14
• Changed bit 16 from RES to GTME	18
• Changed bit 28 from RES to PFD FC	18

HFG (S-CQFP-F52)

CERAMIC QUAD FLATPACK WITH NCTB



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
 - This package is hermetically sealed with a metal lid.
 - The leads are gold plated and can be solderdipped.
 - Leads not shown for clarity purposes.
 - Lid and heat sink are connected to GND leads.

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