

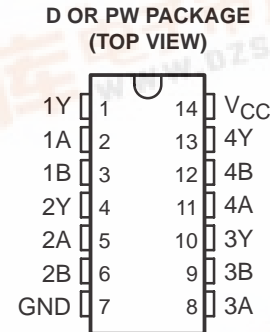
SN74HC02-EP QUADRUPLE 2-INPUT POSITIVE-NOR GATE

查询"SN74HC02-EP"供应商

SCLS478A – APRIL 2003 – REVISED JANUARY 2004

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of Up To –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **2-V to 6-V V_{CC} Operation**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 8 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



description/ordering information

The SN74HC02 contains four independent 2-input NOR gates. It performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

ORDERING INFORMATION

| T _A | PACKAGE‡ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------|---------------|-----------------------|------------------|
| –40°C to 125°C | TSSOP – PW | Tape and reel | SN74HC02QPWREP | SHC02EP |
| –55°C to 125°C | SOIC – D | Tape and reel | SN74HC02MDREP | HC02MEP |

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each gate)

| INPUTS | | OUTPUT |
|--------|---|--------|
| A | B | Y |
| H | X | L |
| X | H | L |
| L | L | H |

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN74HC02-EP

QUADRUPLE 2-INPUT POSITIVE-NOR GATE

SCL9999 "SN74HC02-EP" V1.0P1 4/11/2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage range, V_{CC} | –0.5 V to 7 V |
| Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | ±20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | ±20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ±25 mA |
| Continuous current through V_{CC} or GND | ±50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): D package | 86°C/W |
| PW package | 113°C/W |
| Storage temperature range, T_{stg} | –65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

| | | MIN | NOM | MAX | UNIT |
|---------------------|---------------------------------|------------------|------|----------|------|
| V_{CC} | Supply voltage | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | |
| | | $V_{CC} = 6$ V | 4.2 | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | |
| | | $V_{CC} = 6$ V | | 1.8 | |
| V_I | Input voltage | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 2$ V | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | 500 | |
| | | $V_{CC} = 6$ V | | 400 | |
| T_A | Operating free-air temperature | Q-suffix device | –40 | 125 | °C |
| | | M-suffix device | –55 | 125 | |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN74HC02-EP QUADRUPLE 2-INPUT POSITIVE-NOR GATE

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----|-------|------|
| | | | | MIN | TYP | MAX | | | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | |
| | | I _{OH} = -4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | |
| | | I _{OH} = -5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 2 | | 40 | µA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | pF |

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | MIN | MAX | UNIT |
|-----------------|--------------|-------------|-----------------|-----------------------|-----|-----|-----|-----|------|
| | | | | MIN | TYP | MAX | | | |
| t _{pd} | A or B | Y | 2 V | | 45 | 90 | | 135 | ns |
| | | | 4.5 V | | 9 | 18 | | 27 | |
| | | | 6 V | | 8 | 15 | | 23 | |
| t _t | | Y | 2 V | | 38 | 75 | | 110 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | |
| | | | 6 V | | 6 | 13 | | 19 | |

operating characteristics, T_A = 25°C

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------|-----|------|
| C _{pd} Power dissipation capacitance per gate | No load | 22 | pF |

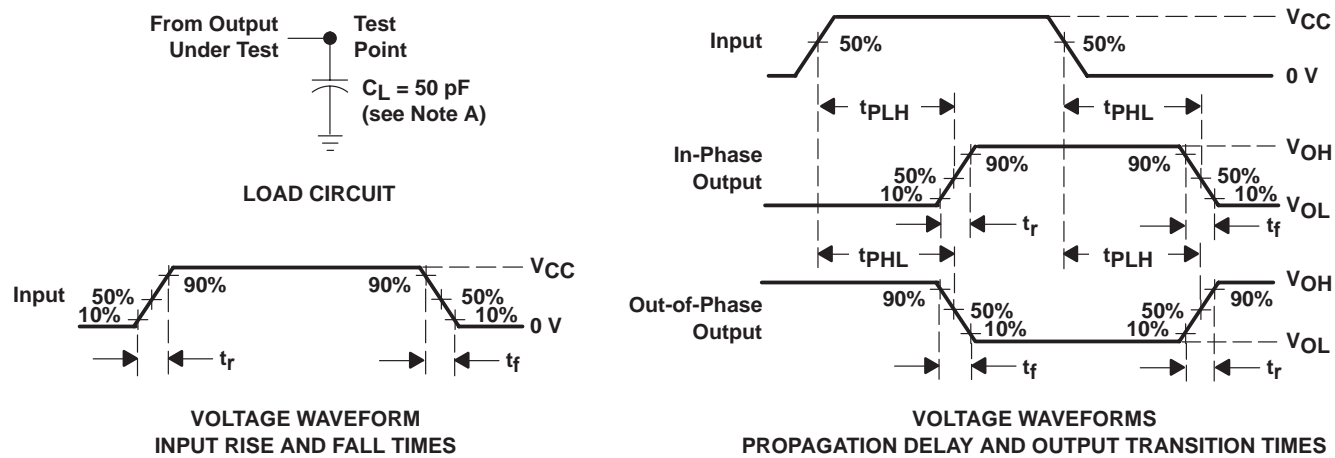


SN74HC02-EP
QUADRUPL 2-INPUT POSITIVE-NOR GATE

SCL95951 "SN74HC02-EP" 2004

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74HC02QPWREP | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/04687-02YE | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [SN74HC02](#)
- Automotive: [SN74HC02-Q1](#)
- Military: [SN54HC02](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC02QPWREP | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC02QPWREP | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |

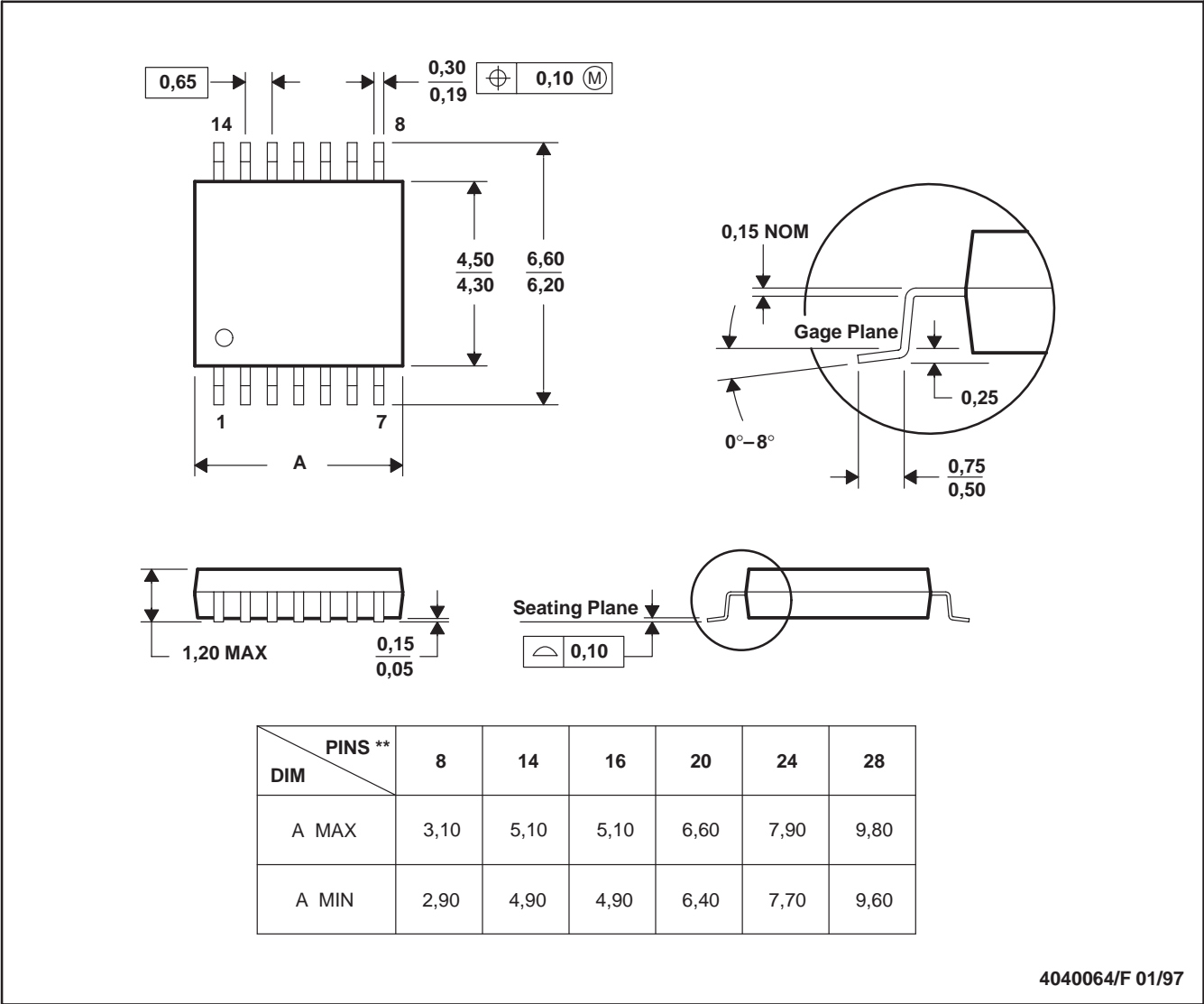
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MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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