Bipolar Integrated Technology Inc.

查询"B3060"供应商

Product Brief

B3060
Digital Correlator

Introduction:

The B3060 is a flexible, high-speed, 1024-bit digital-correlation circuit. It can be user configured in 4x256x1, 2x512x1 or 1x1024x1 bit modes.

Differential I/O is used on all signals for maximum signal integrity in demanding environments. Inputs and outputs can be used single-ended in applications requiring less demanding environments.

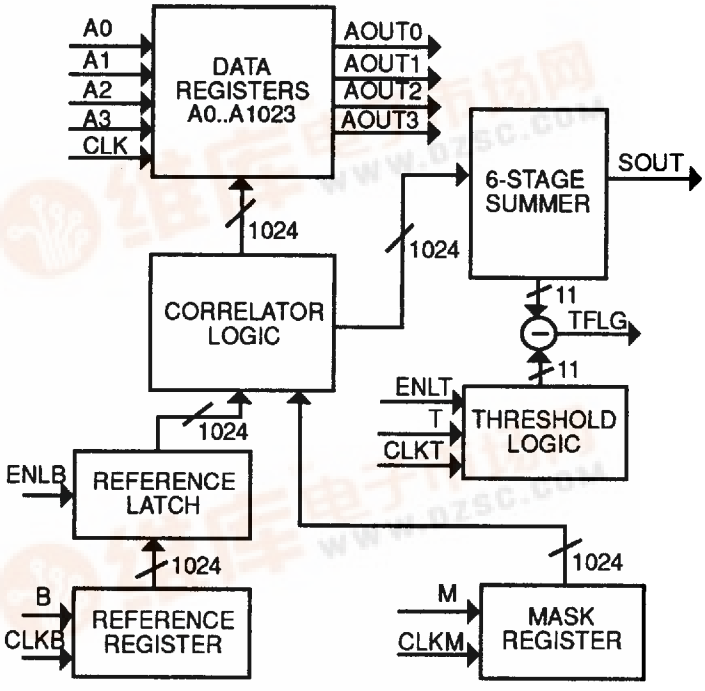
Digital correlation is performed on a serially-shifted data stream A against a serially-shifted reference pattern B, latched in the pattern latch L. The bit-wise mask M allows selectable comparisons for every bit position and provides flexible word lengths.

The correlation count output, SOUT, is computed every cycle. The correlation count is the sum of all bits which have their mask bit set and whose data and pattern latch bits match. A flag output, TFLG, is asserted for each cycle in which the correlation count output is greater than or equal to the threshold latch value.

The data shift registers are divided into four 256-bit sections, but can be configured as two 512-bit sections or one 1024-bit shift register. The B and M shift registers are 1024 bits in length and match the A shift register bit-for-bit in the 1x1024x1 mode.

Features:

- 150 MHz correlation rate (worst case)
- Data stream shift registers configurable as 4x256, 2x512 or 1x1024
- Independent clocking of data stream, pattern reference, bit mask, and threshold
- Programmable data word length
- Differential 10KH ECL I/O
- Configurable for single-ended operation
- Fully digital
- Single -5.2v supply
- Military temperature range operation, -55 to +125 °C
- 84-pin hermetic ceramic quad flat-pack suitable for surface mounting



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Signal Descriptions:

A0..A3	Data input for serial shift registers.
B	Serial pattern-to-match input. The value of this 1024-bit shift register is transferred to the compare latch when ENLB is asserted. Bit 0 matches A0, bit 0; bit 256 matches A1, bit 0; etc.
M	Serial mask input. This register is used to mask bits to prevent them from adding to the correlation count. Bit 0 matches A0, bit 0; bit 256 matches A1, bit 0; etc. The mask bit is set (1) for all bits that are to be used for the correlation and reset for all bits that are to be ignored during correlation.
T	11-bit serial threshold input. After being loaded, the threshold value can be transferred to the threshold latch by asserting ENLT.
CLK	Data shift register, summation pipeline, and output register clock.
CLKB	Pattern-to-match register clock.
CLKM	Mask shift register clock.
CLKT	Threshold register clock.
ENLB	Pattern-to-match latch enable.
ENLT	Threshold latch enable.
AOUT0..AOUT3	Data output for data shift registers.
BOUT	Serial data output for pattern-to-match register.
MOUT	Serial data output for mask register.
SOUT	Eleven-bit correlation sum output.
TFLG	Threshold flag output. Asserted if the correlation sum is greater-than-or-equal-to the threshold latch value.

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