

NPe405H

Data Sheet

PowerNP NPe405H Embedded Processor

FEATURES

- PowerNP™ technology using an AMCC PowerPC® 405 32-bit RISC processor core operating up to 266 MHz
- PC-133 synchronous DRAM (SDRAM) interface
 - 32-bit interface for non-ECC applications
 - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External bus for peripheral devices
 - Flash and ROM interface
 - Direct support for 8-, or 16-, or 32-bit SRAM and external peripherals
 - Up to 8 devices
 - External mastering supported
- DMA support for external peripherals, internal UARTs and memory
 - Scatter-gather chaining supported
 - Four channels
- PCI Revision 2.2 compliant interface (32-bit, up to 66MHz)
 - Asynchronous PCI bus interface
 - Internal PCI bus arbiter which can be disabled for use with an external arbiter
- Four 10/100 Ethernet MACs supporting up to four external PHYs via MII, RMII, or SMII interfaces
- HDLC interface with 32 channels through two ports at up to 4.096 Mbps each or 8.192 Mbps for a single port
- HDLC interface with 8 channels through 8 ports at 2.048 Mbps maximum
- Programmable interrupt controller
 - Seven external and 49 internal
 - Edge triggered or level-sensitive
 - Positive or negative active
 - Non-critical or critical interrupt to processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector
- Programmable timers
- Two serial ports (16550 compatible UART)
- One IIC interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal processor local bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory
- User accessible performance counters

DESCRIPTION

Designed specifically to address embedded applications, the NPe405H provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus bridge, Ethernet EMACs, HDLC controllers, external bus controller for ROM, Flash, and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: CMOS SA-12E 0.25 μm (0.18 μm L_{eff})

Package: 35mm, 580-ball enhanced plastic ball grid array (E-PBGA)

Power (typical): 2.3W at 133MHz, 2.9W at 200MHz, 3.4W at 266MHz

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ORDERING, PVR, AND JTAG INFORMATION

| Product Name | Order Part Number ¹ | Processor Frequency | Package | Rev Level | PVR Value | JTAG ID |
|--------------|--------------------------------|---------------------|------------------|-----------|------------|------------|
| NPe405H | NPe405H-3BA133C | 133MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |
| NPe405H | NPe405H-3BA133CZ | 133MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |
| NPe405H | NPe405H-3BA200C | 200MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |
| NPe405H | NPe405H-3BA200CZ | 200MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |
| NPe405H | NPe405H-3BA266C | 266MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |
| NPe405H | NPe405H-3BA266CZ | 266MHz | 35mm, 580 E-PBGA | A | 0x41410140 | 0x04267049 |

Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.

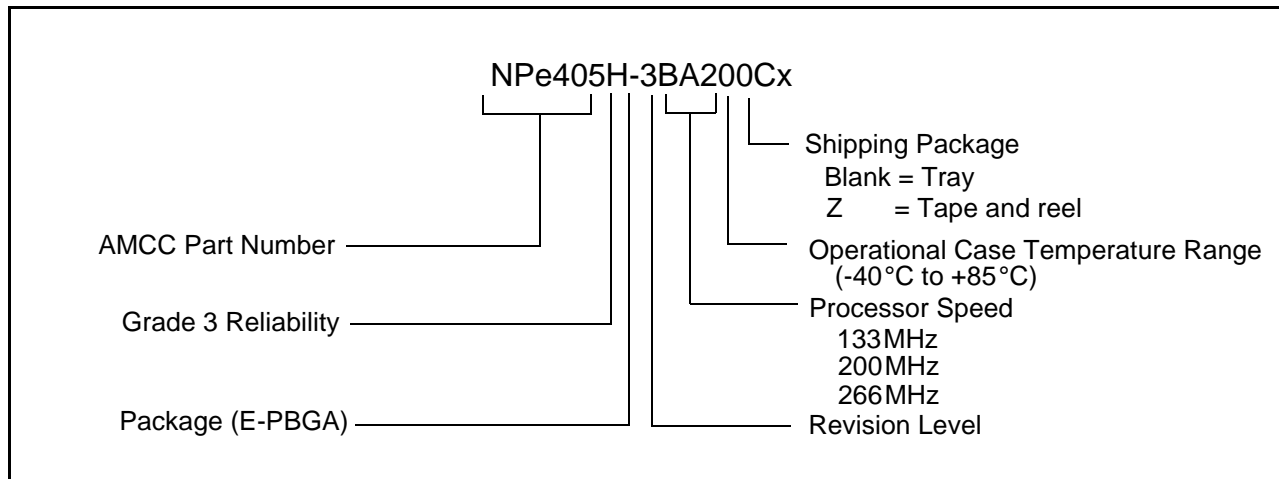
This section provides the part numbering nomenclature for the NPe405H. For availability, contact your local AMCC sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

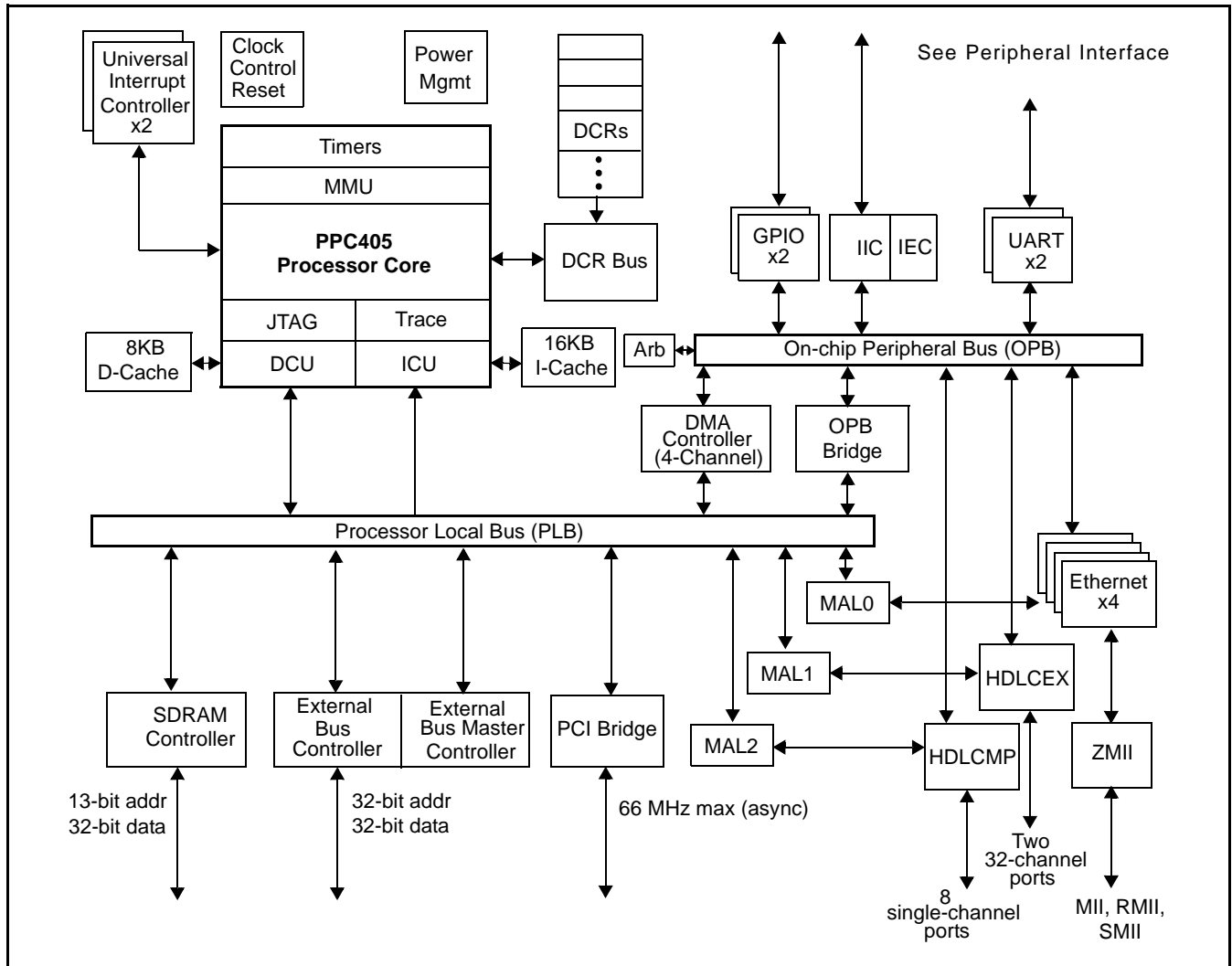
The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the NPe405H User’s Manual for details on the register content.

AMCC Part Number Key



NPE405H EMBEDDED CONTROLLER FUNCTIONAL BLOCK DIAGRAM

Figure 1. NPe405H Embedded Controller Functional Block Diagram



The NPe405H is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated to create an application-specific ASIC product. This approach provides a consistent way to generate complex ASICs using IBM CoreConnect™ Bus Architecture.

ADDRESS MAP SUPPORT

The NPe405H incorporates two separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCRs). The DCRs are accessed by software running on the NPe405H processor through the use of **mtdcr** and **mfdcr** commands.

SYSTEM ADDRESS MAP

Table 1. System Address Map 4GB Total System Memory

| Function | Subfunction | Start Address | End Address | Size |
|----------------------|--|---------------|-------------|--------|
| General use | SDRAM, External peripherals, and PCI memory Note: Any of the address ranges listed at right may be use for any of the above functions. | 0x00000000 | 0xE7FFFFFF | 3712MB |
| | | 0xE8010000 | 0xE87FFFFFF | 8MB |
| | | 0xEC000000 | 0xEEBFFFFFF | 44MB |
| | | 0xEEE00000 | 0xEF3FFFFFF | 6MB |
| | | 0xEF500000 | 0xEF5FFFFFF | 1MB |
| Boot-up | External peripheral bus boot ¹ | 0xFFE00000 | 0xFFFFFFFF | 2MB |
| | PCI boot ² | 0xFFFE0000 | 0xFFFFFFFF | 128KB |
| PCI | PCI I/O | 0xE8000000 | 0xE800FFFF | 64KB |
| | PCI I/O | 0xE8800000 | 0xEBFFFFFF | 56MB |
| | Configuration registers | 0xEEC00000 | 0xEEC00007 | 8B |
| | Interrupt Acknowledge and special cycle | 0xEED00000 | 0xEED00003 | 4B |
| | Local configuration registers | 0xEF400000 | 0xEF40003F | 64B |
| Internal peripherals | UART0 | 0xEF600300 | 0xEF600307 | 8B |
| | UART1 | 0xEF600400 | 0xEF600407 | 8B |
| | IIC0 | 0xEF600500 | 0xEF60051F | 32B |
| | OPB arbiter | 0xEF600600 | 0xEF60063F | 64B |
| | GPIO0 controller registers | 0xEF600700 | 0xEF60077F | 128B |
| | GPIO1 controller registers | 0xEF600780 | 0xEF6007FF | 128B |
| | Ethernet MAC 0 registers | 0xEF600800 | 0xEF6008FF | 256B |
| | Ethernet MAC 1 registers | 0xEF600900 | 0xEF6009FF | 256B |
| | Ethernet MAC 2 registers | 0xEF600A00 | 0xEF600AFF | 256B |
| | Ethernet MAC 3 registers | 0xEF600B00 | 0xEF600BFF | 256B |
| | ZMII control registers | 0xEF600C10 | 0xEF600C1F | 16B |
| | HDLCEX | 0xEF610000 | 0xEF61FFFF | 64KB |
| | HDLCMP | 0xEF620000 | 0xEF62FFFF | 64KB |

Notes:

1. When external peripheral bus boot is selected, peripheral bank 0 is automatically configured at reset to the address range listed above.
2. If PCI boot is selected, a PLB-to-PCI mapping is automatically configured at reset to the address range listed above.
3. After the boot process, software may reassign the boot memory regions for other uses.
4. All address ranges not listed above are reserved.

DCR ADDRESS MAP

Table 2. DCR Address Map 4KB Device Configuration Register

| Function | Start | End | Size |
|-----------------------------------|-------|-------|------------------------|
| DCR address space ¹ | 0x000 | 0x3FF | 1KW (4KB) ¹ |
| Reserved | 0x000 | 0x00F | 16W |
| Memory controller registers | 0x010 | 0x011 | 2W |
| External bus controller registers | 0x012 | 0x013 | 2W |
| Reserved | 0x014 | 0x07F | 108W |
| PLB registers | 0x080 | 0x08F | 16W |
| Performance counters | 0x090 | 0x091 | 2W |
| Reserved | 0x092 | 0x09F | 14W |
| OPB bridge-out registers | 0x0A0 | 0x0A7 | 8W |
| Reserved | 0x0A8 | 0x0AF | 8W |
| Clock, control and reset | 0x0B0 | 0x0B7 | 8W |
| Power management | 0x0B8 | 0x0BF | 8W |
| Interrupt controller 0 | 0x0C0 | 0x0CF | 16W |
| Interrupt controller 1 | 0x0D0 | 0x0DF | 16W |
| Reserved | 0x0E0 | 0x0EF | 16W |
| Miscellaneous | 0x0F0 | 0x0FF | 16W |
| DMA controller registers | 0x100 | 0x13F | 64W |
| Reserved | 0x140 | 0x17F | 64W |
| MAL0 registers (Ethernet) | 0x180 | 0x1FF | 128W |
| MAL1 registers (HDLCEX) | 0x200 | 0x27F | 128W |
| MAL2 registers (HDLCMP) | 0x280 | 0x2FF | 128W |
| Reserved | 0x300 | 0x3FF | 256W |

Notes:

- DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

PLB TO PCI BRIDGE

The PLB to PCI bridge provides a mechanism for connecting PCI devices to the processor, peripherals, and memory. This interface is PCI Specification rev 2.2 compliant.

Features include:

- Internal PCI bus arbiter for up to six external devices at PCI bus speeds up to 66MHz. Internal arbiter use is optional and can be disabled for systems which employ an external arbiter.
- PCI bus frequency up to 66MHz
 - Asynchronous operation from 1/8 PLB frequency to 66MHz maximum
- 32-bit PCI Address/Data Bus
- Power Management:
 - PCI Bus Power Management v1.1 compliant
- Buffering between PLB and PCI:
 - PCI Target 64-byte write post buffer
 - PCI Target 96-byte read prefetch buffer
 - PLB Slave 32-byte write post buffer
 - PLB Slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI Target side configuration
- Supports processor access to all PCI address spaces:
 - Single-byte PCI I/O reads and writes
 - PCI memory single-beat and prefetch-burst reads and single-beat writes
 - Single-byte PCI configuration reads and writes (type 0 and type 1)
 - PCI interrupt acknowledge
 - PCI special cycle
- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM MEMORY CONTROLLER

The NPe405H Memory Controller provides a low latency access path to SDRAM memory. The memory controller supports four logical banks. Up to 256MB per bank are supported, for a maximum of 1 GB total. Memory access and refresh timing, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 row-column address modes (2- and 4-bank devices supported)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address range for each bank of memory
 - 4GB address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- 200 MHz NPe405H supports up to 100 MHz memory with PC100 support
- 266 MHz NPe405H supports up to 133 MHz memory with PC133 support
- 4MB to 256MB per bank
- Programmable timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
 - Standard single error correct, double error detect coverage
 - Aligned nibble error detect
 - Address error logging

EXTERNAL BUS CONTROLLER (EBC)

- Supports eight ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 66.66MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous
- Programmable 2K clock-cycle time-out counter with disable for Ready
- Programmable access timing per device
 - 0–255 wait states for non-bursting devices
 - 0 –31 Burst Wait States for first access and up to 7 Wait States for subsequent accesses
 - Programmable chip select assertion/negation relative to driving address bus
 - Programmable output and write-enable assertion/negation relative to assertion of chip select
- Programmable address mapping
- Peripheral device wait via "Ready"
- External master interface
 - Write posting from external master
 - Read prefetching on PLB for external master reads
 - Bursting capable from external master
 - Allows external master access to all non-EBC PLB slaves
 - External master can control EBC slaves for own access and control

DMA CONTROLLER

- Supports the following transfers:
 - Memory-to-memory transfers
 - Buffered peripheral to memory transfers
 - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external bus attached)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

SERIAL INTERFACE

- Two 8-pin UART interfaces provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC BUS INTERFACE

- Compliant with Phillips® Semiconductors I²C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

IIC EEPROM CONTROLLER

Supports setting of processor configuration from serial EEPROM during system reset.

HDLCEX INTERFACE

- 32-channel HDLC controller
- Two full-duplex Pulse Code Modulation (PCM) Highway ports at speeds up to 4.096 Mbps per port or 8.192 Mbps when using a single port
- Supports HDLC protocol as well as a Transparent mode
- For a single channel per port, autonomous management of I-Frames and S-Frames of the Normal Response mode (NRM) protocol on one channel per port. U-frames are handled by software.
- Supports software emulation of NRM on all channels

HDLCMP INTERFACE

- HDLC controller provides eight full-duplex serial ports
- Up to 2.048Mbps data rate
- Supports HDLC protocol as well as a Transparent mode
- Software emulation of NRM

GENERAL PURPOSE IO (GPIO) CONTROLLER

- Two GPIO controllers
 - 32-signal system GPIO (GPIO0)
 - 32-signal communications GPIO (GPIO1)
- Most GPIOs are pin-shared with other functions. Configuration registers are provided to determine whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. Both GPIO functions have 32 I/Os.
- Each GPIO output is separately programmable to emulate an open-drain driver (drives to zero, three-stated if output bit is 1)

UNIVERSAL INTERRUPT CONTROLLER (UIC)

Two cascaded Universal Interrupt Controllers (UICs) provide the control, status, and communications necessary for the interrupt sources and the PowerPC processor.

Features include:

- Seven external and 49 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Selectable non-critical or critical interrupt requests to the PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector generation for reduced latency interrupt handling

10/100 MBPS ETHERNET MAC

- Four units capable of full- and half-duplex, 10 Mbps or 100 Mbps operation
- Integrated ZMII Bridge supports use of MII, SMII or RMII connections to external PHYs (PHYs not included on chip)
 - Reduced Media Independent Interface (RMII) or Serial Media Independent Interface (SMII) for one to four PHY applications
 - Media Independent Interface (MII) for single or dual PHY applications
- Dedicated media access layer (MAL) provides DMA support

JTAG

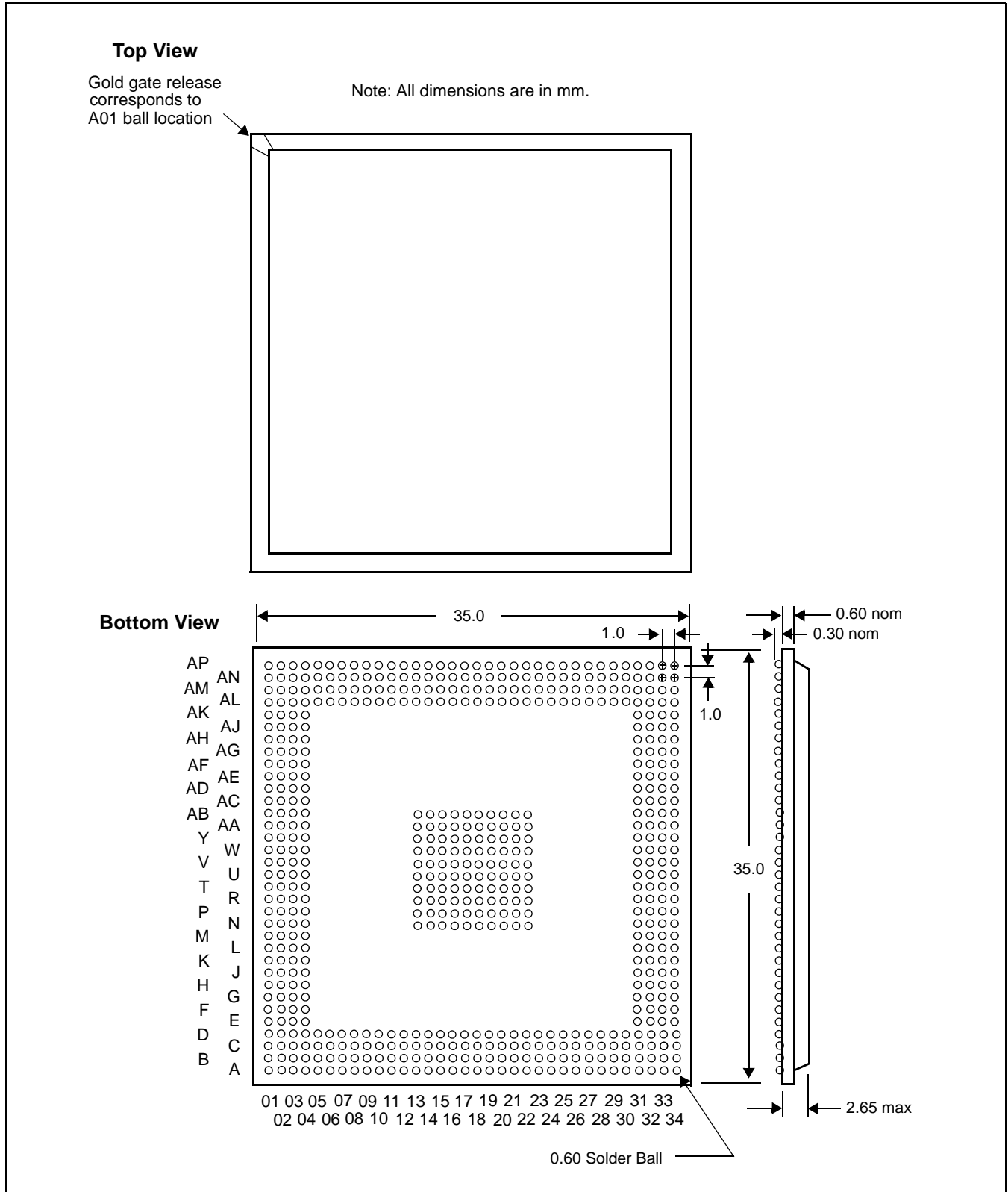
- IEEE 1149.1 Test Access Port
- Debugger support
- JTAG boundary scan support (BSDL file available)

PERFORMANCE COUNTERS

A series of software accessible PLB transaction event counters that can be used to analyze PLB performance.

35 MM, 580-BALL E-PBGA PACKAGE

Figure 2. 35mm, 580-Ball E-PBGA Package



SIGNAL LISTS

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal or signals in brackets. Multiplexed signals appear alphabetically multiple times in the list—once for each signal name on the ball. The page number listed gives the page in “Signal Functional Description” on page 43 where the signals in the indicated interface group begin.

SIGNALS LISTED ALPHABETICALLY

Table 3. Signals Listed Alphabetically (Sheet 1 of 17)

| Signal Name | Ball | Interface Group | Page |
|--|------|--------------------------------|------|
| AV _{DD} | P31 | Power | 51 |
| BA0 | AN31 | SDRAM | 46 |
| BA1 | AM31 | | |
| $\overline{\text{BankSel0}}$ | AL21 | SDRAM | 46 |
| $\overline{\text{BankSel1}}$ | AP23 | | |
| $\overline{\text{BankSel2}}$ | AM22 | | |
| $\overline{\text{BankSel3}}$ | AN23 | | |
| $[\overline{\text{BE0}}]\text{PCIC0}$ | D01 | PCI | 43 |
| $[\overline{\text{BE1}}]\text{PCIC1}$ | B06 | | |
| $[\overline{\text{BE2}}]\text{PCIC2}$ | B10 | | |
| $[\overline{\text{BE3}}]\text{PCIC3}$ | C15 | | |
| BusReq | H03 | External Master Peripheral Bus | 49 |
| $\overline{\text{CAS}}$ | AN22 | SDRAM | 46 |
| ClkEn0 | AP21 | SDRAM | 46 |
| ClkEn1 | AN21 | | |
| $[\overline{\text{DMAAck0}}]\text{GPIO0_13}$ | AB34 | External Slave Peripheral Bus | 47 |
| $[\overline{\text{DMAAck1}}]\text{GPIO0_14}$ | AB33 | | |
| $[\overline{\text{DMAAck2}}]\text{GPIO0_15}$ | AA31 | | |
| $[\overline{\text{DMAAck3}}]\text{GPIO0_16}[\text{PerCS5}]$ | AC34 | | |
| $[\overline{\text{DMAReq0}}]\text{GPIO0_09}$ | AA34 | External Slave Peripheral Bus | 47 |
| $[\overline{\text{DMAReq1}}]\text{GPIO0_10}$ | W32 | | |
| $[\overline{\text{DMAReq2}}]\text{GPIO0_11}$ | AA33 | | |
| $[\overline{\text{DMAReq3}}]\text{GPIO0_12}[\text{PerCS4}]$ | AA32 | | |
| DQM0 | AN20 | SDRAM | 46 |
| DQM1 | AN15 | | |
| DQM2 | AP12 | | |
| DQM3 | AN09 | | |
| DQM _{CB} | AM20 | SDRAM | 46 |
| ECC0 | AP24 | SDRAM | 46 |
| ECC1 | AN24 | | |
| ECC2 | AM24 | | |
| ECC3 | AN25 | | |
| ECC4 | AP26 | | |
| ECC5 | AM25 | | |
| ECC6 | AN26 | | |
| ECC7 | AL25 | | |
| EMC0MDCIk | C21 | Ethernet | 44 |

Table 3. Signals Listed Alphabetically (Sheet 2 of 17)

| Signal Name | Ball | Interface Group | Page |
|---|------|--------------------------------|------|
| EMC0MDIO | B21 | Ethernet | 44 |
| [EMC0Sync]EMC0TxEn[EMC0Tx0En] | D21 | Ethernet | 44 |
| EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] | A24 | Ethernet | 44 |
| EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] | B23 | | |
| EMC0TxD2[EMC0Tx1D0][EMC0Tx2D] | C22 | | |
| EMC0TxD3[EMC0Tx1D1][EMC0Tx3D] | A23 | | |
| EMC0TxEn[EMC0Tx0En][EMC0Sync] | D21 | Ethernet | 44 |
| EMC0TxErr[EMC0Tx1En] | A22 | Ethernet | 44 |
| [EMC0Tx0En]EMC0TxEn[EMC0Sync] | D21 | Ethernet | 44 |
| [EMC0Tx1En]EMC0TxErr | A22 | | |
| [EMC1TxEn][EMC1Tx2En]GPIO1_12[HDLCMPTxEn6] | B30 | Ethernet | 44 |
| [EMC1TxErr][EMC1Tx3En]GPIO1_11[HDLCMPTxData6] | C29 | | |
| [EMC1Tx2En][EMC1TxEn]GPIO1_12[HDLCMPTxEn6] | B30 | | |
| [EMC1Tx3En][EMC1TxErr]GPIO1_11[HDLCMPTxData6] | C29 | | |
| [EMC1TxD0][EMC1Tx2D0]GPIO1_04[HDLCMPRxData4] | A28 | Ethernet | 44 |
| [EMC1TxD1][EMC1Tx2D1]GPIO1_05[HDLCMPTxClk5] | C27 | | |
| [EMC1TxD2][EMC1Tx3D0]GPIO1_06[HDLCMPTxData5] | B28 | | |
| [EMC1TxD3][EMC1Tx3D1]GPIO1_07[HDLCMPTxEn5] | D27 | | |
| [EOT0/TC0]GPIO0_24 | AF34 | External Slave Peripheral Bus | 47 |
| [EOT1/TC1]GPIO0_25 | AE32 | | |
| [EOT2/TC2]GPIO0_26 | AF33 | | |
| [EOT3/TC3]GPIO0_27[PerCS7] | AE31 | | |
| ExtAck | H02 | External Master Peripheral Bus | 49 |
| ExtReq | J03 | External Master Peripheral Bus | 49 |
| ExtReset | K03 | External Master Peripheral Bus | 49 |

Table 3. Signals Listed Alphabetically (Sheet 3 of 17)

| Signal Name | Ball | Interface Group | Page |
|-------------|---------|--|------|
| GND | A01 | Power Note: Balls N13-N22, P13-P22, R13-R22, T13-T22, U13-U22, V13-V22, W13-W22, Y13-Y22, AA13-AA22, and AB13-AB22 are also thermal balls. | 51 |
| GND | A02 | | |
| GND | A06 | | |
| GND | A10 | | |
| GND | A15 | | |
| GND | A20 | | |
| GND | A25 | | |
| GND | A29 | | |
| GND | A33 | | |
| GND | A34 | | |
| GND | B01 | | |
| GND | B02 | | |
| GND | B33 | | |
| GND | B34 | | |
| GND | C03 | | |
| GND | C32 | | |
| GND | D04 | | |
| GND | D12 | | |
| GND | D17 | | |
| GND | D18 | | |
| GND | D23 | | |
| GND | D31 | | |
| GND | F01 | | |
| GND | F34 | | |
| GND | K01 | | |
| GND | K34 | | |
| GND | M04 | | |
| GND | M31 | | |
| GND | N13–N22 | | |
| GND | P13–P22 | | |
| GND | R01 | | |
| GND | R13–R22 | | |
| GND | R34 | | |
| GND | T13–T22 | | |
| GND | U04 | | |
| GND | U13–U22 | | |
| GND | U31 | | |

Table 3. Signals Listed Alphabetically (Sheet 4 of 17)

| Signal Name | Ball | Interface Group | Page |
|-----------------------|-----------|--|------|
| GND | V04 | Power Note: Balls N13-N22, P13-P22, R13-R22, T13-T22, U13-U22, V13-V22, W13-W22, Y13-Y22, AA13-AA22, and AB13-AB22 are also thermal balls. | 51 |
| GND | V13–V22 | | |
| GND | V31 | | |
| GND | W13–W22 | | |
| GND | Y13–Y22 | | |
| GND | Y01 | | |
| GND | Y34 | | |
| GND | AA13–AA22 | | |
| GND | AB13–AB22 | | |
| GND | AC04 | | |
| GND | AC31 | | |
| GND | AE01 | | |
| GND | AE34 | | |
| GND | AJ01 | | |
| GND | AJ34 | | |
| GND | AL04 | | |
| GND | AL12 | | |
| GND | AL17 | | |
| GND | AL18 | | |
| GND | AL23 | | |
| GND | AL31 | | |
| GND | AM03 | | |
| GND | AM17 | | |
| GND | AM32 | | |
| GND | AN01 | | |
| GND | AN02 | | |
| GND | AN33 | | |
| GND | AN34 | | |
| GND | AP01 | | |
| GND | AP02 | | |
| GND | AP06 | | |
| GND | AP10 | | |
| GND | AP15 | | |
| GND | AP20 | | |
| GND | AP25 | | |
| GND | AP29 | | |
| GND | AP33 | | |
| GND | AP34 | | |
| [Gnt]PCIReq $\bar{0}$ | A19 | PCI | 43 |

Table 3. Signals Listed Alphabetically (Sheet 5 of 17)

| Signal Name | Ball | Interface Group | Page |
|----------------------------|------|-----------------|------|
| GPIO0_00 | U34 | System | 51 |
| GPIO0_01[TS1E] | U33 | | |
| GPIO0_02[TS2E] | V33 | | |
| GPIO0_03[TS1O] | V34 | | |
| GPIO0_04[TS2O] | W34 | | |
| GPIO0_05[TS3] | W33 | | |
| GPIO0_06[TS4] | V32 | | |
| GPIO0_07[TS5] | Y33 | | |
| GPIO0_08[TS6] | Y32 | | |
| GPIO0_09[DMAReq0] | AA34 | | |
| GPIO0_10[DMAReq1] | W32 | | |
| GPIO0_11[DMAReq2] | AA33 | | |
| GPIO0_12[DMAReq3][PerCS4] | AA32 | | |
| GPIO0_13[DMAAck0] | AB34 | | |
| GPIO0_14[DMAAck1] | AB33 | | |
| GPIO0_15[DMAAck2] | AA31 | | |
| GPIO0_16[DMAAck3][PerCS5] | AC34 | | |
| GPIO0_17[IRQ0] | AB32 | | |
| GPIO0_18[IRQ1] | AC33 | | |
| GPIO0_19[IRQ2] | AD34 | | |
| GPIO0_20[IRQ3] | AC32 | | |
| GPIO0_21[IRQ4] | AD33 | | |
| GPIO0_22[IRQ5] | AD32 | | |
| GPIO0_23[IRQ6][PerCS6] | AE33 | | |
| GPIO0_24[EOT0/TC0] | AF34 | | |
| GPIO0_25[EOT1/TC1] | AE32 | | |
| GPIO0_26[EOT2/TC2] | AF33 | | |
| GPIO0_27[EOT3/TC3][PerCS7] | AE31 | | |
| GPIO0_28[PerCS1] | AG34 | | |
| GPIO0_29[PerCS2] | AF32 | | |
| GPIO0_30[PerCS3] | AG33 | | |
| GPIO0_31[TrcClk] | AH34 | | |

Table 3. Signals Listed Alphabetically (Sheet 6 of 17)

| Signal Name | Ball | Interface Group | Page |
|---|------|-----------------|------|
| GPIO1_00[HDLCMPtxCIk4][PHY1Rx2D0][PHY1Rx2D0] | D25 | System | 51 |
| GPIO1_01[HDLCMPtXData4][PHY1Rx2D1][PHY1Rx2D1] | A27 | | |
| GPIO1_02[HDLCMPtXEn4][PHY1Rx2D2][PHY1Rx3D0] | C26 | | |
| GPIO1_03[HDLCMPRxCIk4][PHY1Rx3D3][PHY1Rx3D1] | B27 | | |
| GPIO1_04[HDLCMPRxDData4][EMC1Tx2D0][EMC1Tx2D0] | A28 | | |
| GPIO1_05[HDLCMPtxCIk5][EMC1Tx2D1][EMC1Tx2D1] | C27 | | |
| GPIO1_06[HDLCMPtXData5][EMC1Tx2D2][EMC1Tx3D0] | B28 | | |
| GPIO1_07[HDLCMPtXEn5][EMC1Tx3D3][EMC1Tx3D1] | D27 | | |
| GPIO1_08[HDLCMPRxCIk5][PHY1RxErr][PHY1Rx2Er] | C28 | | |
| GPIO1_09[HDLCMPRxDData5][PHY1Rx2DV][PHY1CrS3DV] | B29 | | |
| GPIO1_10[HDLCMPtxCIk6][PHY1CrS][PHY1CrS2DV] | A30 | | |
| GPIO1_11[HDLCMPtXData6][EMC1TxErr][EMC1Tx3En] | C29 | | |
| GPIO1_12[HDLCMPtXEn6][EMC1TxEn][EMC1Tx2En] | B30 | | |
| GPIO1_13[HDLCMPRxCIk6][PHY1RxClk] | A31 | | |
| GPIO1_14[HDLCMPRxDData6][PHY1Col][PHY1Rx3Er] | B32 | | |
| GPIO1_15[HDLCMPtxCIk7] | D29 | | |
| GPIO1_16[HDLCMPtXData7] | C30 | | |
| GPIO1_17[HDLCMPtXEn7][PHY1TxClk] | A32 | | |
| GPIO1_18[HDLCMPRxCIk7] | B31 | | |
| GPIO1_19[HDLCMPRxDData7] | C31 | | |
| GPIO1_20[HDLCMPtXEn0][UART1_CTS] | D33 | | |
| GPIO1_21[HDLCMPtXEn1][UART1_DSR] | C34 | | |
| GPIO1_22[HDLCMPtXEn2][UART1_DCD] | E32 | | |
| GPIO1_23[HDLCMPtXEn3][UART1_RI] | F31 | | |
| GPIO1_24[HDLCExTxEnA][UART1_RTS] | C33 | | |
| GPIO1_25[HDLCExTxEnB][UART1_DTR] | D34 | | |
| GPIO1_26[UART0_CTS] | E33 | | |
| GPIO1_27[UART0_DSR] | F32 | | |
| GPIO1_28[UART0_DCD] | E34 | | |
| GPIO1_29[UART0_RI]x | F33 | | |
| GPIO1_30[UART0_RTS] | G32 | | |
| GPIO1_31[UART0_DTR] | H31 | | |
| Halt | N33 | System | 51 |
| HDLCExRxClk | AJ31 | HDLC 32-Channel | 44 |
| HDLCExRxDataA | AK33 | HDLC 32-Channel | 44 |
| HDLCExRxDataB | AL34 | | |
| HDLCExRxFS | AM33 | HDLC 32-Channel | 44 |
| HDLCExTxClk | AL32 | HDLC 32-Channel | 44 |
| HDLCExTxDataA | AK32 | HDLC 32-Channel | 44 |
| HDLCExTxDataB | AM34 | | |
| [HDLCExTxEnA]GPIO1_24[UART1_RTS] | C33 | HDLC 32-Channel | 44 |
| [HDLCExTxEnB]GPIO1_25[UART1_DTR] | D34 | | |
| HDLCExTxFS | AL33 | HDLC 32-Channel | 44 |

Table 3. Signals Listed Alphabetically (Sheet 7 of 17)

| Signal Name | Ball | Interface Group | Page |
|---|------|--------------------------------|------|
| HDLCMPRxClk0 | G33 | HDLC 8-Port | 44 |
| HDLCMPRxClk1 | H33 | | |
| HDLCMPRxClk2 | H34 | | |
| HDLCMPRxClk3 | N34 | | |
| [HDLCMPRxClk4]GPIO1_03[PHY1Rx3D3][PHY1Rx3D1] | B27 | HDLC 8-Port | 44 |
| [HDLCMPRxClk5]GPIO1_08[PHY1RxErr][PHY1Rx2Er] | C28 | | |
| [HDLCMPRxClk6]GPIO1_13[PHY1RxClk] | A31 | | |
| [HDLCMPRxClk7]GPIO1_18] | B31 | | |
| HDLCMPRxData0 | G34 | HDLC 8-Port | 44 |
| HDLCMPRxData1 | J32 | | |
| HDLCMPRxData2 | K31 | | |
| HDLCMPRxData3 | P32 | | |
| [HDLCMPRxData4]GPIO1_04[EMC1TxD0][EMC1Tx2D0] | A28 | HDLC 8-Port | 44 |
| [HDLCMPRxData5]GPIO1_09[PHY1RxDV][PHY1CrS3DV] | B29 | | |
| [HDLCMPRxData6]GPIO1_14[PHY1Co][PHY1Rx3Er] | B32 | | |
| [HDLCMPRxData7]GPIO1_19 | C31 | | |
| HDLCMPTxClk0 | P33 | HDLC 8-Port | 44 |
| HDLCMPTxClk1 | P34 | | |
| HDLCMPTxClk2 | R33 | | |
| HDLCMPTxClk3 | T33 | | |
| [HDLCMPTxClk4]GPIO1_00[PHY1Rx3D0][PHY1Rx2D0] | D25 | HDLC 8-Port | 44 |
| [HDLCMPTxClk5]GPIO1_05[EMC1Tx2D1][EMC1Tx3D1] | C27 | | |
| [HDLCMPTxClk6]GPIO1_10[PHY1CrS][PHY1CrS2DV] | A30 | | |
| [HDLCMPTxClk7]GPIO1_15 | D29 | | |
| HDLCMPTxData0 | T32 | HDLC 8-Port | 44 |
| HDLCMPTxData1 | R32 | | |
| HDLCMPTxData2 | U32 | | |
| HDLCMPTxData3 | T34 | | |
| [HDLCMPTxData4]GPIO1_01[PHY1Rx2D1][PHY1Rx3D1] | A27 | HDLC 8-Port | 44 |
| [HDLCMPTxData5]GPIO1_06[EMC1Tx2D2][EMC1Tx3D0] | B28 | | |
| [HDLCMPTxData6]GPIO1_11[EMC1TxErr][EMC1Tx3En] | C29 | | |
| [HDLCMPTxData7]GPIO1_16 | C30 | | |
| [HDLCMPTxEn0]GPIO1_20[UART1_CTS] | D33 | HDLC 8-Port | 44 |
| [HDLCMPTxEn1]GPIO1_21[UART1_DSR] | C34 | | |
| [HDLCMPTxEn2]GPIO1_22[UART1_DCD] | E32 | | |
| [HDLCMPTxEn3]GPIO1_23[UART1_RI] | F31 | | |
| [HDLCMPTxEn4]GPIO1_02[PHYRx3D0] | C26 | | |
| [HDLCMPTxEn5]GPIO1_07[EMC0Tx3D1] | D27 | | |
| [HDLCMPTxEn6]GPIO1_12[EMC0Tx2En] | B30 | | |
| [HDLCMPTxEn7]GPIO1_17[PHY1TxClk] | A32 | | |
| HoldAck | H01 | External Master Peripheral Bus | 49 |
| HoldPri | K04 | | |
| HoldReq | J02 | | |
| IIC_SCL[IIC_SCL] | AK34 | Internal Peripheral Bus | 49 |
| IIC_SDA[IIC_SDA] | AJ32 | | |

Table 3. Signals Listed Alphabetically (Sheet 8 of 17)

| Signal Name | Ball | Interface Group | Page |
|------------------------|------|--|------|
| [IRQ0]GPIO0_17 | AB32 | Interrupts | 50 |
| [IRQ1]GPIO0_18 | AC33 | | |
| [IRQ2]GPIO0_19 | AD34 | | |
| [IRQ3]GPIO0_20 | AC32 | | |
| [IRQ4]GPIO0_21 | AD33 | | |
| [IRQ5]GPIO0_22 | AD32 | | |
| [IRQ6]GPIO0_23[PerCS6] | AE33 | | |
| MemAddr00 | AP27 | SDRAM Note: During a $\overline{\text{CAS}}$ cycle MemAddr00 is the least significant bit (lsb) on this bus. | 46 |
| MemAddr01 | AM26 | | |
| MemAddr02 | AN27 | | |
| MemAddr03 | AN28 | | |
| MemAddr04 | AM28 | | |
| MemAddr05 | AN29 | | |
| MemAddr06 | AP30 | | |
| MemAddr07 | AM29 | | |
| MemAddr08 | AN30 | | |
| MemAddr09 | AP31 | | |
| MemAddr10 | AL29 | | |
| MemAddr11 | AM30 | | |
| MemAddr12 | AP32 | | |
| MemClkOut0 | AM27 | SDRAM | 46 |
| MemClkOut1 | AP28 | | |

Table 3. Signals Listed Alphabetically (Sheet 9 of 17)

| Signal Name | Ball | Interface Group | Page |
|-------------|------|--|------|
| MemData00 | AM18 | SDRAM Notes: 1. MemData00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb) | 46 |
| MemData01 | AN19 | | |
| MemData02 | AP19 | | |
| MemData03 | AP18 | | |
| MemData04 | AN18 | | |
| MemData05 | AN17 | | |
| MemData06 | AP16 | | |
| MemData07 | AN16 | | |
| MemData08 | AM15 | | |
| MemData09 | AP14 | | |
| MemData10 | AM16 | | |
| MemData11 | AN14 | | |
| MemData12 | AM14 | | |
| MemData13 | AP13 | | |
| MemData14 | AN13 | | |
| MemData15 | AL14 | | |
| MemData16 | AM13 | | |
| MemData17 | AN12 | | |
| MemData18 | AP11 | | |
| MemData19 | AM12 | | |
| MemData20 | AN11 | | |
| MemData21 | AN10 | | |
| MemData22 | AP09 | | |
| MemData23 | AM10 | | |
| MemData24 | AL10 | | |
| MemData25 | AP08 | | |
| MemData26 | AM09 | | |
| MemData27 | AN08 | | |
| MemData28 | AP07 | | |
| MemData29 | AM08 | | |
| MemData30 | AN07 | | |
| MemData31 | AL08 | | |

Table 3. Signals Listed Alphabetically (Sheet 10 of 17)

| Signal Name | Ball | Interface Group | Page |
|------------------|------|-----------------|------|
| OV _{DD} | A11 | Power | 51 |
| OV _{DD} | B05 | | |
| OV _{DD} | B22 | | |
| OV _{DD} | C08 | | |
| OV _{DD} | C16 | | |
| OV _{DD} | D05 | | |
| OV _{DD} | D07 | | |
| OV _{DD} | D09 | | |
| OV _{DD} | D11 | | |
| OV _{DD} | D24 | | |
| OV _{DD} | D26 | | |
| OV _{DD} | D28 | | |
| OV _{DD} | D30 | | |
| OV _{DD} | E03 | | |
| OV _{DD} | E04 | | |
| OV _{DD} | E31 | | |
| OV _{DD} | F03 | | |
| OV _{DD} | G04 | | |
| OV _{DD} | G31 | | |
| OV _{DD} | J04 | | |
| OV _{DD} | J31 | | |
| OV _{DD} | L04 | | |
| OV _{DD} | L31 | | |
| OV _{DD} | L32 | | |
| OV _{DD} | M32 | | |
| OV _{DD} | M34 | | |
| OV _{DD} | AD04 | | |
| OV _{DD} | AD31 | | |
| OV _{DD} | AF04 | | |
| OV _{DD} | AF31 | | |
| OV _{DD} | AH04 | | |
| OV _{DD} | AH31 | | |
| OV _{DD} | AK04 | | |
| OV _{DD} | AK31 | | |

Table 3. Signals Listed Alphabetically (Sheet 11 of 17)

| Signal Name | Ball | Interface Group | Page |
|------------------|------|-----------------|------|
| OV _{DD} | AL05 | Power | 51 |
| OV _{DD} | AL07 | | |
| OV _{DD} | AL09 | | |
| OV _{DD} | AL11 | | |
| OV _{DD} | AL24 | | |
| OV _{DD} | AL26 | | |
| OV _{DD} | AL27 | | |
| OV _{DD} | AL28 | | |
| OV _{DD} | AL30 | | |
| OV _{DD} | AM06 | | |
| OV _{DD} | AM11 | | |
| OV _{DD} | AM19 | | |
| OV _{DD} | AM23 | | |
| OV _{DD} | AN32 | | |
| OV _{DD} | AP17 | | |

Table 3. Signals Listed Alphabetically (Sheet 12 of 17)

| Signal Name | Ball | Interface Group | Page |
|--------------|------|--|------|
| PCIAD00 | H04 | PCI Note: PCIAD31 is the most significant bit (msb) on this bus. | 43 |
| PCIAD01 | G01 | | |
| PCIAD02 | G02 | | |
| PCIAD03 | G03 | | |
| PCIAD04 | F02 | | |
| PCIAD05 | F04 | | |
| PCIAD06 | E01 | | |
| PCIAD07 | D03 | | |
| PCIAD08 | C01 | | |
| PCIAD09 | C02 | | |
| PCIAD10 | B03 | | |
| PCIAD11 | A03 | | |
| PCIAD12 | C04 | | |
| PCIAD13 | A04 | | |
| PCIAD14 | A05 | | |
| PCIAD15 | C06 | | |
| PCIAD16 | C11 | | |
| PCIAD17 | C12 | | |
| PCIAD18 | B12 | | |
| PCIAD19 | A12 | | |
| PCIAD20 | A13 | | |
| PCIAD21 | B13 | | |
| PCIAD22 | C14 | | |
| PCIAD23 | B14 | | |
| PCIAD24 | B15 | | |
| PCIAD25 | B16 | | |
| PCIAD26 | A16 | | |
| PCIAD27 | C17 | | |
| PCIAD28 | B17 | | |
| PCIAD29 | C18 | | |
| PCIAD30 | B18 | | |
| PCIAD31 | A18 | | |
| PCIC0[BE0] | D01 | PCI | 43 |
| PCIC1[BE1] | B06 | | |
| PCIC2[BE2] | B10 | | |
| PCIC3[BE3] | C15 | | |
| PCIClk | B11 | PCI | 43 |
| PCIDevSel | A08 | PCI | 43 |
| PCIFrame | C10 | PCI | 43 |
| PCIGnt0[Req] | B19 | PCI | 43 |
| PCIGnt1 | A17 | | |
| PCIGnt2 | D06 | | |
| PCIGnt3 | D10 | | |
| PCIGnt4 | C13 | | |
| PCIGnt5 | D14 | | |
| PCIIDSel | A14 | PCI | 43 |

Table 3. Signals Listed Alphabetically (Sheet 13 of 17)

| Signal Name | Ball | Interface Group | Page |
|---------------|------|---------------------------|------|
| PCIINT[PerWE] | C05 | PCI | 43 |
| PCIIRDY | B09 | PCI | 43 |
| PCIParity | B07 | PCI | 43 |
| PCIPErr | A07 | PCI | 43 |
| PCIReq0[Gnt] | A19 | PCI | 43 |
| PCIReq1 | D02 | | |
| PCIReq2 | E02 | | |
| PCIReq3 | B04 | | |
| PCIReq4 | C07 | | |
| PCIReq5 | A09 | | |
| PCIReset | B20 | PCI | 43 |
| PCISErr | D08 | PCI | 43 |
| PCIStop | B08 | PCI | 43 |
| PCITRDY | C09 | PCI | 43 |
| PerAddr00 | AD02 | External Slave Peripheral | 47 |
| PerAddr01 | AC03 | | |
| PerAddr02 | AD01 | | |
| PerAddr03 | AC02 | | |
| PerAddr04 | AB03 | | |
| PerAddr05 | AC01 | | |
| PerAddr06 | AA04 | | |
| PerAddr07 | AB02 | | |
| PerAddr08 | AB01 | | |
| PerAddr09 | AA03 | | |
| PerAddr10 | AA02 | | |
| PerAddr11 | W03 | | |
| PerAddr12 | AA01 | | |
| PerAddr13 | Y03 | | |
| PerAddr14 | Y02 | | |
| PerAddr15 | V03 | | |
| PerAddr16 | W02 | | |
| PerAddr17 | W01 | | |
| PerAddr18 | V01 | | |
| PerAddr19 | V02 | | |
| PerAddr20 | U02 | | |
| PerAddr21 | U01 | | |
| PerAddr22 | T01 | | |
| PerAddr23 | T02 | | |
| PerAddr24 | U03 | | |
| PerAddr25 | R02 | | |
| PerAddr26 | R03 | | |
| PerAddr27 | P01 | | |
| PerAddr28 | T03 | | |
| PerAddr29 | P02 | | |
| PerAddr30 | P03 | | |
| PerAddr31 | N01 | | |

Table 3. Signals Listed Alphabetically (Sheet 14 of 17)

| Signal Name | Ball | Interface Group | Page |
|----------------------------|------|--|------|
| PerBLast | L03 | External Slave Peripheral Bus | 47 |
| PerClk | K02 | External Slave Peripheral Bus | 47 |
| PerCS0 | M02 | External Slave Peripheral Bus | 47 |
| [PerCS1]GPIO0_28 | AG34 | | |
| [PerCS2]GPIO0_29 | AF32 | | |
| [PerCS3]GPIO0_30 | AG33 | | |
| [PerCS4]GPIO0_12[DMAReq3] | AA32 | | |
| [PerCS5]GPIO0_16[DMAAck3] | AC34 | | |
| [PerCS6]GPIO0_23[IRQ6] | AE33 | | |
| [PerCS7]GPIO0_27[EOT3/TC3] | AE31 | | |
| PerData00 | AM07 | External Slave Peripheral Bus Note: PerData00 is the most significant bit (msb) on this bus. | 47 |
| PerData01 | AN06 | | |
| PerData02 | AP05 | | |
| PerData03 | AN05 | | |
| PerData04 | AP04 | | |
| PerData05 | AN03 | | |
| PerData06 | AL06 | | |
| PerData07 | AM05 | | |
| PerData08 | AN04 | | |
| PerData09 | AM04 | | |
| PerData10 | AL03 | | |
| PerData11 | AL02 | | |
| PerData12 | AM01 | | |
| PerData13 | AK03 | | |
| PerData14 | AJ04 | | |
| PerData15 | AM02 | | |
| PerData16 | AK02 | | |
| PerData17 | AJ03 | | |
| PerData18 | AK01 | | |
| PerData19 | AJ02 | | |
| PerData20 | AH03 | | |
| PerData21 | AG04 | | |
| PerData22 | AH02 | | |
| PerData23 | AG03 | | |
| PerData24 | AG02 | | |
| PerData25 | AF03 | | |
| PerData26 | AG01 | | |
| PerData27 | AE04 | | |
| PerData28 | AF02 | | |
| PerData29 | AE03 | | |
| PerData30 | AF01 | | |
| PerData31 | AE02 | | |
| PerErr | J01 | External Slave Peripheral Bus | 49 |
| PerOE | L01 | External Slave Peripheral Bus | 47 |

Table 3. Signals Listed Alphabetically (Sheet 15 of 17)

| Signal Name | Ball | Interface Group | Page |
|---|------|-------------------------------|------|
| PerPar0 | AP03 | External Slave Peripheral Bus | 47 |
| PerPar1 | AL01 | | |
| PerPar2 | AH01 | | |
| PerPar3 | AD03 | | |
| PerR \overline{W} | M03 | External Slave Peripheral Bus | 47 |
| PerReady | L02 | External Slave Peripheral Bus | 47 |
| $\overline{\text{PerWBE0}}$ | N02 | External Slave Peripheral Bus | 47 |
| $\overline{\text{PerWBE1}}$ | P04 | | |
| $\overline{\text{PerWBE2}}$ | M01 | | |
| $\overline{\text{PerWBE3}}$ | N03 | | |
| $[\overline{\text{PerWE}}]\text{PCIINT}$ | C05 | External Slave Peripheral Bus | 43 |
| PHY0Col[PHY0Rx1Er] | C20 | Ethernet | 44 |
| PHY0CrS[PHY0CrS0DV] | A21 | Ethernet | 44 |
| $[\text{PHY0CrS0DV}]\text{PHY0CrS}$ | A21 | Ethernet | 44 |
| $[\text{PHY0CrS1DV}]\text{PHY0RxDV}$ | C23 | | |
| $[\text{PHY0RefClk}]\text{PHY0TxClk}$ | C19 | Ethernet | 44 |
| PHY0RxClk | B24 | Ethernet | 44 |
| PHY0Rx0D0[PHY0Rx0D0][PHY0Rx0D] | B26 | Ethernet | 44 |
| PHY0Rx0D1[PHY0Rx0D1][PHY0Rx1D] | C25 | | |
| PHY0Rx0D2[PHY0Rx1D0][PHY0Rx2D] | A26 | | |
| PHY0Rx0D3[PHY0Rx1D1][PHY0Rx3D] | B25 | | |
| PHY0Rx0DV[PHY0CrS1DV] | C23 | Ethernet | 44 |
| PHY0RxErr[PHY0Rx0Er] | C24 | Ethernet | 44 |
| $[\text{PHY0Rx0Er}]\text{PHY0RxErr}$ | C24 | Ethernet | 44 |
| $[\text{PHY0Rx1Er}]\text{PHY0Col}$ | C20 | | |
| PHY0TxClk[PHY0RefClk] | C19 | Ethernet | 44 |
| $[\text{PHY1Col}][\text{PHY1Rx3Er}]\text{GPIO1}_14[\text{HDLCMPrxData6}]$ | B32 | Ethernet | 44 |
| $[\text{PHY1CrS}][\text{PHY1CrS2DV}]\text{GPIO1}_10[\text{HDLCMPTxClk6}]$ | A30 | Ethernet | 44 |
| $[\text{PHY1CrS2DV}][\text{PHY1CrS}]\text{GPIO1}_10[\text{HDLCMPTxClk6}]$ | A30 | Ethernet | 44 |
| $[\text{PHY1CrS3DV}][\text{PHY1RxDV}]\text{GPIO1}_09[\text{HDLCMPrxData5}]$ | B29 | Ethernet | 44 |
| $[\text{PHY1RxClk}]\text{GPIO1}_13[\text{HDLCMPrxCIk6}]$ | A31 | Ethernet | 44 |
| $[\text{PHY1RxDV}][\text{PHY1CrS3DV}]\text{GPIO1}_09[\text{HDLCMPrxData5}]$ | B29 | Ethernet | 44 |
| $[\text{PHY1Rx0D0}][\text{PHY1Rx2D0}]\text{GPIO1}_00[\text{HDLCMPTxClk4}]$ | D25 | Ethernet | 44 |
| $[\text{PHY1Rx0D1}][\text{PHY1Rx2D1}]\text{GPIO1}_01[\text{HDLCMPTxData4}]$ | A27 | | |
| $[\text{PHY1Rx0D2}][\text{PHY1Rx3D0}]\text{GPIO1}_02[\text{HDLCMPTxEn4}]$ | C26 | | |
| $[\text{PHY1Rx0D3}][\text{PHY1Rx3D1}]\text{GPIO1}_03[\text{HDLCMPrxCIk4}]$ | B27 | | |
| $[\text{PHY1RxErr}][\text{PHY1Rx2Er}]\text{GPIO1}_08[\text{HDLCMPrxCIk5}]$ | C28 | Ethernet | 44 |
| $[\text{PHY1Rx2Er}][\text{PHY1RxErr}]\text{GPIO1}_08[\text{HDLCMPrxCIk5}]$ | C28 | Ethernet | 44 |
| $[\text{PHY1Rx3Er}][\text{PHY1Col}]\text{GPIO1}_14[\text{HDLCMPrxData6}]$ | B32 | | |
| $[\text{PHY1TxClk}]\text{GPIO1}_17[\text{HDLCMPTxEn7}]$ | A32 | Ethernet | 44 |
| $\overline{\text{RAS}}$ | AP22 | SDRAM | 46 |
| $[\text{Req}]\text{PCI}Gnt0$ | B19 | PCI | 43 |
| Reserved | | Other | 51 |
| SysClk | L33 | System | 51 |
| SysErr | K32 | System | 51 |
| $\overline{\text{SysReset}}$ | J33 | System | 51 |

Table 3. Signals Listed Alphabetically (Sheet 16 of 17)

| Signal Name | Ball | Interface Group | Page |
|----------------------------------|------|-------------------------------|------|
| TCK | K33 | JTAG | 50 |
| [TC0/EOT0]GPIO0_24 | AF34 | External Slave Peripheral Bus | 47 |
| [TC1/EOT1]GPIO0_25 | AE32 | | |
| [TC2/EOT2]GPIO0_26 | AF33 | | |
| [TC3/EOT3]GPIO0_27 | AE31 | | |
| TDI | N32 | JTAG | 50 |
| TDO | J34 | JTAG | 50 |
| TestEn | M33 | System | 51 |
| TmrClk | D32 | System | 51 |
| TMS | H32 | JTAG | 50 |
| [TrcClk]GPIO0_31 | AH34 | Trace | 51 |
| TRST | L34 | JTAG | 50 |
| [TS1E]GPIO0_01 | U33 | Trace | 51 |
| [TS2E]GPIO0_02 | V33 | | |
| [TS1O]GPIO0_03 | V34 | Trace | 51 |
| [TS2O]GPIO0_04 | W34 | | |
| [TS3]GPIO0_05 | W33 | Trace | 51 |
| [TS4]GPIO0_06 | V32 | | |
| [TS5]GPIO0_07 | Y33 | | |
| [TS6]GPIO0_08 | Y32 | | |
| [UART0_CTS]GPIO1_26 | E33 | Internal Peripheral | 49 |
| [UART0_DCD]GPIO1_28 | E34 | Internal Peripheral | 49 |
| [UART0_DSR]GPIO1_27 | F32 | Internal Peripheral | 49 |
| [UART0_DTR]GPIO1_31 | H31 | Internal Peripheral | 49 |
| [UART0_RI]GPIO1_29 | F33 | Internal Peripheral | 49 |
| [UART0_RTS]GPIO1_30 | G32 | Internal Peripheral | 49 |
| UART0_Rx | AG32 | Internal Peripheral | 49 |
| UART0_Tx | AH33 | Internal Peripheral | 49 |
| [UART1_CTS]GPIO1_20[HDLCMPTxEn0] | D33 | Internal Peripheral | 49 |
| [UART1_DCD]GPIO1_22[HDLCMPTxEn2] | E32 | Internal Peripheral | 49 |
| [UART1_DSR]GPIO1_21[HDLCMPTxEn1] | C34 | Internal Peripheral | 49 |
| [UART1_DTR]GPIO1_25[HDLCMPTxEnB] | D34 | Internal Peripheral | 49 |
| [UART1_RI]GPIO1_23[HDLCMPTxEn3] | F31 | Internal Peripheral | 49 |
| [UART1_RTS]GPIO1_24[HDLCMPTxEnA] | C33 | Internal Peripheral | 49 |
| UART1_Rx | AH32 | Internal Peripheral | 49 |
| UART1_Tx | AJ33 | Internal Peripheral | 49 |
| UARTSerClk | AG31 | Internal Peripheral | 49 |

Table 3. Signals Listed Alphabetically (Sheet 17 of 17)

| Signal Name | Ball | Interface Group | Page |
|-----------------|------|-----------------|------|
| V _{DD} | D13 | Power | 51 |
| V _{DD} | D15 | | |
| V _{DD} | D16 | | |
| V _{DD} | D19 | | |
| V _{DD} | D20 | | |
| V _{DD} | D22 | | |
| V _{DD} | N04 | | |
| V _{DD} | N31 | | |
| V _{DD} | R04 | | |
| V _{DD} | R31 | | |
| V _{DD} | T04 | | |
| V _{DD} | T31 | | |
| V _{DD} | W04 | | |
| V _{DD} | W31 | | |
| V _{DD} | Y04 | | |
| V _{DD} | Y31 | | |
| V _{DD} | AB04 | | |
| V _{DD} | AB31 | | |
| V _{DD} | AL13 | | |
| V _{DD} | AL15 | | |
| V _{DD} | AL16 | | |
| V _{DD} | AL19 | | |
| V _{DD} | AL20 | | |
| V _{DD} | AL22 | | |
| \overline{WE} | AM21 | SDRAM | 46 |

SIGNALS LISTED BY BALL ASSIGNMENT

Table 4. Signals Listed by Ball Assignment (Sheet 1 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|------------------|------|------------------|------|------------------|------|------------------|
| A01 | GND | B01 | GND | C01 | PCIAD08 | D01 | PCIC0[BE0] |
| A02 | GND | B02 | GND | C02 | PCIAD09 | D02 | PCIReq1 |
| A03 | PCIAD11 | B03 | PCIAD10 | C03 | GND | D03 | PCIAD07 |
| A04 | PCIAD13 | B04 | PCIReq3 | C04 | PCIAD12 | D04 | GND |
| A05 | PCIAD14 | B05 | OV _{DD} | C05 | PCIINT[PerWE] | D05 | OV _{DD} |
| A06 | GND | B06 | PCIC1[BE1] | C06 | PCIAD15 | D06 | PCIInt2 |
| A07 | PCIPErr | B07 | PCIParity | C07 | PCIReq4 | D07 | OV _{DD} |
| A08 | PCIDevSel | B08 | PCIStop | C08 | OV _{DD} | D08 | PCISErr |
| A09 | PCIReq5 | B09 | PCIIRDY | C09 | PCITRDY | D09 | OV _{DD} |
| A10 | GND | B10 | PCIC2[BE2] | C10 | PCIFrame | D10 | PCIInt3 |
| A11 | OV _{DD} | B11 | PCIClk | C11 | PCIAD16 | D11 | OV _{DD} |
| A12 | PCIAD19 | B12 | PCIAD18 | C12 | PCIAD17 | D12 | GND |
| A13 | PCIAD20 | B13 | PCIAD21 | C13 | PCIInt4 | D13 | V _{DD} |
| A14 | PCIIDSel | B14 | PCIAD23 | C14 | PCIAD22 | D14 | PCIInt5 |
| A15 | GND | B15 | PCIAD24 | C15 | PCIC3[BE3] | D15 | V _{DD} |
| A16 | PCIAD26 | B16 | PCIAD25 | C16 | OV _{DD} | D16 | V _{DD} |
| A17 | PCIInt1 | B17 | PCIAD28 | C17 | PCIAD27 | D17 | GND |
| A18 | PCIAD31 | B18 | PCIAD30 | C18 | PCIAD29 | D18 | GND |
| A19 | PCIReq0 * | B19 | PCIInt0[Req] | C19 | PHY0TxClk * | D19 | V _{DD} |
| A20 | GND | B20 | PCIReset | C20 | PHY0Col * | D20 | V _{DD} |
| A21 | PHY0CrS * | B21 | EMC0MDIO | C21 | EMC0MDClk | D21 | EMC0TxEn * |
| A22 | EMC0TxErr * | B22 | OV _{DD} | C22 | EMC0TxD2 * | D22 | V _{DD} |
| A23 | EMC0TxD3 * | B23 | EMC0TxD1 * | C23 | PHY0RxDV * | D23 | GND |
| A24 | EMC0TxD0 * | B24 | PHY0RxClk | C24 | PHY0RxErr * | D24 | OV _{DD} |
| A25 | GND | B25 | PHY0RxD3 * | C25 | PHY0RxD1 * | D25 | GPIO1_00 * |
| A26 | PHY0RxD2 * | B26 | PHY0RxD0 * | C26 | GPIO1_02 * | D26 | OV _{DD} |
| A27 | GPIO1_01 * | B27 | GPIO1_03 * | C27 | GPIO1_05 * | D27 | GPIO1_07 * |
| A28 | GPIO1_04 * | B28 | GPIO1_06 * | C28 | GPIO1_08 * | D28 | OV _{DD} |
| A29 | GND | B29 | GPIO1_09 * | C29 | GPIO1_11 * | D29 | GPIO1_15 * |
| A30 | GPIO1_10 * | B30 | GPIO1_12 * | C30 | GPIO1_16 * | D30 | OV _{DD} |
| A31 | GPIO1_13 * | B31 | GPIO1_18 * | C31 | GPIO1_19 * | D31 | GND |
| A32 | GPIO1_17 * | B32 | GPIO1_14 *] | C32 | GND | D32 | TmrClk |
| A33 | GND | B33 | GND | C33 | GPIO1_24 * | D33 | GPIO1_20 * |
| A34 | GND | B34 | GND | C34 | GPIO1_21 * | D34 | GPIO1_25 * |

Table 4. Signals Listed by Ball Assignment (Sheet 2 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|-------------|------|-------------|------|---------------|------|--------------|
| E01 | PCIAD06 | F01 | GND | G01 | PCIAD01 | H01 | HoldAck |
| E02 | PCIReq2 | F02 | PCIAD04 | G02 | PCIAD02 | H02 | ExtAck |
| E03 | OVDD | F03 | OVDD | G03 | PCIAD03 | H03 | BusReq |
| E04 | OVDD | F04 | PCIAD05 | G04 | OVDD | H04 | PCIAD00 |
| E05 | No ball | F05 | No ball | G05 | No ball | H05 | No ball |
| E06 | No ball | F06 | No ball | G06 | No ball | H06 | No ball |
| E07 | No ball | F07 | No ball | G07 | No ball | H07 | No ball |
| E08 | No ball | F08 | No ball | G08 | No ball | H08 | No ball |
| E09 | No ball | F09 | No ball | G09 | No ball | H09 | No ball |
| E10 | No ball | F10 | No ball | G10 | No ball | H10 | No ball |
| E11 | No ball | A11 | No ball | G11 | No ball | H11 | No ball |
| E12 | No ball | F12 | No ball | G12 | No ball | H12 | No ball |
| E13 | No ball | F13 | No ball | G13 | No ball | H13 | No ball |
| E14 | No ball | F14 | No ball | G14 | No ball | H14 | No ball |
| E15 | No ball | F15 | No ball | G15 | No ball | H15 | No ball |
| E16 | No ball | F16 | No ball | G16 | No ball | H16 | No ball |
| E17 | No ball | F17 | No ball | G17 | No ball | H17 | No ball |
| E18 | No ball | F18 | No ball | G18 | No ball | H18 | No ball |
| E19 | No ball | F19 | No ball | G19 | No ball | H19 | No ball |
| E20 | No ball | F20 | No ball | G20 | No ball | H20 | No ball |
| E21 | No ball | F21 | No ball | G21 | No ball | H21 | No ball |
| E22 | No ball | F22 | No ball | G22 | No ball | H22 | No ball |
| E23 | No ball | F23 | No ball | G23 | No ball | H23 | No ball |
| E24 | No ball | F24 | No ball | G24 | No ball | H24 | No ball |
| E25 | No ball | F25 | No ball | G25 | No ball | H25 | No ball |
| E26 | No ball | F26 | No ball | G26 | No ball | H26 | No ball |
| E27 | No ball | F27 | No ball | G27 | No ball | H27 | No ball |
| E28 | No ball | F28 | No ball | G28 | No ball | H28 | No ball |
| E29 | No ball | F29 | No ball | G29 | No ball | H29 | No ball |
| E30 | No ball | F30 | No ball | G30 | No ball | H30 | No ball |
| E31 | OVDD | F31 | GPIO1_23 * | G31 | OVDD | H31 | GPIO1_31 * |
| E32 | GPIO1_22 * | F32 | GPIO1_27 * | G32 | GPIO1_30 * | H32 | TMS |
| E33 | GPIO1_26 * | F33 | GPIO1_29 * | G33 | HDLCMPRxClk0 | H33 | HDLCMPRxClk1 |
| E34 | GPIO1_28 *] | F34 | GND | G34 | HDLCMPRxData0 | H34 | HDLCMPRxClk2 |

Table 4. Signals Listed by Ball Assignment (Sheet 3 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|------------------|------|---------------|------|------------------|------|------------------|
| J01 | PerErr | K01 | GND | L01 | PerOE | M01 | PerWBE2 |
| J02 | HoldReq | K02 | PerClk | L02 | PerReady | M02 | PerCS0 |
| J03 | ExtReq | K03 | ExtReset | L03 | PerBLast | M03 | PerR \bar{W} |
| J04 | OV _{DD} | K04 | HoldPri | L04 | OV _{DD} | M04 | GND |
| J05 | No ball | K05 | No ball | L05 | No ball | M05 | No ball |
| J06 | No ball | K06 | No ball | L06 | No ball | M06 | No ball |
| J07 | No ball | K07 | No ball | L07 | No ball | M07 | No ball |
| J08 | No ball | K08 | No ball | L08 | No ball | M08 | No ball |
| J09 | No ball | K09 | No ball | L09 | No ball | M09 | No ball |
| J10 | No ball | K10 | No ball | L10 | No ball | M10 | No ball |
| J11 | No ball | K11 | No ball | L11 | No ball | M11 | No ball |
| J12 | No ball | K12 | No ball | L12 | No ball | M12 | No ball |
| J13 | No ball | K13 | No ball | L13 | No ball | M13 | No ball |
| J14 | No ball | K14 | No ball | L14 | No ball | M14 | No ball |
| J15 | No ball | K15 | No ball | L15 | No ball | M15 | No ball |
| J16 | No ball | K16 | No ball | L16 | No ball | M16 | No ball |
| J17 | No ball | K17 | No ball | L17 | No ball | M17 | No ball |
| J18 | No ball | K18 | No ball | L18 | No ball | M18 | No ball |
| J19 | No ball | K19 | No ball | L19 | No ball | M19 | No ball |
| J20 | No ball | K20 | No ball | L20 | No ball | M20 | No ball |
| J21 | No ball | K21 | No ball | L21 | No ball | M21 | No ball |
| J22 | No ball | K22 | No ball | L22 | No ball | M22 | No ball |
| J23 | No ball | K23 | No ball | L23 | No ball | M23 | No ball |
| J24 | No ball | K24 | No ball | L24 | No ball | M24 | No ball |
| J25 | No ball | K25 | No ball | L25 | No ball | M25 | No ball |
| J26 | No ball | K26 | No ball | L26 | No ball | M26 | No ball |
| J27 | No ball | K27 | No ball | L27 | No ball | M27 | No ball |
| J28 | No ball | K28 | No ball | L28 | No ball | M28 | No ball |
| J29 | No ball | K29 | No ball | L29 | No ball | M29 | No ball |
| J30 | No ball | K30 | No ball | L30 | No ball | M30 | No ball |
| J31 | OV _{DD} | K31 | HDLCMPRxData2 | L31 | OV _{DD} | M31 | GND |
| J32 | HDLCMPRxData1 | K32 | SysErr | L32 | OV _{DD} | M32 | OV _{DD} |
| J33 | SysReset | K33 | TCK | L33 | SysClk | M33 | TestEn |
| J34 | TDO | K34 | GND | L34 | TRST | M34 | OV _{DD} |

Table 4. Signals Listed by Ball Assignment (Sheet 4 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|-----------------------------|------|-----------------------------|------|-----------------|------|-----------------|
| N01 | PerAddr31 | P01 | PerAddr27 | R01 | GND | T01 | PerAddr22 |
| N02 | $\overline{\text{PerWBE0}}$ | P02 | PerAddr29 | R02 | PerAddr25 | T02 | PerAddr23 |
| N03 | $\overline{\text{PerWBE3}}$ | P03 | PerAddr30 | R03 | PerAddr26 | T03 | PerAddr28 |
| N04 | V _{DD} | P04 | $\overline{\text{PerWBE1}}$ | R04 | V _{DD} | T04 | V _{DD} |
| N05 | No ball | P05 | No ball | R05 | No ball | T05 | No ball |
| N06 | No ball | P06 | No ball | R06 | No ball | T06 | No ball |
| N07 | No ball | P07 | No ball | R07 | No ball | T07 | No ball |
| N08 | No ball | P08 | No ball | R08 | No ball | T08 | No ball |
| N09 | No ball | P09 | No ball | R09 | No ball | T09 | No ball |
| N10 | No ball | P10 | No ball | R10 | No ball | T10 | No ball |
| N11 | No ball | P11 | No ball | R11 | No ball | T11 | No ball |
| N12 | No ball | P12 | No ball | R12 | No ball | T12 | No ball |
| N13 | GND | P13 | GND | R13 | GND | T13 | GND |
| N14 | GND | P14 | GND | R14 | GND | T14 | GND |
| N15 | GND | P15 | GND | R15 | GND | T15 | GND |
| N16 | GND | P16 | GND | R16 | GND | T16 | GND |
| N17 | GND | P17 | GND | R17 | GND | T17 | GND |
| N18 | GND | P18 | GND | R18 | GND | T18 | GND |
| N19 | GND | P19 | GND | R19 | GND | T19 | GND |
| N20 | GND | P20 | GND | R20 | GND | T20 | GND |
| N21 | GND | P21 | GND | R21 | GND | T21 | GND |
| N22 | GND | P22 | GND | R22 | GND | T22 | GND |
| N23 | No ball | P23 | No ball | R23 | No ball | T23 | No ball |
| N24 | No ball | P24 | No ball | R24 | No ball | T24 | No ball |
| N25 | No ball | P25 | No ball | R25 | No ball | T25 | No ball |
| N26 | No ball | P26 | No ball | R26 | No ball | T26 | No ball |
| N27 | No ball | P27 | No ball | R27 | No ball | T27 | No ball |
| N28 | No ball | P28 | No ball | R28 | No ball | T28 | No ball |
| N29 | No ball | P29 | No ball | R29 | No ball | T29 | No ball |
| N30 | No ball | P30 | No ball | R30 | No ball | T30 | No ball |
| N31 | V _{DD} | P31 | AV _{DD} | R31 | V _{DD} | T31 | V _{DD} |
| N32 | TDI | P32 | HDLCMPRxData3 | R32 | HDLCMPTxData1 | T32 | HDLCMPTxData0 |
| N33 | $\overline{\text{Halt}}$ | P33 | HDLCMPTxCIk0 | R33 | HDLCMPTxCIk2 | T33 | HDLCMPTxCIk3 |
| N34 | HDLCMPRxCIk3 | P34 | HDLCMPTxCIk1 | R34 | GND | T34 | HDLCMPTxData3 |

Table 4. Signals Listed by Ball Assignment (Sheet 5 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|---------------|------|-------------|------|-----------------|------|-----------------|
| U01 | PerAddr21 | V01 | PerAddr18 | W01 | PerAddr17 | Y01 | GND |
| U02 | PerAddr20 | V02 | PerAddr19 | W02 | PerAddr16 | Y02 | PerAddr14 |
| U03 | PerAddr24 | V03 | PerAddr15 | W03 | PerAddr11 | Y03 | PerAddr13 |
| U04 | GND | V04 | GND | W04 | V _{DD} | Y04 | V _{DD} |
| U05 | No ball | V05 | No ball | W05 | No ball | Y05 | No ball |
| U06 | No ball | V06 | No ball | W06 | No ball | Y06 | No ball |
| U07 | No ball | V07 | No ball | W07 | No ball | Y07 | No ball |
| U08 | No ball | V08 | No ball | W08 | No ball | Y08 | No ball |
| U09 | No ball | V09 | No ball | W09 | No ball | Y09 | No ball |
| U10 | No ball | V10 | No ball | W10 | No ball | Y10 | No ball |
| U11 | No ball | V11 | No ball | W11 | No ball | Y11 | No ball |
| U12 | No ball | V12 | No ball | W12 | No ball | Y12 | No ball |
| U13 | GND | V13 | GND | W13 | GND | Y13 | GND |
| U14 | GND | V14 | GND | W14 | GND | Y14 | GND |
| U15 | GND | V15 | GND | W15 | GND | Y15 | GND |
| U16 | GND | V16 | GND | W16 | GND | Y16 | GND |
| U17 | GND | V17 | GND | W17 | GND | Y17 | GND |
| U18 | GND | V18 | GND | W18 | GND | Y18 | GND |
| U19 | GND | V19 | GND | W19 | GND | Y19 | GND |
| U20 | GND | V20 | GND | W20 | GND | Y20 | GND |
| U21 | GND | V21 | GND | W21 | GND | Y21 | GND |
| U22 | GND | V22 | GND | W22 | GND | Y22 | GND |
| U23 | No ball | V23 | No ball | W23 | No ball | Y23 | No ball |
| U24 | No ball | V24 | No ball | W24 | No ball | Y24 | No ball |
| U25 | No ball | V25 | No ball | W25 | No ball | Y25 | No ball |
| U26 | No ball | V26 | No ball | W26 | No ball | Y26 | No ball |
| U27 | No ball | V27 | No ball | W27 | No ball | Y27 | No ball |
| U28 | No ball | V28 | No ball | W28 | No ball | Y28 | No ball |
| U29 | No ball | V29 | No ball | W29 | No ball | Y29 | No ball |
| U30 | No ball | V30 | No ball | W30 | No ball | Y30 | No ball |
| U31 | GND | V31 | GND | W31 | V _{DD} | Y31 | V _{DD} |
| U32 | HDLCMPTxData2 | V32 | GPIO0_06 * | W32 | GPIO0_10 * | Y32 | GPIO0_08 * |
| U33 | GPIO0_01 * | V33 | GPIO0_02 * | W33 | GPIO0_05 * | Y33 | GPIO0_07 * |
| U34 | GPIO0_00 | V34 | GPIO0_03 * | W34 | GPIO0_04 * | Y34 | GND |

Table 4. Signals Listed by Ball Assignment (Sheet 6 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|-------------|------|-----------------|------|-------------|------|------------------|
| AA01 | PerAddr12 | AB01 | PerAddr08 | AC01 | PerAddr05 | AD01 | PerAddr02 |
| AA02 | PerAddr10 | AB02 | PerAddr07 | AC02 | PerAddr03 | AD02 | PerAddr00 |
| AA03 | PerAddr09 | AB03 | PerAddr04 | AC03 | PerAddr01 | AD03 | PerPar3 |
| AA04 | PerAddr06 | AB04 | V _{DD} | AC04 | GND | AD04 | OV _{DD} |
| AA05 | No ball | AB05 | No ball | AC05 | No ball | AD05 | No ball |
| AA06 | No ball | AB06 | No ball | AC06 | No ball | AD06 | No ball |
| AA07 | No ball | AB07 | No ball | AC07 | No ball | AD07 | No ball |
| AA08 | No ball | AB08 | No ball | AC08 | No ball | AD08 | No ball |
| AA09 | No ball | AB09 | No ball | AC09 | No ball | AD09 | No ball |
| AA10 | No ball | AB10 | No ball | AC10 | No ball | AD10 | No ball |
| AA11 | No ball | AB11 | No ball | AC11 | No ball | AD11 | No ball |
| AA12 | No ball | AB12 | No ball | AC12 | No ball | AD12 | No ball |
| AA13 | GND | AB13 | GND | AC13 | No ball | AD13 | No ball |
| AA14 | GND | AB14 | GND | AC14 | No ball | AD14 | No ball |
| AA15 | GND | AB15 | GND | AC15 | No ball | AD15 | No ball |
| AA16 | GND | AB16 | GND | AC16 | No ball | AD16 | No ball |
| AA17 | GND | AB17 | GND | AC17 | No ball | AD17 | No ball |
| AA18 | GND | AB18 | GND | AC18 | No ball | AD18 | No ball |
| AA19 | GND | AB19 | GND | AC19 | No ball | AD19 | No ball |
| AA20 | GND | AB20 | GND | AC20 | No ball | AD20 | No ball |
| AA21 | GND | AB21 | GND | AC21 | No ball | AD21 | No ball |
| AA22 | GND | AB22 | GND | AC22 | No ball | AD22 | No ball |
| AA23 | No ball | AB23 | No ball | AC23 | No ball | AD23 | No ball |
| AA24 | No ball | AB24 | No ball | AC24 | No ball | AD24 | No ball |
| AA25 | No ball | AB25 | No ball | AC25 | No ball | AD25 | No ball |
| AA26 | No ball | AB26 | No ball | AC26 | No ball | AD26 | No ball |
| AA27 | No ball | AB27 | No ball | AC27 | No ball | AD27 | No ball |
| AA28 | No ball | AB28 | No ball | AC28 | No ball | AD28 | No ball |
| AA29 | No ball | AB29 | No ball | AC29 | No ball | AD29 | No ball |
| AA30 | No ball | AB30 | No ball | AC30 | No ball | AD30 | No ball |
| AA31 | GPIO0_15 * | AB31 | V _{DD} | AC31 | GND | AD31 | OV _{DD} |
| AA32 | GPIO0_12 * | AB32 | GPIO0_17 * | AC32 | GPIO0_20 * | AD32 | GPIO0_22 * |
| AA33 | GPIO0_11 * | AB33 | GPIO0_14 * | AC33 | GPIO0_18 * | AD33 | GPIO0_21 * |
| AA34 | GPIO0_09 * | AB34 | GPIO0_13 * | AC34 | GPIO0_16 * | AD34 | GPIO0_19 * |

Table 4. Signals Listed by Ball Assignment (Sheet 7 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|-------------|------|------------------|------|-------------|------|------------------|
| AE01 | GND | AF01 | PerData30 | AG01 | PerData26 | AH01 | PerPar2 |
| AE02 | PerData31 | AF02 | PerData28 | AG02 | PerData24 | AH02 | PerData22 |
| AE03 | PerData29 | AF03 | PerData25 | AG03 | PerData23 | AH03 | PerData20 |
| AE04 | PerData27 | AF04 | OV _{DD} | AG04 | PerData21 | AH04 | OV _{DD} |
| AE05 | No ball | AF05 | No ball | AG05 | No ball | AH05 | No ball |
| AE06 | No ball | AF06 | No ball | AG06 | No ball | AH06 | No ball |
| AE07 | No ball | AF07 | No ball | AG07 | No ball | AH07 | No ball |
| AE08 | No ball | AF08 | No ball | AG08 | No ball | AH08 | No ball |
| AE09 | No ball | AF09 | No ball | AG09 | No ball | AH09 | No ball |
| AE10 | No ball | AF10 | No ball | AG10 | No ball | AH10 | No ball |
| AE11 | No ball | AF11 | No ball | AG11 | No ball | AH11 | No ball |
| AE12 | No ball | AF12 | No ball | AG12 | No ball | AH12 | No ball |
| AE13 | No ball | AF13 | No ball | AG13 | No ball | AH13 | No ball |
| AE14 | No ball | AF14 | No ball | AG14 | No ball | AH14 | No ball |
| AE15 | No ball | AF15 | No ball | AG15 | No ball | AH15 | No ball |
| AE16 | No ball | AF16 | No ball | AG16 | No ball | AH16 | No ball |
| AE17 | No ball | AF17 | No ball | AG17 | No ball | AH17 | No ball |
| AE18 | No ball | AF18 | No ball | AG18 | No ball | AH18 | No ball |
| AE19 | No ball | AF19 | No ball | AG19 | No ball | AH19 | No ball |
| AE20 | No ball | AF20 | No ball | AG20 | No ball | AH20 | No ball |
| AE21 | No ball | AF21 | No ball | AG21 | No ball | AH21 | No ball |
| AE22 | No ball | AF22 | No ball | AG22 | No ball | AH22 | No ball |
| AE23 | No ball | AF23 | No ball | AG23 | No ball | AH23 | No ball |
| AE24 | No ball | AF24 | No ball | AG24 | No ball | AH24 | No ball |
| AE25 | No ball | AF25 | No ball | AG25 | No ball | AH25 | No ball |
| AE26 | No ball | AF26 | No ball | AG26 | No ball | AH26 | No ball |
| AE27 | No ball | AF27 | No ball | AG27 | No ball | AH27 | No ball |
| AE28 | No ball | AF28 | No ball | AG28 | No ball | AH28 | No ball |
| AE29 | No ball | AF29 | No ball | AG29 | No ball | AH29 | No ball |
| AE30 | No ball | AF30 | No ball | AG30 | No ball | AH30 | No ball |
| AE31 | GPIO0_27 * | AF31 | OV _{DD} | AG31 | UARTSerClk | AH31 | OV _{DD} |
| AE32 | GPIO0_25 * | AF32 | GPIO0_29 * | AG32 | UART0_Rx | AH32 | UART1_Rx |
| AE33 | GPIO0_23 * | AF33 | GPIO0_26 * | AG33 | GPIO0_30 * | AH33 | UART0_Tx |
| AE34 | GND | AF34 | GPIO0_24 * | AG34 | GPIO0_28 * | AH34 | GPIO0_31 * |

Table 4. Signals Listed by Ball Assignment (Sheet 8 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|----------------|------|------------------|------|------------------|------|------------------|
| AJ01 | GND | AK01 | PerData18 | AL01 | PerPar1 | AM01 | PerData12 |
| AJ02 | PerData19 | AK02 | PerData16 | AL02 | PerData11 | AM02 | PerData15 |
| AJ03 | PerData17 | AK03 | PerData13 | AL03 | PerData10 | AM03 | GND |
| AJ04 | PerData14 | AK04 | OV _{DD} | AL04 | GND | AM04 | PerData09 |
| AJ05 | No ball | AK05 | No ball | AL05 | OV _{DD} | AM05 | PerData07 |
| AJ06 | No ball | AK06 | No ball | AL06 | PerData06 | AM06 | OV _{DD} |
| AJ07 | No ball | AK07 | No ball | AL07 | OV _{DD} | AM07 | PerData00 |
| AJ08 | No ball | AK08 | No ball | AL08 | MemData31 | AM08 | MemData29 |
| AJ09 | No ball | AK09 | No ball | AL09 | OV _{DD} | AM09 | MemData26 |
| AJ10 | No ball | AK10 | No ball | AL10 | MemData24 | AM10 | MemData23 |
| AJ11 | No ball | AK11 | No ball | AL11 | OV _{DD} | AM11 | OV _{DD} |
| AJ12 | No ball | AK12 | No ball | AL12 | GND | AM12 | MemData19 |
| AJ13 | No ball | AK13 | No ball | AL13 | V _{DD} | AM13 | MemData16 |
| AJ14 | No ball | AK14 | No ball | AL14 | MemData15 | AM14 | MemData12 |
| AJ15 | No ball | AK15 | No ball | AL15 | V _{DD} | AM15 | MemData08 |
| AJ16 | No ball | AK16 | No ball | AL16 | V _{DD} | AM16 | MemData10 |
| AJ17 | No ball | AK17 | No ball | AL17 | GND | AM17 | GND |
| AJ18 | No ball | AK18 | No ball | AL18 | GND | AM18 | MemData00 |
| AJ19 | No ball | AK19 | No ball | AL19 | V _{DD} | AM19 | OV _{DD} |
| AJ20 | No ball | AK20 | No ball | AL20 | V _{DD} | AM20 | DQMCB |
| AJ21 | No ball | AK21 | No ball | AL21 | BankSel0 | AM21 | WE |
| AJ22 | No ball | AK22 | No ball | AL22 | V _{DD} | AM22 | BankSel2 |
| AJ23 | No ball | AK23 | No ball | AL23 | GND | AM23 | OV _{DD} |
| AJ24 | No ball | AK24 | No ball | AL24 | OV _{DD} | AM24 | ECC2 |
| AJ25 | No ball | AK25 | No ball | AL25 | ECC7 | AM25 | ECC5 |
| AJ26 | No ball | AK26 | No ball | AL26 | OV _{DD} | AM26 | MemAddr01 |
| AJ27 | No ball | AK27 | No ball | AL27 | OV _{DD} | AM27 | MemClkOut0 |
| AJ28 | No ball | AK28 | No ball | AL28 | OV _{DD} | AM28 | MemAddr04 |
| AJ29 | No ball | AK29 | No ball | AL29 | MemAddr10 | AM29 | MemAddr07 |
| AJ30 | No ball | AK30 | No ball | AL30 | OV _{DD} | AM30 | MemAddr11 |
| AJ31 | HDLCEXRxCik | AK31 | OV _{DD} | AL31 | GND | AM31 | BA1 |
| AJ32 | IICSDA[IICSDA] | AK32 | HDLCEXTxDataA | AL32 | HDLCEXTxCik | AM32 | GND |
| AJ33 | UART1_Tx | AK33 | HDLCEXRxDatA | AL33 | HDLCEXTxFS | AM33 | HDLCEXRxFs |
| AJ34 | GND | AK34 | IICscl[IICscl] | AL34 | HDLCEXRxDatB | AM34 | HDLCEXTxDatB |

Table 4. Signals Listed by Ball Assignment (Sheet 9 of 9)

Signal names followed by an asterisk (*) are multiplexed. Look up the name shown in “Signals Listed Alphabetically” on page 15 for an indication of all signals on the pin.

| Ball | Signal Name | Ball | Signal Name | Ball | Signal Name | Ball | Signal Name |
|------|------------------|------|------------------|------|-------------|------|-------------|
| AN01 | GND | AP01 | GND | | | | |
| AN02 | GND | AP02 | GND | | | | |
| AN03 | PerData05 | AP03 | PerPar0 | | | | |
| AN04 | PerData08 | AP04 | PerData04 | | | | |
| AN05 | PerData03 | AP05 | PerData02 | | | | |
| AN06 | PerData01 | AP06 | GND | | | | |
| AN07 | MemData30 | AP07 | MemData28 | | | | |
| AN08 | MemData27 | AP08 | MemData25 | | | | |
| AN09 | DQM3 | AP09 | MemData22 | | | | |
| AN10 | MemData21 | AP10 | GND | | | | |
| AN11 | MemData20 | AP11 | MemData18 | | | | |
| AN12 | MemData17 | AP12 | DQM2 | | | | |
| AN13 | MemData14 | AP13 | MemData13 | | | | |
| AN14 | MemData11 | AP14 | MemData09 | | | | |
| AN15 | DQM1 | AP15 | GND | | | | |
| AN16 | MemData07 | AP16 | MemData06 | | | | |
| AN17 | MemData05 | AP17 | OV _{DD} | | | | |
| AN18 | MemData04 | AP18 | MemData03 | | | | |
| AN19 | MemData01 | AP19 | MemData02 | | | | |
| AN20 | DQM0 | AP20 | GND | | | | |
| AN21 | ClkEn1 | AP21 | ClkEn0 | | | | |
| AN22 | CAS | AP22 | RAS | | | | |
| AN23 | BankSel3 | AP23 | BankSel1 | | | | |
| AN24 | ECC1 | AP24 | ECC0 | | | | |
| AN25 | ECC3 | AP25 | GND | | | | |
| AN26 | ECC6 | AP26 | ECC4 | | | | |
| AN27 | MemAddr02 | AP27 | MemAddr00 | | | | |
| AN28 | MemAddr03 | AP28 | MemClkOut1 | | | | |
| AN29 | MemAddr05 | AP29 | GND | | | | |
| AN30 | MemAddr08 | AP30 | MemAddr06 | | | | |
| AN31 | BA0 | AP31 | MemAddr09 | | | | |
| AN32 | OV _{DD} | AP32 | MemAddr12 | | | | |
| AN33 | GND | AP33 | GND | | | | |
| AN34 | GND | AP34 | GND | | | | |

SIGNAL DESCRIPTION

The following table provides a summary of the number of package pins (balls) associated with each functional interface group.

PIN SUMMARY

Table 5. Pin Summary

| Group | No. of Pins |
|--------------------------|-------------|
| Nonmultiplexed Signals | 256 |
| Multiplexed Signals | 85 |
| Total Signal Pins | 341 |
| AV _{DD} | 1 |
| OV _{DD} | 49 |
| V _{DD} | 24 |
| Gnd | 65 |
| Gnd (and thermal) | 100 |
| Reserved | 0 |
| Total Pins | 580 |

Multiplexed Pins

In the table “Signal Functional Description” on page 43, each external signal is listed along with a short description of the signal function. The signals are grouped together according to their function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In most cases, the signal name is shown in this table unaccompanied by multiplexed signal names that may be associated with it. In cases where multiplexed signals are in the same functional group, the names appear as a default signal followed by secondary signals in square brackets (for example, EMC0TxErr[EMC0Tx1En]). Active-low signals (for example, RAS) are marked with an overline. Any signal that is not the primary (default) signal on a multiplexed pin is shown in square brackets.

The active signal on a multiplexed pin is controlled by programming. It is expected that in any single application, a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

Multipurpose Pins

In addition to multiplexing, pins may also be multipurpose. An example of multi-purpose use occurs when the EBC peripheral controller address pins are used as outputs by the NPe405H to broadcast an address to external slave devices when the NPe405H has control of the external bus. However, when an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the NPe405H. In this example, the pins are also bidirectional, serving as both inputs and outputs.

Initialization Strapping

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 68). Note that the use of these pins for strapping is not considered multiplexing since the strapping function is not programmable.

Pull-up and Pull-down Resistors

Pull-up and pull-down resistors are used for strapping during reset and to retain unused or undriven inputs in an appropriate state. The recommended pull-up value of 3k Ω to +3.3V (10k Ω to +5V can be used on 5V tolerant I/Os) and pull-down value of 1k Ω to GND, applies only to individually terminated signals. To prevent possible damage to the device, I/Os capable of becoming outputs *must never* be tied together and terminated through a common resistor.

If your system-level test methodology permits, input-only signals can be connected together and terminated through either a common resistor or directly to +3.3V or GND. When a resistor is used, its value must ensure that the grouped I/Os reach a valid logic zero or logic one state when accounting for the total input current into the NPe405H.

Unused I/Os

Strapping of some pins may be necessary when they are unused. Although the NPe405H requires only the pull-up and pull-down terminations as specified in the “Signal Functional Description” on page 43, good design practice is to terminate all unused inputs or to configure I/Os such that they always drive. If unused, the peripheral, SDRAM, and PCI buses should be configured and terminated as follows:

- Peripheral interface—PerAddr00:31, PerData00:31, and all of the control signals are driven by default. Terminate PerReady high and PerError low.
- SDRAM—Program SDRAM0_CFG[EMDULR]=1 and SDRAM0_CFG[DCE]=1. This causes the NPe405H to actively drive all of the SDRAM address, data, and control signals.
- PCI—Configure the PCI controller to park on the bus and actively drive PCIAD31:0, PCIC3:0[BE3:0], and the remaining PCI control signals by doing the following:
 - Strap the NPe405H to disable the internal PCI arbiter.
 - Individually connect $\overline{\text{PCISerr}}$, $\overline{\text{PCIPErr}}$, $\overline{\text{PCITRDY}}$, and $\overline{\text{PCIStop}}$ through 3.3k Ω resistors to +3.3V.
 - Terminate $\overline{\text{PCIReq1:5}}$ to +3.3V.
 - Terminate $\overline{\text{PCIReq0[Gnt]}}$ to GND.

External Peripheral Bus Control Signals

All external peripheral bus control signals ($\overline{\text{PerCS0:7}}$, $\overline{\text{PerR/W}}$, $\overline{\text{PerWBE0:3}}$, $\overline{\text{PerOE}}$, $\overline{\text{PerWE}}$, $\overline{\text{PerBLast}}$, HoldAck, ExtAck) are set to the high-impedance state when $\overline{\text{ExtReset}}=0$. In addition, as detailed in the *PowerNP NPe405H Embedded Processor User's Manual*, the peripheral bus controller can be programmed via EBC0_CFG to float some of these control signals between transactions or when an external master owns the peripheral bus. As a result, a pull-up resistor should be added to those control signals where an undriven state may affect any devices receiving that particular signal.

The following table lists all of the I/O signals provided by the NPe405H. Please see “Signals Listed Alphabetically” on page 15 for the pin number to which each signal is assigned. In cases where a multiplexed signal (indicated by the square brackets) is shown without the other signals that are assigned to that pin, you can see what the other signals are by referring to the same table.

SIGNAL FUNCTIONAL DESCRIPTION

Table 6. Signal Functional Description (Sheet 1 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|----------------------|---|-----|-------------------------|-------|
| PCI Interface | | | | |
| PCIAD0:31 | PCI Address/Data bus. Multiplexed address and data bus | I/O | 5V tolerant 3.3V PCI | |
| PCIC3:0[BE3:0] | PCI bus command or Byte Enable | I/O | 5V tolerant 3.3V PCI | |
| PCIParity | PCI Parity. Parity is even across PCIAD0:31 and PCIC0:3[BE0:3]. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD0:31 is responsible for driving PCIParity on the next PCI bus clock. | I/O | 5V tolerant 3.3V PCI | |
| PCIFrame | Driven by the current PCI bus master to indicate the beginning and duration of a PCI access. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIIRDY | Driven by the current PCI bus master. Assertion of PCIIRDY indicates that the PCI initiator is ready to transfer data. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCITRDY | The target of the current PCI transaction drives PCITRDY. Assertion of PCITRDY indicates that the PCI target is ready to transfer data. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIStop | The target of the current PCI transaction can assert PCIStop to indicate to the requesting PCI master that it wants to end the current transaction. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIDevSel | Driven by the target of the current PCI transaction. A PCI target asserts PCIDevSel when it has decoded an address and command encoding and claims the transaction. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIIDSel | Used during configuration cycles to select the PCI slave interface for configuration | I | 5V tolerant 3.3V PCI | 5 |
| PCISErr | Used for reporting address parity errors or catastrophic failures detected by a PCI target. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIPErr | Used for reporting data parity errors on PCI transactions. PCIPErr is driven active by the device receiving PCIAD0:31, PCIC0:3[BE0:3], and PCIParity, two PCI clocks following the data in which bad parity is detected. | I/O | 5V tolerant 3.3V PCI | 4 |
| PCIClk | Used as the asynchronous PCI clock. | I | 5V tolerant 3.3V PCI | |
| PCIReset | PCI specific reset | O | 5V tolerant 3.3V PCI | |
| PCIINT | PCI Interrupt. Open-drain output (two states; 0 or open circuit). | O | 5V tolerant 3.3V PCI | |
| PCIReq0[Gnt] | Req0 when internal arbiter is used, or Gnt when external arbiter is used. IF PCI bus is used, pull this signal up; otherwise, pull down. | I | 5V tolerant 3.3V PCI | |
| PCIReq1:5 | Used as PCIReq1:5 input when internal arbiter is used | I | 5V tolerant 3.3V PCI | 4 |
| PCIGnt0[Req] | Gnt0 when internal arbiter is used, or Req when external arbiter is used | O | 5V tolerant 3.3V PCI | |

Table 6. Signal Functional Description (Sheet 2 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|---------------------------|--|-----|----------------------------|-------|
| PCIGnt1:5 | PCIGnt1:5 output when internal arbiter is used. | O | 5V tolerant 3.3V PCI | |
| HDLCEX Interface | | | | |
| HDLCEXTxCIk | Transmit Clock | I | 3.3V LVTTTL | |
| HDLCEXTxFS | Transmit Frame Synchronization | I | 3.3V LVTTTL | |
| HDLCEXTxDataA | Transmit Data port A | O | 3.3V LVTTTL | |
| HDLCEXTxDataB | Transmit Data port B | O | 3.3V LVTTTL | |
| HDLCEXRxCIk | Receive Clock | I | 3.3V LVTTTL | |
| HDLCEXRxFS | Receive Frame Synchronization | I | 3.3V LVTTTL | |
| HDLCEXRxDataA | Receive Data port A | I | 3.3V LVTTTL | |
| HDLCEXRxDataB | Receive Data port B | I | 3.3V LVTTTL | |
| [HDLCEXTxEnA] | Transmit Enable port A | O | 5V tolerant 3.3V LVTTTL | |
| [HDLCEXTxEnB] | Transmit Enable port B | O | 5V tolerant 3.3V LVTTTL | |
| HDLCMP Interface | | | | |
| HDLCMPTxCIk0:3 | Transmit Clock signal that controls the transmit bit rate | O | 3.3V LVTTTL | |
| [HDLCMPTxCIk4:7] | Transmit Clock signal that controls the transmit bit rate | O | 5V tolerant 3.3V LVTTTL | |
| HDLCMPTxData0:3 | Transmit Data signal | O | 3.3V LVTTTL | |
| [HDLCMPTxData4:7] | Transmit Data signal | O | 5V tolerant 3.3V LVTTTL | |
| [HDLCMPTxEn0:7] | Transmit Data Enable signal that controls when the external buffer is tri-stated | O | 5V tolerant 3.3V LVTTTL | |
| HDLCMPRxCIk0:3 | Receive Clock signal that controls the receive bit rate | I | 3.3V LVTTTL | |
| [HDLCMPRxCIk4:7] | Receive Clock signal that controls the receive bit rate | I | 5V tolerant 3.3V LVTTTL | |
| HDLCMPRxData0:3 | Receive Data signal | I | 3.3V LVTTTL | |
| [HDLCMPRxData4:7] | Receive Data signal | I | 5V tolerant 3.3V LVTTTL | |
| Ethernet Interface | | | | |
| EMC0MDCIk | Management Data Clock. The MDCIk is sourced to the PHY. Management information is transferred synchronously with respect to this clock (MII, RMII, and SMII). | O | 3.3V LVTTTL | |
| EMC0MDIO | Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information (MII, RMII, and SMII). | I/O | 5V tolerant 3.3V LVTTTL | 1, 4 |

Table 6. Signal Functional Description (Sheet 3 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|--|---|-----|----------------------------|-------|
| EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0][EMC0Tx2D] EMC0TxD3[EMC0Tx1D1][EMC0Tx3D] | Transmit Data. A nibble wide data bus towards the net. The data is synchronous with PHY0TxClk (MII 0[RMII 0, 1][SMII 0, 1, 2, 3]). | O | 3.3V LVTTTL | |
| [EMC1TxD0][EMC1Tx2D0] [EMC1TxD1][EMC1Tx2D1] [EMC1TxD2][EMC1Tx3D0] [EMC1TxD3][EMC1Tx3D1] | RMII Transmit Data (MII 1[RMII 2, 3]). | O | 5V tolerant 3.3V LVTTTL | |
| EMC0TxEn[EMC0Tx0En][EMC0Sync] | Transmit Enable. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous with PHYTxClk (MII 0[RMII 0]). or SMII Sync. | O | 3.3V LVTTTL | |
| EMC0TxErr[EMC0Tx1En] | Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY0TxClk. It informs the PHY that an error was detected (MII 0). or Transmit Enable [RMII 1]. | O | 3.3V LVTTTL | |
| [EMC1TxEn][EMC1Tx2En] | Transmit Enable ([MII 1][RMII 2]). | O | 5V tolerant 3.3V LVTTTL | |
| [EMC1TxErr][EMC1Tx3En] | Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY1TxClk. It informs the PHY that an error was detected ([MII 1]). or Transmit Enable [RMII 3]. | O | 5V tolerant 3.3V LVTTTL | |
| PHY0Col[PHY0Rx1Er] | Collision [receive error] signal from the PHY. This is an asynchronous signal (MII 0). or Receive Error ([RMII 1]). | I | 5V tolerant 3.3V LVTTTL | |
| PHY0CrS[PHY0CrS0DV] | Carrier Sense signal from the PHY. This is an asynchronous signal (MII 0). or Carrier sense data valid ([RMII 0]). | I | 5V tolerant 3.3V LVTTTL | 1, 5 |
| PHY0RxClk | Receiver medium clock. This signal is generated by the PHY (MII 0). | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| PHY0Rx0D0[PHY0Rx0D0][PHY0Rx0D] PHY0Rx0D1[PHY0Rx0D1][PHY0Rx1D] PHY0Rx0D2[PHY0Rx1D0][PHY0Rx2D] PHY0Rx0D3[PHY0Rx1D1][PHY0Rx3D] | Received Data. This is a nibble wide bus from the PHY. The data is synchronous with PHY0RxClk (MII 0[RMII 0, 1][SMII 0, 1, 2, 3]). | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| [PHY1Rx0D0][PHY1Rx2D0] [PHY1Rx0D1][PHY1Rx2D1] [PHY1Rx0D2][PHY1Rx3D0] [PHY1Rx0D3][PHY1Rx3D1] | Receive Data (MII 1[RMII 2, 3]). | I | 5V tolerant 3.3V LVTTTL | |

Table 6. Signal Functional Description (Sheet 4 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|------------------------|--|-----|----------------------------|-------|
| PHY0RxDV[PHY0CrS1DV] | Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception (MII 0). or Carrier sense data valid ([RMII 1]) | I | 5V tolerant 3.3V LVTTTL | 1, 5 |
| PHY0RxErr[PHY0Rx0Er] | Receive Error. This signal comes from the PHY and is synchronous with PHY0RxClk (MII 0 [RMII 0]). | I | 5V tolerant 3.3V LVTTTL | 1, 5 |
| PHY0TxClk[PHY0RefClk] | Transmit medium clock. This signal is generated the PHY ([MII 0]). or Reference Clock [RMII and SMII]. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| [PHY1Col][PHY1Rx3Er] | Collision [receive error] signal from the PHY. This is an asynchronous signal ([MII 1]). or Receive Error. This signal comes from the PHY and is synchronous with PHY1RxClk ([RMII 3]). | I | 5V tolerant 3.3V LVTTTL | 1, 5 |
| [PHY1CrS][PHY1CrS2DV] | Carrier Sense signal from the PHY. This is an asynchronous signal ([MII 1]). or Carrier Sense Data Valid ([RMII 2]). | I | 5V tolerant 3.3V LVTTTL | |
| [PHY1RxClk] | Receiver medium clock. This signal is generated by the PHY ([MII 1]). | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| [PHY1RxDV][PHY1CrS3DV] | Receive Data Valid ([MII 1]). or Carrier Sense Data Valid ([RMII 3]). | i | 5V tolerant 3.3V LVTTTL | |
| [PHY1RxErr][PHY1Rx2Er] | Receive Error. This signal comes from the PHY and is synchronous with PHY1RxClk ([MII 1][RMII 2]). | I | 5V tolerant 3.3V LVTTTL | |
| [PHY1TxClk] | Transmit medium clock. This signal is generated the PHY ([MII 1]). | I | 5V tolerant 3.3V LVTTTL | 1, 4 |

SDRAM Interface

| | | | | |
|-------------------------|---|-----|-------------|--|
| MemAddr00:31 | Memory Data bus Notes: 1. MemAddr00 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb). | I/O | 3.3V LVTTTL | |
| MemAddr12:00 | Memory Address bus. Notes: 1. MemAddr12 is the most significant bit (msb). 2. MemAddr00 is the least significant bit (lsb). | O | 3.3V LVTTTL | |
| BA1:0 | Bank Address supporting up to 4 internal banks | O | 3.3V LVTTTL | |
| $\overline{\text{RAS}}$ | Row Address Strobe. | O | 3.3V LVTTTL | |
| $\overline{\text{CAS}}$ | Column Address Strobe. | O | 3.3V LVTTTL | |
| DQM0:3 | DQM for byte lane 0 (MemAddr00:7), 1 (MemAddr08:15), 2 (MemData16:23), and 3 (MemData24:31) | O | 3.3V LVTTTL | |

Table 6. Signal Functional Description (Sheet 5 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|--|--|-----|----------------------------|---------|
| DQMCB | DQM for ECC check bits. | O | 3.3V LVTTTL | |
| ECC0:7 | ECC check bits 0:7. | I/O | 3.3V LVTTTL | |
| $\overline{\text{BankSel0:3}}$ | Select up to four external SDRAM banks. | O | 3.3V LVTTTL | |
| $\overline{\text{WE}}$ | Write Enable. | O | 3.3V LVTTTL | |
| ClkEn0:1 | SDRAM Clock Enable. | O | 3.3V LVTTTL | |
| MemClkOut0:1 | Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attachment without requiring this signal to be repowered by a PLL or zero-delay buffer. | O | 3.3V LVTTTL | |
| External Slave Peripheral Bus Interface | | | | |
| PerData00:31 | External peripheral data bus when not in external master mode, otherwise used by external master. Note: PerData00 is the most significant bit (msb) on this bus. | I/O | 5V tolerant 3.3V LVTTTL | 1 |
| PerAddr00:31 | External peripheral address bus when not in external master mode, otherwise used by external master. | I/O | 5V tolerant 3.3V LVTTTL | 1 |
| PerPar0:3 | External peripheral byte parity signals. | I/O | 5V tolerant 3.3V LVTTTL | 1 |
| $\overline{\text{PerWBE0:3}}$ | Peripheral write-bte enable. Byte-enables which are valid for an entire cycle or write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. Used by either external bus controller or DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface. | I/O | 5V tolerant 3.3V LVTTTL | 1, 2, 7 |
| $[\overline{\text{PerWE}}]$ | Peripheral write enable. Low when any of the four $\overline{\text{PerWBE}}$ signals are low. | I/O | 5V tolerant 3.3V LVTTTL | 7 |
| $\overline{\text{PerCS0}}$ $[\overline{\text{PerCS1:7}}]$ | Peripheral Chip Selects | O | 5V tolerant 3.3V LVTTTL | |
| $\overline{\text{PerOE}}$ | Peripheral output enable. Used by either the external bus controller or the DMA controller depending upon the type of transfer involved. When the NPe405H is the bus master, it enables the peripherals to drive the bus. | O | 5V tolerant 3.3V LVTTTL | 7 |
| PerR $\overline{\text{W}}$ | Peripheral read/write. Used when not in external master mode by either the external bus controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of transfer. | I/O | 5V tolerant 3.3V LVTTTL | 1 |
| PerReady | Indicates peripheral is ready to transfer data. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $\overline{\text{PerBLast}}$ | Peripheral burst last. Used to indicate the last transfer of a memory access. | I/O | 5V tolerant 3.3V LVTTTL | 1, 7 |
| PerClk | Peripheral Clock. Used by an external master and by synchronous peripheral slaves. | O | 5V tolerant 3.3V LVTTTL | |
| PerErr | Used to indicate errors from peripherals. | I | 5V tolerant 3.3V LVTTTL | 1, 5 |

Table 6. Signal Functional Description (Sheet 6 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|--|---|-----|----------------------------|-------|
| $\overline{\text{DMAReq0:3}}$ | DMA request. Used by peripheral slaves to request a data transfer. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $\overline{\text{DMAAck0:3}}$ | DMA acknowledge. Used to indicate to peripherals that data transfer is complete. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register. | O | 5V tolerant 3.3V LVTTTL | |
| $\overline{\text{EOT0:3}}/\overline{\text{TC0:3}}$ | End Of Transfer/Terminal Count. Indication by peripherals that all data has been transferred, or by DMA controller that programmed amount of data has been transferred. Following a system reset, the default mode of the signals is active-low. They may be programmed to active-high using the DMA0_POL register. | I/O | 5V tolerant 3.3V LVTTTL | 1 |

Table 6. Signal Functional Description (Sheet 7 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|---|---|-----|------------------------------|-------|
| External Master Peripheral Interface | | | | |
| $\overline{\text{ExtReset}}$ | Peripheral Reset. Used by an external master and synchronous peripheral slaves. | O | 5V tolerant 3.3V LVTTTL | |
| HoldReq | Hold Request. Used by an external master to request ownership of the peripheral bus. | I | 5V tolerant 3.3V LVTTTL | 1, 5 |
| HoldAck | Hold Acknowledge. Used by the NPe405H to transfer ownership of peripheral bus to an external master. | O | 5V tolerant 3.3V LVTTTL | 6 |
| $\overline{\text{ExtReq}}$ | External Request. Used by an external master to indicate it is prepared to transfer data. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $\overline{\text{ExtAck}}$ | External Acknowledgement. Used by the NPe405H to indicate that a data transfer occurred. | O | 5V tolerant 3.3V LVTTTL | 6 |
| HoldPri | Hold Primary. Used by an external master to indicate the priority of a given transfer (0 = high, 1 = low). | I | 5V tolerant 3.3V LVTTTL | 1 |
| BusReq | Bus Request. Used when the NPe405H needs to regain control of peripheral interface from an external Master. | O | 5V tolerant 3.3V LVTTTL | |
| Internal Peripheral Interface | | | | |
| UARTSerCik | Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1. | I | 5V tolerant 3.3V LVTTTL | 1 |
| UART0_Rx | UART0 Receive data. | I | 5V tolerant 3.3V LVTTTL | 1 |
| UART0_Tx | UART0 Transmit data. | O | 5V tolerant 3.3V LVTTTL | |
| $[\overline{\text{UART0_DCD}}]$ | UART0 Data Carrier Detect. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $[\overline{\text{UART0_DSR}}]$ | UART0 Data Set Ready. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $[\overline{\text{UART0_CTS}}]$ | UART0 Clear To Send. | I | 5V tolerant 3.3V LVTTTL | 1 |
| $[\overline{\text{UART0_DTR}}]$ | UART0 Data Terminal Ready. | O | 5V tolerant 3.3V LVTTTL | |
| $[\overline{\text{UART0_RTS}}]$ | UART0 Request To Send. | O | 5V tolerant 3.3V LVTTTL | |
| $[\overline{\text{UART0_RI}}]$ | UART0 Ring Indicator. | I | 5V tolerant 3.3V LVTTTL r | 1 |

Table 6. Signal Functional Description (Sheet 8 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|----------------------------------|---|-----|----------------------------|-------|
| UART1_Rx | UART1 Receive data. | I | 5V tolerant 3.3V LVTTTL | 1 |
| UART1_Tx | UART1 Transmit data. | O | 5V tolerant 3.3V LVTTTL | 6 |
| $\overline{\text{[UART1_DCD]}}$ | UART1 Data Carrier Detect. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| $\overline{\text{[UART1_DSR]}}$ | UART1 Data Set Ready. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| $\overline{\text{[UART1_CTS]}}$ | UART1 Clear To Send. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| $\overline{\text{[UART1_DTR]}}$ | UART1 Data Terminal Ready. | O | 5V tolerant 3.3V LVTTTL | |
| $\overline{\text{[UART1_RTS]}}$ | UART1 Request To Send. | O | 5V tolerant 3.3V LVTTTL | |
| $\overline{\text{[UART1_RI]}}$ | UART1 Ring Indicator. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| IIC_SCL[IIECSCL] | IIC [Initialization PROM] Serial Clock. | I/O | 5V tolerant 3.3V LVTTTL | 1, 2 |
| IIC_SDA[IIECSDA] | IIC [Initialization PROM] Serial Data. | I/O | 5V tolerant 3.3V LVTTTL | 1, 2 |
| Interrupts Interface | | | | |
| [IRQ0:6] | Interrupt Requests. | I | 5V tolerant 3.3V LVTTTL | 1 |
| JTAG Interface | | | | |
| TDI | Test Data In. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| TMS | Test Mode Select. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| TDO | Test Data Out. | O | 5V tolerant 3.3V LVTTTL | |
| TCK | Test Clock. | I | 5V tolerant 3.3V LVTTTL | 1, 4 |
| $\overline{\text{TRST}}$ | Test Reset. $\overline{\text{TRST}}$ must be low at power-on to reset the JTAG boundary scan state machine. | I | 5V tolerant 3.3V LVTTTL | 5 |

Table 6. Signal Functional Description (Sheet 9 of 9)

Notes:

1. Receiver input has hysteresis.
2. Must pull up. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
3. Must pull down. See “Pull-up and Pull-down Resistors” on page 42 for recommended termination values.
4. If not used, must pull up.
5. If not used, must pull down.
6. Strapping input during reset; pull up or pull down as required.
7. Pull-up may be required. See “External Peripheral Bus Control Signals” on page 42.

| Signal Name | Description | I/O | Type | Notes |
|------------------------------|--|-----|-------------------------|-------|
| System Interface | | | | |
| SysClk | Main System Clock input. | I | 3.3V Analog Wire w/ESD | |
| $\overline{\text{SysReset}}$ | Main System Reset. | I/O | 5V tolerant 3.3V LVTTTL | 1, 2 |
| SysErr | Set to 1 when a Machine Check is generated. | O | 5V tolerant 3.3V LVTTTL | |
| $\overline{\text{Halt}}$ | Halt from external debugger. | I | 5V tolerant 3.3V LVTTTL | 1 |
| GPIO0_00:31 | System General Purpose I/O. | I/O | 5V tolerant 3.3V LVTTTL | |
| GPIO1_00:31 | Communications General Purpose I/O. | I/O | 5V tolerant 3.3V LVTTTL | |
| TestEn | Test Enable. Used only for manufacturing tests. Pull down for normal operation. | I | 3.3V LVTTTL Rcvr w/PD | |
| TmrClk | This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range). | I | 5V tolerant 3.3V LVTTTL | 1 |
| Trace Interface | | | | |
| [TS1E] [TS2E] | Even Trace execution status. To access this function, software must toggle a DCR bit. | O | 5V tolerant 3.3V LVTTTL | |
| [TS1O] [TS2O] | Odd Trace execution status. To access this function, software must toggle a DCR bit. | O | 5V tolerant 3.3V LVTTTL | |
| [TS3:6] | Trace Status. To access this function, software must toggle a DCR bit. | O | 5V tolerant 3.3V LVTTTL | |
| [TrcClk] | Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit. | O | 5V tolerant 3.3V LVTTTL | 1 |
| Power Pins | | | | |
| GND | Ground Note: J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls. | I | Hardwire | |
| V _{DD} | Logic voltage—2.5V | I | Hardwire | |
| OV _{DD} | Output driver voltage—3.3V | I | Hardwire | |
| AV _{DD} | Filtered PLL voltage—2.5V | I | 3.3V DC Wire w/ESD | |
| Other Pins | | | | |
| Reserved | Do not connect signals, voltage, or ground to these pins. | n/a | n/a | |

ABSOLUTE MAXIMUM RATINGS

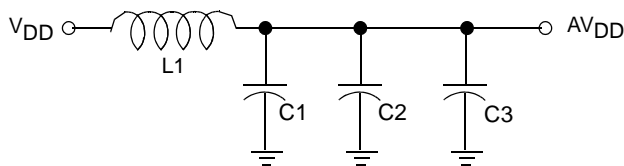
Table 7. Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

| Characteristic | Symbol | Value | Unit |
|---------------------------------------|-----------|-----------------------------|------|
| Supply Voltage (Internal Logic) | V_{DD} | 0 to +2.7 | V |
| Supply Voltage (I/O Interface) | OV_{DD} | 0 to +3.6 | V |
| PLL Supply Voltage ² | AV_{DD} | 0 to +2.7 | V |
| Input Voltage (3.3V LVTTTL receivers) | V_{IN} | -0.6 to ($OV_{DD} + 0.6$) | V |
| Input Voltage (5.0V LVTTTL receivers) | V_{IN} | -0.6 to ($OV_{DD} + 2.4$) | V |
| Storage Temperature Range | T_{STG} | -55 to +150 | °C |
| Case temperature under bias | T_C | -40 to +120 | °C |

Notes:

- All voltages are specified with respect to ground (GND).
- AV_{DD} should be derived from V_{DD} using the following circuit:



- $L1$ – 2.2 μ H SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700S)
- $C1$ – 3.3 μ F SMT tantalum
- $C2$ – 0.1 μ F SMT monolithic ceramic capacitor with X7R dielectric or equivalent
- $C3$ – 0.01 μ F SMT monolithic ceramic capacitor with X7R dielectric or equivalent

PACKAGE THERMAL SPECIFICATIONS

Table 8. Package Thermal Specifications

The NPe405H is designed to operate within a case temperature range of -40°C to 85°C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

| Package—Thermal Resistance | Symbol | Airflow ft/min (m/sec) | | | Unit |
|--|---------------|---------------------------|------------|------------|------|
| | | 0 (0) | 100 (0.51) | 200 (1.02) | |
| 35mm, 580-balls—Junction-to-Case | θ_{JC} | 2 | 2 | 2 | °C/W |
| 35mm, 580-balls—Case-to-Ambient ¹ | θ_{CA} | 13 | 12 | 11 | °C/W |

Notes:

- For a chip mounted on a JEDEC 2S2P card without a heat sink.
- For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
 - Case temperature, T_C , is measured at top center of case surface with device soldered to circuit board.
 - $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
 - $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

RECOMMENDED DC OPERATING CONDITIONS

Table 9. Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

1. PCI drivers meet PCI specifications.

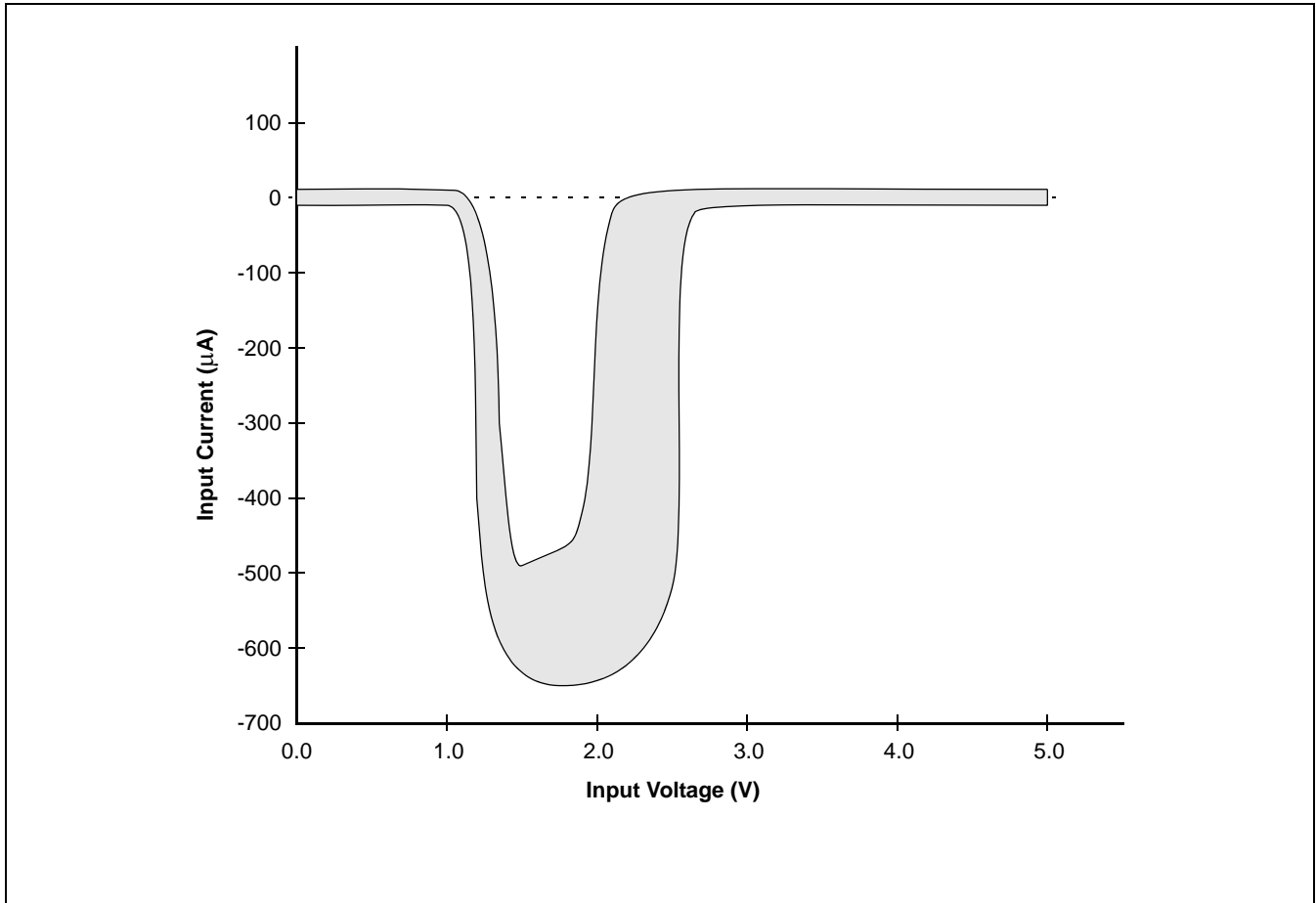
| Parameter | Symbol | Minimum | Typical | Maximum | Unit | Notes |
|---|---------------------|-------------|---------|------------------------|------|-------|
| Logic Supply Voltage | V _{DD} | +2.3 | +2.5 | +2.7 | V | |
| I/O Supply Voltage | OV _{DD} | +3.0 | +3.3 | +3.6 | V | |
| PLL Supply Voltage | AV _{DD} | +2.3 | +2.5 | +2.7 | V | |
| Input Logic High (3.3V LVTTTL receivers) | V _{IH} | +2.0 | | OV _{DD} | V | |
| Input Logic High (2.5V CMOS receivers) | V _{IH} | +1.7 | | V _{DD} | V | |
| Input Logic High (5.0V LVTTTL receivers) | V _{IH} | +2.0 | | +5.5 | V | |
| Input Logic Low | V _{IL} | 0 | | +0.8 | V | |
| Output Logic High | V _{OH} | +2.4 | | OV _{DD} | V | |
| Output Logic Low | V _{OL} | 0 | | +0.4 | V | |
| 3.3V I/O input current (no pull-up or pull-down) | I _{IL1} | | | ±10 | µA | |
| Input Current (with internal pull-down) | I _{IL2} | ±10 (@ 0V) | | 400 (@ 3.6V) | µA | |
| Input Current (with internal pull-up) | I _{IL3} | -250 (@ 0V) | | ±10 (@ 3.6V) | µA | |
| Input Max Allowable Overshoot (2.5V CMOS receivers) | V _{IMAO25} | | | V _{DD} + 0.6 | V | |
| Input Max Allowable Overshoot (3.3V LVTTTL receivers) | V _{IMAO3} | | | OV _{DD} + 0.6 | V | |
| Input Max Allowable Overshoot (5.0V LVTTTL receivers) | V _{IMAO5} | | | +5.5 | V | |
| Input Max Allowable Undershoot (3.3V or 5.0V receivers) | V _{IMAU} | - 0.6 | | | V | |
| Output Max Allowable Overshoot (3.3V or 5.0V receivers) | V _{OMAO} | | | OV _{DD} + 0.3 | V | |
| Output Max Allowable Undershoot (3.3V and 5.0V receivers) | V _{OMAU3} | - 0.6 | | | V | |
| Case Temperature | T _C | - 40 | | +85 | °C | |

Notes:

1. See "" on page 54

5 V-TOLERANT I/O INPUT CURRENT

Figure 3. 5V-Tolerant I/O Input Current



INPUT CAPACITANCE

Table 10. Input Capacitance

| Parameter | Symbol | Maximum | Unit | Notes |
|------------------------|------------------|---------|------|-------|
| 3.3V LVTTTL I/O) | C _{IN1} | 2.5 | pF | |
| 5V tolerant LVTTTL I/O | C _{IN2} | 3.5 | pF | |
| PCI I/O | C _{IN3} | 5.0 | pF | |
| RX only pins | C _{IN4} | 0.75 | pF | |

DC ELECTRICAL CHARACTERISTICS

Table 11. DC Electrical Characteristics

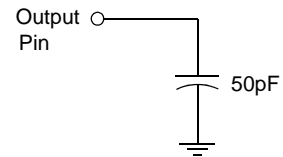
| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|--|------------------|---------|---------|------------------|------|
| Active Operating Current for V _{DD} @ 133MHz | I _{DD} | 599 | 669 | 740 | mA |
| Active Operating Current for V _{DD} @ 200MHz | I _{DD} | 755 | 843 | 928 | mA |
| Active Operating Current for V _{DD} @ 266MHz | I _{DD} | 964 | 1074 | 1183 | mA |
| Active Operating Current for OV _{DD} @ 133MHz | I _{ODD} | 77 | 89 | 99 | mA |
| Active Operating Current for OV _{DD} @ 200MHz | I _{ODD} | 89 | 102 | 112 | mA |
| Active Operating Current for OV _{DD} @ 266MHz | I _{ODD} | 97 | 111 | 123 | mA |
| Active Operating Current for AV _{DD} | I _{ADD} | 5.5 | 6 | 6.5 | mA |
| Active Operating Power @ 133MHz | P _{DD} | 1.6 | 2 | 2.4 ¹ | W |
| Active Operating Power @ 200MHz | P _{DD} | 2 | 2.4 | 2.9 ¹ | W |
| Active Operating Power @ 266MHz | P _{DD} | 2.5 | 3 | 3.6 ¹ | W |

Notes:

- Maximum power is characterized at V_{DD}=2.7V, OV_{DD}=3.6V, T_C=85°C, across the silicon process (worse case to best case), while running an application designed to maximize power consumption. The maximum power values are measured with the following clock rate combinations:
 - CPU=133.33MHz, PLB=66.66MHz, OPB=66.66MHz, EBC=33.33MHz, PCI=33.33MHz
 - CPU=200 MHz, PLB=100MHz, OPB=50MHz, EBC=50MHz, PCI=33.33MHz
 - CPU=266.66MHz, PLB=133.33MHz, OPB=66.66MHz, EBC=66.66MHz, PCI=33.33MHz

TEST CONDITIONS

Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at OV_{DD} = 3.00V and T_J = 85°C with the 50pF test load shown in the figure at right.



CLOCKING SPECIFICATIONS

Table 12. Clocking Specifications

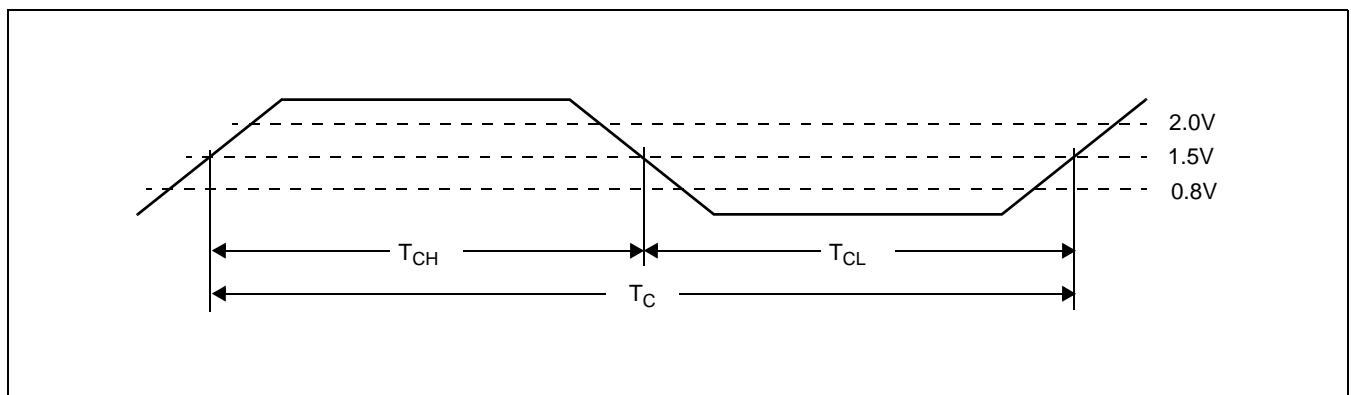
| Symbol | Parameter | Min | Max | Units |
|--------------------------------------|---|-----------------------|-----------------------|-------|
| SysClk Input | | | | |
| F_C | SysClk clock input frequency | 25 | 66.66 | MHz |
| T_C | SysClk clock period | 15 | 40 | ns |
| T_{CS} | Clock edge stability (phase jitter, cycle to cycle) | | 0.15 | ns |
| T_{CH} | Clock input high time | 40% of nominal period | 60% of nominal period | ns |
| T_{CL} | Clock input low time | 40% of nominal period | 60% of nominal period | ns |
| Note: Input slew rate > 2V/ns | | | | |
| MemClkOut Output | | | | |
| F_C | MemClkOut clock output frequency–133MHz | | 66.66 | MHz |
| T_C | MemClkOut clock period–133MHz | 15 | | ns |
| F_C | MemClkOut clock output frequency–200MHz | | 100 | MHz |
| T_C | MemClkOut clock period–200MHz | 10 | | ns |
| F_C | MemClkOut clock output frequency–266MHz | | 133.33 | MHz |
| T_C | MemClkOut clock period–266MHz | 7.5 | | ns |
| T_{CH} | Clock output high time | 45% of nominal period | 55% of nominal period | ns |
| T_{CL} | Clock output low time | 45% of nominal period | 55% of nominal period | ns |
| Other Clocks | | | | |
| F_C | VCO frequency | 400 | 800 | MHz |
| F_C | PLB frequency–133MHz | | 66.66 | MHz |
| F_C | PLB frequency–200MHz | | 100 | MHz |
| F_C | PLB frequency–266MHz | | 133.33 | MHz |
| F_C | OPB frequency–133MHz | | 50 ¹ | MHz |
| F_C | OPB frequency–200MHz | | 50 | MHz |
| F_C | OPB frequency–266MHz | | 50 ¹ | MHz |

Notes:

1. If HDLCEX is not used, the maximum OPB frequency is 66.66MHz.

CLOCKING WAVEFORM

Figure 4. Clocking Waveform



SPREAD SPECTRUM CLOCKING

Care must be taken when using a spread spectrum clock generator (SSCG) with the NPe405H. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the NPe405H the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the NPe405H with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board NPe405H peripherals impose more stringent requirements (see Note 1).
- Use the peripheral bus clock (PerClk) for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClkOut since it also tracks the modulation.

Please refer to the application note *Using a Spread Spectrum Clock Generator with the PowerPC 405GP* for additional details. This application note is available on the AMCC web site at <http://www.amcc.com>.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation.
2. Ethernet operation is unaffected.
3. IIC operation is unaffected.
4. The PCI clock specification for 66MHz allows a maximum frequency deviation of –1% at a modulation between 30kHz and 33kHz. PCI asynchronous mode is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the NPe405H meets the above requirements and does not adversely affect other aspects of the system.

PERIPHERAL INTERFACE CLOCK TIMINGS

Table 13. Peripheral Interface Clock Timings

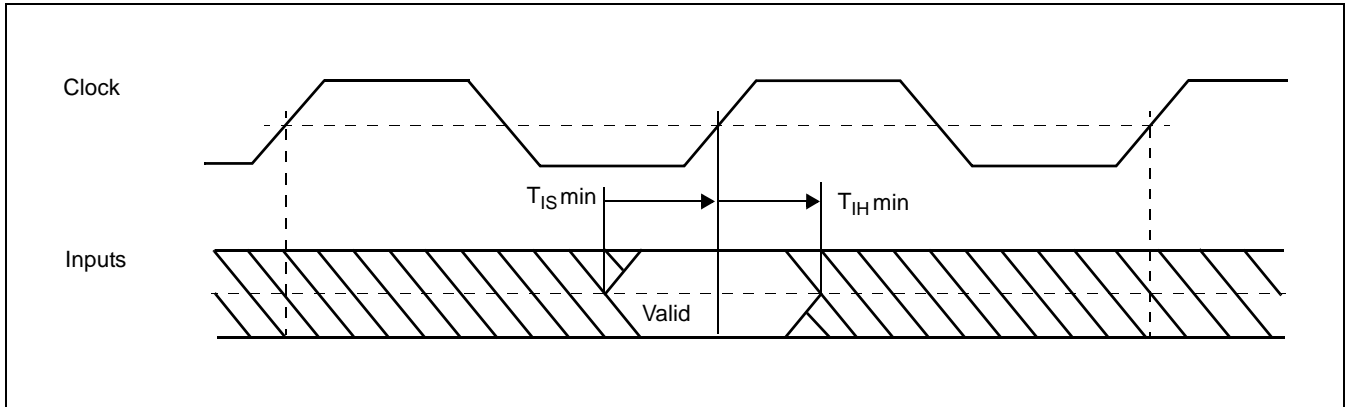
| Parameter | Min | Max | Units |
|--|-----------------------|--------------------------------|-------|
| PCIClk input frequency (asynchronous mode) | Note 2 | 66 | MHz |
| PCIClk period (asynchronous mode) | 15 | Note 2 | ns |
| PCIClk input high time | 40% of nominal period | 60% of nominal period | ns |
| PCIClk input low time | 40% of nominal period | 60% of nominal period | ns |
| EMC0MDCIk output frequency | – | 2.5 | MHz |
| EMC0MDCIk period | 400 | – | ns |
| EMC0MDCIk output high time | 160 | – | ns |
| EMC0MDCIk output low time | 160 | – | ns |
| PHY0TxClk input frequency | 2.5 | 25 | MHz |
| PHY0TxClk period | 40 | 400 | ns |
| PHY0TxClk input high time | 35% of nominal period | – | ns |
| PHY0TxClk input low time | 35% of nominal period | – | ns |
| PHY0RxClk input frequency | 2.5 | 25 | MHz |
| PHY0RxClk period | 40 | 400 | ns |
| PHY0RxClk input high time | 35% of nominal period | – | ns |
| PHY0RxClk input low time | 35% of nominal period | – | ns |
| PerClk output frequency–133MHz | – | 33.33 | MHz |
| PerClk period–133MHz | 30 | – | ns |
| PerClk output frequency–200MHz | – | 50 | MHz |
| PerClk period–200MHz | 20 | – | ns |
| PerClk output frequency–266MHz) | – | 66.66 | MHz |
| PerClk period–266MHz | 15 | – | ns |
| PerClk output high time | 45% of nominal period | 55% of nominal period | ns |
| PerClk output low time | 45% of nominal period | 55% of nominal period | ns |
| UARTSerClk input frequency (Note 1) | – | 1000/(2T _{OPB} + 2ns) | MHz |
| UARTSerClk period | 2T _{OPB} + 2 | – | ns |
| UARTSerClk input high time | T _{OPB} + 1 | – | ns |
| UARTSerClk input low time | T _{OPB} + 1 | – | ns |
| TmrClk input frequency–133MHz | – | 33.33 | MHz |
| TmrClk period–133MHz | 30 | – | ns |
| TmrClk input frequency–200MHz | – | 50 | MHz |
| TmrClk period–200MHz | 20 | – | ns |
| TmrClk input frequency–266MHz | – | 66.66 | MHz |
| TmrClk period–266MHz | 15 | – | ns |
| TmrClk input high time | 40% of nominal period | 60% of nominal period | ns |
| TmrClk input low time | 40% of nominal period | 60% of nominal period | ns |
| HDLCEXTxClk, HDLCEXRxCIk | 0 | 8.192 | MHz |
| HDLCMPTxClk, HDLCMPRxClk | – | 2.048 | MHz |

Notes:

1. T_{OPB} is the period in ns of the OPB clock. The maximum OPB clock frequency is 33.33 MHz for 133MHz parts, 50 MHz for 200MHz parts, and 66.66MHz for 266MHz parts.
2. In asynchronous PCI mode the minimum PCIClk frequency is 1/8 the PLB Clock. Refer to the NPe405H User's Manual for more information.

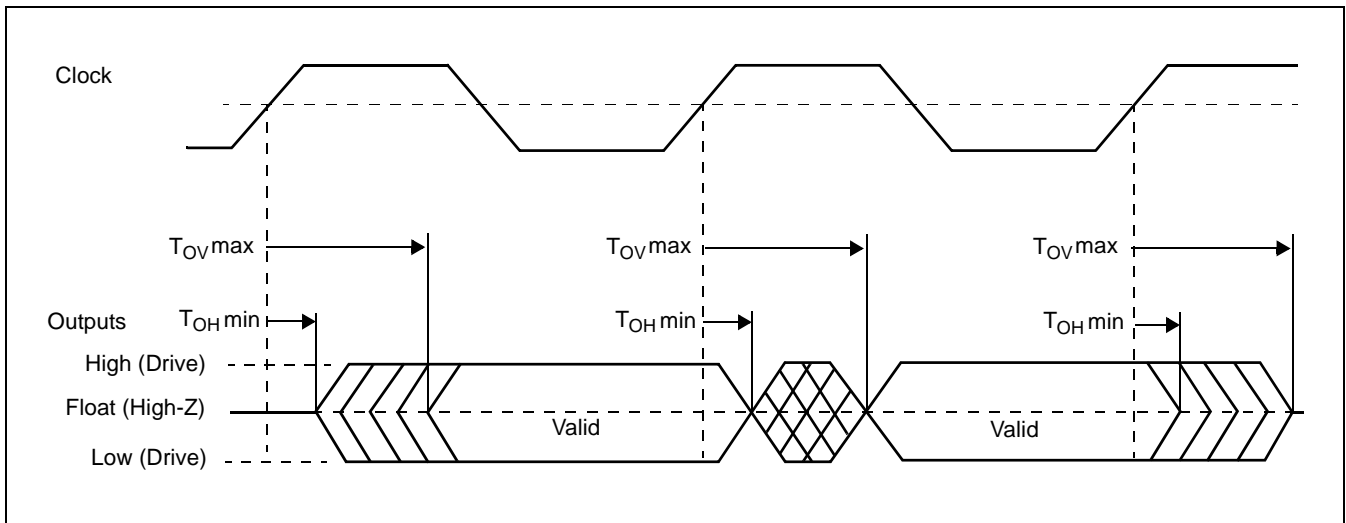
INPUT SETUP AND HOLD WAVEFORM

Figure 5. Input Setup and Hold Waveform



OUTPUT DELAY AND FLOAT TIMING WAVEFORM

Figure 6. Output Delay and Float Timing Waveform



I/O SPECIFICATIONS—ALL

Table 14. I/O Specifications—All (Sheet 1 of 2)

Notes:

1. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1 ns for 66MHz and 2 ns for 33MHz.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|--------------------------------------|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|--------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| PCI Interface | | | | | | | | |
| PCIAD00:31 | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIC0:3[BE3:0] | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIClk | n/a | n/a | n/a | n/a | n/a | n/a | | async |
| PCIDevSel | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIFrame | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIGnt0[Req] PCIGnt1:5 | n/a | n/a | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIIDSel | 3.0 | 0.0 | n/a | n/a | n/a | n/a | PCIClk | 6 |
| PCIINT[PerWE] | n/a | n/a | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | async |
| PCIIRDY | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIParity | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIPErr | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCIReq0[Gnt] PCIReq1:5 | 5.0 | 0.0 | n/a | n/a | n/a | n/a | PCIClk | 6 |
| PCIReset | n/a | n/a | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | |
| PCISErr | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | |
| PCIStop | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| PCITRDY | 3.0 | 0.0 | 6.0 | 2.0 | 0.5 | 1.5 | PCIClk | 6 |
| Internal Peripheral Interface | | | | | | | | |
| IIC_SCL | async | async | async | async | 17 | 11 | | |
| IIC_SDA | async | async | async | async | 17 | 11 | | |
| [UART0_CTS] | async | async | n/a | n/a | n/a | n/a | | |
| [UART0_DCD] | async | async | n/a | n/a | n/a | n/a | | |
| [UART0_DSR] | async | async | n/a | n/a | n/a | n/a | | |
| [UART0_DTR] | n/a | n/a | async | async | 12 | 8 | | |
| [UART0_RI] | async | async | n/a | n/a | n/a | n/a | | |
| [UART0_RTS] | n/a | n/a | async | async | 12 | 8 | | |
| UART0_Rx | async | async | n/a | n/a | n/a | n/a | | |
| UART0_Tx | n/a | n/a | async | async | 12 | 8 | | |
| [UART1_CTS] | async | async | n/a | n/a | n/a | n/a | | |
| [UART1_DCD] | async | async | n/a | n/a | n/a | n/a | | |
| [UART1_DSR] | async | async | n/a | n/a | n/a | n/a | | |
| [UART1_DTR] | n/a | n/a | async | async | 12 | 8 | | |
| [UART1_RI] | async | async | n/a | n/a | n/a | n/a | | |
| [UART1_RTS] | n/a | n/a | async | async | 12 | 8 | | |
| UART1_Rx | async | async | n/a | n/a | n/a | n/a | | |
| UART1_Tx | n/a | n/a | async | async | 12 | 8 | | |
| UARTSerCk | async | async | n/a | n/a | n/a | n/a | | |
| Interrupts Interface | | | | | | | | |
| [IRQ0:6] | async | async | n/a | n/a | n/a | n/a | | |

Table 14. I/O Specifications—All (Sheet 2 of 2)

Notes:

1. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1 ns for 66MHz and 2ns for 33MHz.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|-------------------------|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| JTAG Interface | | | | | | | | |
| TCK | async | async | n/a | n/a | n/a | n/a | | |
| TDI | async | async | n/a | n/a | n/a | n/a | | |
| TDO | n/a | n/a | async | async | 12 | 8 | | |
| TMS | async | async | n/a | n/a | n/a | n/a | | |
| TRST | async | async | n/a | n/a | n/a | n/a | | |
| System Interface | | | | | | | | |
| GPIO0:1 | na | na | na | na | 12 | 8 | | |
| Halt | async | async | n/a | n/a | n/a | n/a | | |
| SysClk | n/a | n/a | n/a | n/a | n/a | n/a | | |
| SysErr | n/a | n/a | 8.6 | 3.7 | 12 | 8 | | |
| SysReset | n/a | n/a | 7.4 | 3.3 | 12 | 8 | | |
| TestEn | dc | dc | n/a | n/a | n/a | n/a | | |
| TmrClk | n/a | n/a | async | async | n/a | n/a | | |

I/O SPECIFICATIONS(A)—133 AND 200 MHZ

Table 15. I/O Specifications—133 and 200MHz (Sheet 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-----------|----------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| Ethernet Interface | | | | | | | | |
| EMC0MDClk | n/a | n/a | n/a | n/a | 12 | 8 | | 1, async |
| EMC0MDIO | 100 | 0.0 | 1 OPB clock period + 10ns | 1 OPB Clock period | 12 | 8 | EMC0MDClk | 1 |
| EMC0TxD0:3 [EMC0Tx0:1D0:1] [EMC0Tx0:3D] | n/a | n/a | 12.4 7.0 5.0 | 4.1 2.3 1.5 | 12 | 8 | PHYTX | 1 |
| EMC0TxEn [EMC0Tx0En] [EMC0Sync] | n/a | n/a | 14.4 7.0 5.0 | 4.3 2.3 1.5 | 12 | 8 | PHYTX | 1 |
| EMC0TxErr[EMC0Tx1En] | n/a | n/a | 13.6[7.1] | 4.0[2.4] | 12 | 8 | PHYTX | 1 |
| [EMC1TxD0][EMC1Tx2D0] | n/a | n/a | [15.0][8.2] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD1][EMC1Tx2D1] | n/a | n/a | [15.0][8.3] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD2][EMC1Tx3D0] | n/a | n/a | [15.1][8.2] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD3][EMC1Tx3D1] | n/a | n/a | [15.0][8.2] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxEn][EMC1Tx2En] | n/a | n/a | [16.4][8.2] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxErr][EMC1Tx3En] | n/a | n/a | [16.5][8.3] | [4.8][2.5] | 12 | 8 | | |
| PHY0Col[PHY0Rx1Er] | async[1.1] | async[0.9] | n/a | n/a | n/a | n/a | | 1 |
| PHY0CrS[PHY0CrS0DV] | async[1.0] | async[1.3] | n/a | n/a | n/a | n/a | | 1 |
| PHY0RxCk | n/a | n/a | n/a | n/a | n/a | n/a | | 1, async |
| PHY0Rx0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:3D] | 1.7 1.1 1.1 | 1.6 0.9 0.2 | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0Rx0DV[PHY0CRS1DV] | 1.5[1.0] | 1.7[1.1] | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0RxErr[PHY0Rx0Er] | 1.5[1.1] | 1.6[1.0] | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0TxClk[PHY0RefClk] | n/a | n/a | n/a | n/a | n/a | n/a | | 1, async |
| [PHY1Rx0][PHY1Rx2D0] | [1.0][1.8] | [3.5][0.7] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx1][PHY1Rx2D1] | [1.3][2.2] | [3.0][0.3] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx2][PHY1Rx3D0] | [1.1][2.2] | [3.0][0.3] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx3][PHY1Rx3D1] | [1.0][1.9] | [3.3][0.7] | n/a | n/a | n/a | n/a | | |
| [PHY1Col][PHY1Rx3Er] | [1.4][2.2] | [2.2][0.3] | n/a | n/a | n/a | n/a | | |
| [PHY1CrS][PHY1CrS2DV] | [1.3][2.1] | [2.6][0.8] | n/a | n/a | n/a | n/a | | |
| [PHY1RxClk] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [PHY1Rx0DV] [PHY1CrS3DV] | [1.0] [2.1] | [2.6] [0.0] | n/a | n/a | n/a | n/a | | |
| [PHY1RxErr][PHY1Rx2Er] | [1.0][1.9] | [3.2][0.6] | n/a | n/a | n/a | n/a | | |
| [PHY1TxClk] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEX Interface | | | | | | | | |
| HDLCEXRxCk | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEXRxDatA:B | 27.7 | 1.4 | n/a | n/a | n/a | n/a | | |
| HDLCEXRxFs | 24.2 | 0.6 | n/a | n/a | n/a | n/a | | |

Table 15. I/O Specifications—133 and 200MHz (Sheet 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|-------------------------|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| HDLCEXTxClk | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEXTxDataA:B | n/a | n/a | 10.5 | 3.3 | 12 | 8 | | |
| HDLCEXTxFS | 24.4 | 0.7 | n/a | n/a | n/a | n/a | | |
| [HDLCEXTxEnA:B] | n/a | n/a | 9.9 | 3.0 | 12 | 8 | | |
| HDLCMP Interface | | | | | | | | |
| HDLCMPTxClk0:3 | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [HDLCMPTxClk4:7] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCMPTxData0:3 | n/a | n/a | 9.3 | 3.0 | 12 | 8 | | |
| [HDLCMPTxData4] | n/a | n/a | [9.9] | [3.3] | 12 | 8 | | |
| [HDLCMPTxData5] | n/a | n/a | [9.8] | [2.8] | 12 | 8 | | |
| [HDLCMPTxData6] | n/a | n/a | [9.8] | [3.0] | 12 | 8 | | |
| [HDLCMPTxData7] | n/a | n/a | [9.8] | [3.0] | 12 | 8 | | |
| [HDLCMPTxEn0] | n/a | n/a | [10.0] | [2.9] | 12 | 8 | | |
| [HDLCMPTxEn1] | n/a | n/a | [9.9] | [2.9] | 12 | 8 | | |
| [HDLCMPTxEn2] | n/a | n/a | [9.4] | [2.9] | 12 | 8 | | |
| [HDLCMPTxEn3] | n/a | n/a | [9.5] | [2.9] | 12 | 8 | | |
| [HDLCMPTxEn4] | n/a | n/a | [9.9] | [3.3] | 12 | 8 | | |
| [HDLCMPTxEn5] | n/a | n/a | [9.8] | [2.8] | 12 | 8 | | |
| [HDLCMPTxEn6] | n/a | n/a | [9.8] | [3.0] | 12 | 8 | | |
| [HDLCMPTxEn7] | n/a | n/a | [9.9] | [3.0] | 12 | 8 | | |
| HDLCMPRxClk0:3 | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxClk4:7] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCMPRxData0:3 | 22.8 | 0.5 | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData4] | [24.9] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData5] | [24.7] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData6] | [24.6] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData7] | [24.8] | [0.1] | n/a | n/a | n/a | n/a | | |
| Trace Interface | | | | | | | | |
| [TrcClk] | n/a | n/a | [12.2] | [2.5] | 12 | 8 | | |
| [TS1E] | n/a | n/a | [7.2] | [2.0] | 12 | 8 | | |
| [TS2E] | n/a | n/a | [7.2] | [2.0] | 12 | 8 | | |
| [TS1O] | n/a | n/a | [7.2] | [2.0] | 12 | 8 | | |
| [TS2O] | n/a | n/a | [7.2] | [2.0] | 12 | 8 | | |
| [TS3:4] | n/a | n/a | [7.2] | [2.0] | 12 | 8 | | |

Table 15. I/O Specifications—133 and 200MHz (Sheet 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-----------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| SDRAM Interface | | | | | | | | |
| BA1:0 | n/a | n/a | 7.1 | 1.1 | 19 | 12 | MemClkOut | 2, 3 |
| BankSel3:0 | n/a | n/a | 5.2 | 0.5 | 19 | 12 | MemClkOut | 3 |
| CAS | n/a | n/a | 6.8 | 1.0 | 19 | 12 | MemClkOut | 2, 3 |
| ClkEn0:1 | n/a | n/a | 4.5 | 0.5 | 40 | 25 | MemClkOut | 3 |
| DQM0:3 | n/a | n/a | 5.3 | 0.5 | 19 | 12 | MemClkOut | 3 |
| DQMCB | n/a | n/a | 5.3 | 0.5 | 19 | 12 | MemClkOut | 3 |
| ECC0:7 | 2.7 | 1.0 | 5.2 | 0.5 | 19 | 12 | MemClkOut | 3 |
| MemAddr12:00 | n/a | n/a | 7.0 | 1.0 | 19 | 12 | MemClkOut | 2, 3 |
| MemData00:31 | 2.8 | 1.0 | 5.2 | 0.5 | 19 | 12 | MemClkOut | 3 |
| RAS | n/a | n/a | 6.7 | 0.9 | 19 | 12 | MemClkOut | 2, 3 |
| WE | n/a | n/a | 5.5 | 1.5 | 19 | 12 | MemClkOut | 2, 3 |
| External Slave Peripheral Bus Interface | | | | | | | | |
| [DMAReq0:3] | [4.7] | [0.0] | n/a | n/a | n/a | n/a | PerClk | |
| [DMAAck0:3] | n/a | n/a | [8.5] | [1.0] | 12 | 8 | PerClk | |
| [EOT0:3/TC0:3] | [4.5] | [0.0] | [8.6] | [1.0] | 12 | 8 | PerClk | |
| PerAddr04:31 | 3.0 | 1.0 | 8.5 | 1.0 | 17 | 11 | PerClk | |
| PerBLast | 4.2 | 0.0 | 7.1 | 1.2 | 12 | 8 | PerClk | |
| PerCS0 | n/a | n/a | 8.7 | 1.0 | 12 | 8 | PerClk | |
| [PerCS1:7] | n/a | n/a | [8.7] | [1.0] | 12 | 8 | PerClk | |
| PerData00:31 | 5.7 | 1.0 | 9.5 | 1.3 | 17 | 11 | PerClk | |
| PerOE | n/a | n/a | 7.5 | 1.3 | 12 | 8 | PerClk | |
| PerPar0:3 | 3.4 | 0.0 | 8.9 | 1.1 | 17 | 11 | PerClk | |
| PerR/W | 4.5 | 0.0 | 7.5 | 1.2 | 12 | 8 | PerClk | |
| PerReady | 7.6 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| PerWBE0:3 | 3.0 | 0.0 | 7.7 | 1.3 | 12 | 8 | PerClk | |
| PerClk | n/a | n/a | -0.6 | -0.7 | 17 | 11 | PLB Clk | 5 |
| PerErr | 2.9 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| External Master Peripheral Bus Interface | | | | | | | | |
| BusReq | n/a | n/a | 6.8 | 1.2 | 12 | 8 | PerClk | |
| ExtAck | n/a | n/a | 6.9 | 1.2 | 12 | 8 | PerClk | |
| ExtReq | 4.5 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| ExtReset | n/a | n/a | 8.0 | 0.0 | 19 | 12 | PerClk | |
| HoldAck | n/a | n/a | 7.3 | 1.4 | 12 | 8 | PerClk | |
| HoldPri | 2.9 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| HoldReq | 4.0 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| IIC EEPROM Controller | | | | | | | | |
| IECSCL | aysnc | aysnc | aysnc | aysnc | 17 | 11 | | |
| IECSDA | aysnc | aysnc | aysnc | aysnc | 17 | 11 | | |

I/O SPECIFICATIONS(A)—266 MHZ

Table 16. I/O Specifications—266MHz (Sheet 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-----------|----------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| Ethernet Interface | | | | | | | | |
| EMC0MDClk | n/a | n/a | n/a | n/a | 12 | 8 | | 1, async |
| EMC0MDIO | 100 | 0.0 | 1 OPB clock period +10ns | 1 OPB clock period | 12 | 8 | EMC0MDCIk | 1 |
| EMC0TxD0:3 [EMC0Tx0:1D0:1] [EMC0Tx0:3D] | n/a | n/a | 9.0 [5.3] [4.6] | 4.1 [2.3] [1.5] | 12 | 8 | PHYTX | 1 |
| EMC0TxEn [EMC0Tx0En] [EMC0Sync] | n/a | n/a | 11.4 [5.2] [4.6] | 4.3 [2.3] [1.5] | 12 | 8 | PHYTX | 1 |
| EMC0TxErr[EMC0Tx1En] | n/a | n/a | 10.8[5.4] | 4.0[2.3] | 12 | 8 | PHYTX | 1 |
| [EMC1TxD0][EMC1Tx2D0] | n/a | n/a | [11.3][6.5] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD1][EMC1Tx2D1] | n/a | n/a | [10.9][6.1] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD2][EMC1Tx3D0] | n/a | n/a | [10.9][6.1] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxD3][EMC1Tx3D1] | n/a | n/a | [11.4][6.5] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxEn][EMC1Tx2En] | n/a | n/a | [12.7][6.2] | [4.8][2.5] | 12 | 8 | | |
| [EMC1TxErr][EMC1Tx3En] | n/a | n/a | [12.7][6.0] | [4.8][2.5] | 12 | 8 | | |
| PHY0Col[PHY0Rx1Er] | async[1.0] | async[0.7] | n/a | n/a | n/a | n/a | | 1 |
| PHY0CrS[PHY0CrS0DV] | async[1.0] | async[0.9] | n/a | n/a | n/a | n/a | | 1 |
| PHY0RxClk | n/a | n/a | n/a | n/a | n/a | n/a | | 1, async |
| PHY0Rx0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:3D] | 1.7 [1.1] [1.1] | 1.2 [0.7] [0.1] | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0Rx0DV[PHY0CRS1DV] | 1.5[1.1] | 1.2[0.8] | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0RxErr[PHY0Rx0Er] | 1.5[1.1] | 1.2[0.8] | n/a | n/a | n/a | n/a | PHYRX | 1 |
| PHY0TxClk[PHY0RefClk] | n/a | n/a | n/a | n/a | n/a | n/a | | 1, async |
| [PHY1Rx0][PHY1Rx2D0] | [1.0][1.5] | [2.6][0.5] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx1][PHY1Rx2D1] | [1.2][1.8] | [2.2][0.3] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx2][PHY1Rx3D0] | [1.1][1.8] | [2.2][0.3] | n/a | n/a | n/a | n/a | | |
| [PHY1Rx3][PHY1Rx3D1] | [0.9][1.5] | [2.5][0.5] | n/a | n/a | n/a | n/a | | |
| [PHY1Col][PHY1Rx3Er] | [1.4][2.0] | [1.5][0.2] | n/a | n/a | n/a | n/a | | |
| [PHY1CrS][PHY1CrS2DV] | [1.3][1.9] | [1.8][0.5] | n/a | n/a | n/a | n/a | | |
| [PHY1RxClk] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [PHY1Rx0DV] [PHY1CrS3DV] | 1.1 [1.8] | 2.0 [0.1] | n/a | n/a | n/a | n/a | | |
| [PHY1RxErr][PHY1Rx2Er] | [1.0][1.6] | [2.4][0.4] | n/a | n/a | n/a | n/a | | |
| [PHY1TxClk] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEX Interface | | | | | | | | |
| HDLCEXRxCIk | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEXRxDatA:B | 25.6 | 1.1 | n/a | n/a | n/a | n/a | | |
| HDLCEXRxFs | 24.2 | 0.5 | n/a | n/a | n/a | n/a | | |

Table 16. I/O Specifications—266MHz (Sheet 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|-------------------------|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| HDLCEXTxCIk | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCEXTxDataA:B | n/a | n/a | 7.2 | 3.1 | 12 | 8 | | |
| HDLCEXTxFS | 24.3 | 0.5 | n/a | n/a | n/a | n/a | | |
| [HDLCEXTxEnA:B] | n/a | n/a | [7.4] | [3.2] | 12 | 8 | | |
| HDLCMP Interface | | | | | | | | |
| HDLCMPTxCIk0:3 | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [HDLCMPTxCIk4:7] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCMPTxData0:3 | n/a | n/a | 7.3 | 3.1 | 12 | 8 | | |
| [HDLCMPTxData4] | n/a | n/a | [7.5] | [3.2] | 12 | 8 | | |
| [HDLCMPTxData5] | n/a | n/a | [7.4] | [2.9] | 12 | 8 | | |
| [HDLCMPTxData6] | n/a | n/a | [7.3] | [3.0] | 12 | 8 | | |
| [HDLCMPTxData7] | n/a | n/a | [7.4] | [3.0] | 12 | 8 | | |
| [HDLCMPTxEn0:3] | n/a | n/a | [7.4] | [2.8] | 12 | 8 | | |
| [HDLCMPTxEn4] | n/a | n/a | [7.5] | [3.2] | 12 | 8 | | |
| [HDLCMPTxEn5] | n/a | n/a | [7.8] | [3.1] | 12 | 8 | | |
| [HDLCMPTxEn6] | n/a | n/a | [7.4] | [3.0] | 12 | 8 | | |
| [HDLCMPTxEn7] | n/a | n/a | [7.4] | [3.0] | 12 | 8 | | |
| HDLCMPRxCIk0:3 | n/a | n/a | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxCIk4:7] | n/a | n/a | n/a | n/a | n/a | n/a | | |
| HDLCMPRxData0:3 | 21.1 | 0.4 | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData4] | [24.8] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData5] | [24.7] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData6] | [24.7] | [0.1] | n/a | n/a | n/a | n/a | | |
| [HDLCMPRxData7] | [24.8] | [0.1] | n/a | n/a | n/a | n/a | | |
| Trace Interface | | | | | | | | |
| [TrcClk] | n/a | n/a | [9.5] | [2.5] | 12 | 8 | | |
| [TS1E] | n/a | n/a | [5.9] | [2.0] | 12 | 8 | | |
| [TS2E] | n/a | n/a | [5.9] | [2.0] | 12 | 8 | | |
| [TS1O] | n/a | n/a | [5.9] | [2.0] | 12 | 8 | | |
| [TS2O] | n/a | n/a | [5.9] | [2.0] | 12 | 8 | | |
| [TS3:6] | n/a | n/a | [5.9] | [2.0] | 12 | 8 | | |

Table 16. I/O Specifications—266MHz (Sheet 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The SDRAM command interface is configurable through SDRAM0_TR[LDF] to provide a 2 to 4 cycle delay before the command is used by SDRAM. Output times in table are in cycle 1.
3. SDRAM I/O timings are specified relative to a MemClkOut terminated in a lumped 10pF load.
4. SDRAM interface hold times are guaranteed at the NPe405H package pin. System designers must use the NPe405H IBIS model (available from www.amcc.com) to ensure their clock distribution topology minimizes loading and reflections, and that the relative delays on clock wiring do not exceed the delays on other SDRAM signal wiring.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

| Signal | Input (ns) | | Output (ns) | | Output Current (mA) | | Clock | Notes |
|---|----------------------------------|---------------------------------|-----------------------------------|---------------------------------|---------------------|-----------------|-----------|-------|
| | Setup Time (T _{IS} min) | Hold Time (T _{IH} min) | Valid Delay (T _{OV} max) | Hold Time (T _{OH} min) | I/O H (maximum) | I/O L (minimum) | | |
| SDRAM Interface | | | | | | | | |
| BA1:0 | n/a | n/a | 6.0 | 1.8 | 19 | 12 | MemClkOut | 2, 3 |
| BankSel3:0 | n/a | n/a | 4.7 | 1.2 | 19 | 12 | MemClkOut | 3 |
| CAS | n/a | n/a | 5.7 | 1.7 | 19 | 12 | MemClkOut | 2, 3 |
| ClkEn0:1 | n/a | n/a | 4.2 | 1.2 | 40 | 25 | MemClkOut | 3 |
| DQM0:3 | n/a | n/a | 4.7 | 1.2 | 19 | 12 | MemClkOut | 3 |
| DQMCB | n/a | n/a | 4.7 | 1.2 | 19 | 12 | MemClkOut | 3 |
| ECC0:7 | 1.6 | 1.0 | 4.8 | 1.2 | 19 | 12 | MemClkOut | 3 |
| MemAddr12:00 | n/a | n/a | 6.0 | 1.7 | 19 | 12 | MemClkOut | 2, 3 |
| MemData00:31 | 1.6 | 1.0 | 4.8 | 1.2 | 19 | 12 | MemClkOut | 3 |
| RAS | n/a | n/a | 5.7 | 1.6 | 19 | 12 | MemClkOut | 2, 3 |
| WE | n/a | n/a | 6.2 | 2.2 | 19 | 12 | MemClkOut | 2, 3 |
| External Slave Peripheral Bus Interface | | | | | | | | |
| [DMAReq0:3] | [3.8] | [0.0] | n/a | n/a | n/a | n/a | PerClk | |
| [DMAAck0:3] | n/a | n/a | [6.1] | [1.0] | 12 | 8 | PerClk | |
| [EOT0:3/TC0:3] | [3.5] | [0.0] | [6.4] | [1.0] | 12 | 8 | PerClk | |
| PerAddr04:31 | 2.4 | 0.0 | 6.6 | 1.0 | 17 | 11 | PerClk | |
| PerBLast | 3.0 | 0.0 | 5.3 | 1.2 | 12 | 8 | PerClk | |
| PerCS0 | n/a | n/a | 5.3 | 1.2 | 12 | 8 | PerClk | |
| [PerCS1:7] | n/a | n/a | [7.1] | [1.0] | 12 | 8 | PerClk | |
| PerData00:31 | 4.4 | 1.0 | 7.2 | 1.2 | 17 | 11 | PerClk | |
| PerOE | n/a | n/a | 7.5 | 1.3 | 12 | 8 | PerClk | |
| PerPar0:3 | 2.7 | 0.0 | 6.9 | 1.1 | 17 | 11 | PerClk | |
| PerR/W | 3.5 | 0.0 | 5.6 | 1.2 | 12 | 8 | PerClk | |
| PerReady | 5.8 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| PerWBE0:3 | 2.4 | 0.0 | 5.7 | 1.3 | 12 | 8 | PerClk | |
| PerClk | n/a | n/a | 0.0 | 0.7 | 17 | 11 | PLB Clk | 5 |
| PerErr | 2.3 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| External Master Peripheral Bus Interface | | | | | | | | |
| BusReq | n/a | n/a | 5.0 | 1.2 | 12 | 8 | PerClk | |
| ExtAck | n/a | n/a | 5.1 | 1.2 | 12 | 8 | PerClk | |
| ExtReq | 3.5 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| ExtReset | n/a | n/a | 8.0 | 0.0 | 19 | 12 | PerClk | |
| HoldAck | n/a | n/a | 5.4 | 1.4 | 12 | 8 | PerClk | |
| HoldPri | 2.3 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| HoldReq | 3.2 | 0.0 | n/a | n/a | n/a | n/a | PerClk | |
| IIC EEPROM Controller | | | | | | | | |
| IECSCL | async | async | async | async | 17 | 11 | | |
| IECSDA | async | async | async | async | 17 | 11 | | |

INITIALIZATION

The following describes the method by which initial chip settings are established when a system reset occurs.

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to NPe405H start-up. The actual capture instant is the nearest SysClk edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. The recommended pull-up is 3kΩ to +3.3V or 10kΩ to +5V, the recommended pull-down is 1kΩ to GND. These pins are used for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options.

STRAPPING PIN ASSIGNMENTS

Table 17. Strapping Pin Assignments

| Function | Option | Ball Strapping | |
|--|-------------------------------------|---------------------------|------------------------|
| SEPROMPresent – Serial EEPROM connection to the IIC interface | | AJ33 (UART1_Tx) | |
| | Not connected | 0 | |
| | Connected | 1 | |
| | | H01 (HoldAck) | H02 (ExtAck) |
| When SEPROMPresent = 1, these pins set the high-order two bits of the EEPROM base address. | High order EEPROM base address bits | x | x |
| When SEPROMPresent = 0, these pins indicated the width of the boot ROM. | 8 bits | 0 | 0 |
| | 16 bits | 0 | 1 |
| | 32 bits | 1 | 0 |
| | reserved | 1 | 1 |

EEPROM

During reset, configuration values other than those obtained from the strapping pins can be read from a serial EEPROM connected to the IIC port. The association of bits in the EEPROM with the configuration values and their default values are covered in detail in the *PowerNP NPe405H Network Processor User's Manual*.

Caution: If SEPROMPresent is strapped to 1, and the EEPROM is not connected or is defective, the NPe405H will not boot up.

DOCUMENT REVISION HISTORY

| Revision | Date | Description |
|----------|----------|--|
| 1.01 | 04/18/07 | Updated SDRAM and MDIO timing in Tables 15 and 16. |
| 1.00 | 07/29/04 | Initial Release |



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