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SBAS426C – AUGUST 2008 – REVISED AUGUST 2009

ADS1246
ADS1247
ADS1248

24-Bit Analog-to-Digital Converters for Temperature Sensors

FEATURES

- 24 Bits, No Missing Codes
- Data Output Rates Up to 2kSPS
- Single-Cycle Settling for All Data Rates
- Simultaneous 50/60Hz Rejection at 20SPS
- 4 Differential/7 Single-Ended Inputs (ADS1248)
- 2 Differential/3 Single-Ended Inputs (ADS1247)
- Low-Noise PGA: 48nV at PGA = 128
- Matched Current Source DACs
- Very Low Drift Internal Voltage Reference: 10ppm/°C (max)
- Sensor Burnout Detection
- 4/8 General-Purpose I/Os (ADS1247/48)
- Internal Temperature Sensor
- Power Supply and V_{REF} Monitoring (ADS1247/48)
- Self and System Calibration
- SPI™-Compatible Serial Interface
- Analog Supply Unipolar (+2.7V to +5.25V)/Bipolar (±2.5V) Operation
- Digital Supply: +2.7V to +5.25V
- Operating Temperature –40°C to +125°C

APPLICATIONS

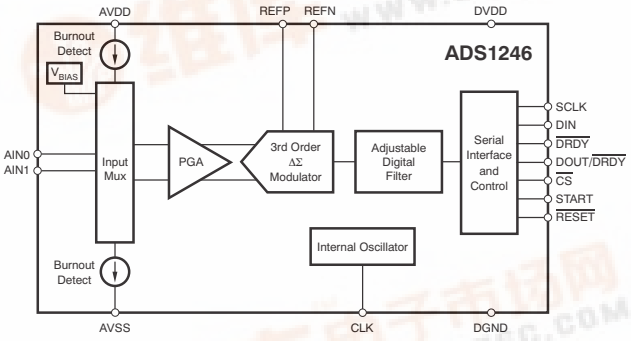
- Temperature Measurement
  - RTDs, Thermocouples, and Thermistors
- Pressure Measurement
- Industrial Process Control

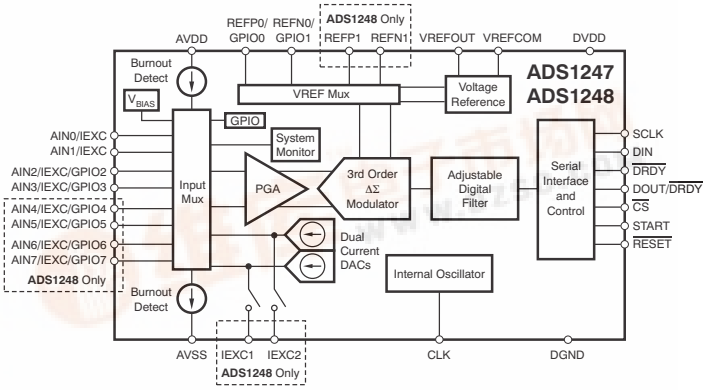
DESCRIPTION

The ADS1246, ADS1247, and ADS1248 are highly-integrated, precision, 24-bit analog-to-digital converters (ADCs). The ADS1246/7/8 feature an onboard, low-noise, programmable gain amplifier (PGA), a precision delta-sigma ADC with a single-cycle settling digital filter, and an internal oscillator. The ADS1247 and ADS1248 also provide a built-in, very low drift voltage reference with 10mA output capacity, and two matched programmable current digital-to-analog converters (DACs). The ADS1246/7/8 provide a complete front-end solution for temperature/bridge sensor applications including thermal couples, thermistors, RTDs, and strain-gauge applications.

An input multiplexer supports four differential inputs for the ADS1248, two for the ADS1247, and one for the ADS1246. In addition, the multiplexer has a sensor burnout detect, voltage bias for thermocouples, system monitoring, and general-purpose digital I/Os (ADS1247 and ADS1248). The onboard, low-noise PGA provides selectable gains of 1 to 128. The delta-sigma modulator and adjustable digital filter settle in only one cycle, for fast channel cycling when using the input multiplexer, and support data rates up to 2kSPS. For data rates of 20SPS or less, both 50Hz and 60Hz interference are rejected by the filter.

The ADS1246 is offered in a small TSSOP-16 package, the ADS1247 is available in a TSSOP-20 package, and the ADS1248 in a TSSOP-28 package. All three devices are rated over the extended specified temperature range of –40°C to +105°C.





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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	NUMBER OF INPUTS	VOLTAGE REFERENCE	DUAL SENSOR EXCITATION CURRENT SOURCES	PACKAGE-LEAD
ADS1246	1 Differential or 1 Single-Ended	External	NO	TSSOP-16
ADS1247	2 Differential or 3 Single-Ended	Internal or External	YES	TSSOP-20
ADS1248	4 Differential or 7 Single-Ended	Internal or External	YES	TSSOP-28

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	ADS1246, ADS1247, ADS1248	UNIT
AVDD to AVSS	–0.3 to +5.5	V
AVSS to DGND	–2.8 to +0.3	V
DVDD to DGND	–0.3 to +5.5	V
Input current	100, momentary	mA
	10, continuous	mA
Analog input voltage to AVSS	AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +125	°C
Storage temperature range	–60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS

Minimum/maximum specifications apply from –40°C to +105°C. Typical specifications are at +25°C. All specifications at AVDD = +5V, DVDD = +3.3V, AVSS = 0V, V_{REF} = +2.048V, and oscillator frequency = 4.096MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1246, ADS1247, ADS1248 MIN	TYP	MAX	UNIT
ANALOG INPUTS					
Full-scale input voltage (V_{IN} = ADCINP – ADCINN)			$\pm V_{REF}$/PGA		V
Common-mode input range		AVSS + 0.1V + $\frac{(V_{IN})(Gain)}{2}$		AVDD – 0.1V – $\frac{(V_{IN})(Gain)}{2}$	V
Differential input current			100		pA
PGA gain settings			1, 2, 4, 8, 16, 32, 64, 128		
Burnout current source			0.5, 2, or 10		µA
Bias voltage			(AVDD + AVSS)/2		V
Bias voltage output impedance			400		Ω
SYSTEM PERFORMANCE					
Resolution	No missing codes	24			Bits
Data rate			5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000		SPS
Integral nonlinearity (INL)	Differential input, end point fit, PGA = 1		6	15	ppm
Offset error	After calibration	–15		15	µV
Offset drift			See Figure 8 to Figure 11		nV/°C
Gain error	T = +25°C, all PGAs, data rate = 40, 80, or 160SPS	–0.02	±0.005	0.02	%
Gain drift			See Figure 12 to Figure 15		ppm/°C
ADC conversion time			Single-cycle settling		
Noise			See Table 5 to Table 8		
Normal-mode rejection			See Table 12		
Common-mode rejection	At dc, PGA = 1	80	90		dB
	At dc, PGA = 32	90	125		dB
Power-supply rejection	AVDD, DVDD at dc	100	135		dB
VOLTAGE REFERENCE INPUT					
Voltage reference input (V_{REF} = V_{REFP} – V_{REFN})		0.5		(AVDD – AVSS) – 1	V
Negative reference input (REFN)		AVSS – 0.1		REFP – 0.5	V
Positive reference input (REFP)		REFN + 0.5		AVDD + 0.1	V
Reference input current			30		nA
ON-CHIP VOLTAGE REFERENCE					
Output voltage		2.038	2.048	2.058	V
Output current(1)				±10	mA
Load regulation			50		µV/mA
Drift(2)	T_A = +25°C to +105°C		2	10	ppm/°C
	T_A = –40°C to +105°C		6	15	ppm/°C
Startup time			See Table 13		µs

(1) Do not exceed this loading on the internal voltage reference.
(2) Specified by the combination of design and final production test.

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ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications apply from –40°C to +105°C. Typical specifications are at +25°C. All specifications at AVDD = +5V, DVDD = +3.3V, AVSS = 0V, V_{REF} = +2.048V, and oscillator frequency = 4.096MHz, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1246, ADS1247, ADS1248 MIN	TYP	MAX	UNIT
CURRENT SOURCES (IDACS)						
Output current				50, 100, 250, 500, 750, 1000, 1500		µA
Voltage compliance		All currents		AVDD – 0.7		V
Initial error		All currents, each IDAC	–6	±1.0	6	% of FS
Initial mismatch		All currents, between IDACs		±0.03		% of FS
Temperature drift		Each IDAC		200		ppm/°C
Temperature drift matching		Between IDACs		10		ppm/°C
SYSTEM MONITORS						
Temperature sensor reading	Voltage	T_A = +25°C		118		mV
	Drift			405		µV/°C
GENERAL-PURPOSE INPUT/OUTPUT (GPIO)						
Logic levels	V_{IH}		0.7AVDD		AVDD	V
	V_{IL}		AVSS		0.3AVDD	V
	V_{OH}	I_{OH} = 1mA	0.8AVDD			V
	V_{OL}	I_{OL} = 1mA			0.2 AVDD	V
DIGITAL INPUT/OUTPUT (other than GPIO)						
Logic levels	V_{IH}		0.7DVDD		DVDD	V
	V_{IL}		DGND		0.3DVDD	V
	V_{OH}	I_{OH} = 1mA	0.8DVDD			V
	V_{OL}	I_{OL} = 1mA	DGND		0.2 DVDD	V
Input leakage		DGND < V_{IN} < DVDD			±10	µA
Clock input (CLK)	Frequency		1		4.5	MHz
	Duty cycle		25		75	%
Internal oscillator frequency			3.89	4.096	4.3	MHz
POWER SUPPLY						
DVDD			2.7		5.25	V
AVSS			–2.5		0	V
AVDD			AVSS + 2.7		AVSS + 5.25	V
DVDD current		Normal mode, DVDD = 5V, data rate = 20SPS, internal oscillator		230		µA
		Normal mode, DVDD = 3.3V, data rate = 20SPS, internal oscillator		210		µA
		Sleep mode		0.2		µA
AVDD current		Converting, AVDD = 5V, data rate = 20SPS, external reference		225		µA
		Converting, AVDD = 3.3V, data rate = 20SPS, external reference		212		µA
		Sleep mode		0.1		µA
		Additional current with internal reference enabled		180		µA
Power dissipation		AVDD = DVDD = 5V, data rate = 20SPS, internal oscillator, external reference		2.3		mW
		AVDD = DVDD = 3.3V, data rate = 20SPS, internal oscillator, external reference		1.4		mW
TEMPERATURE RANGE						
Specified			–40		+105	°C
Operating			–40		+125	°C
Storage			–60		+150	°C

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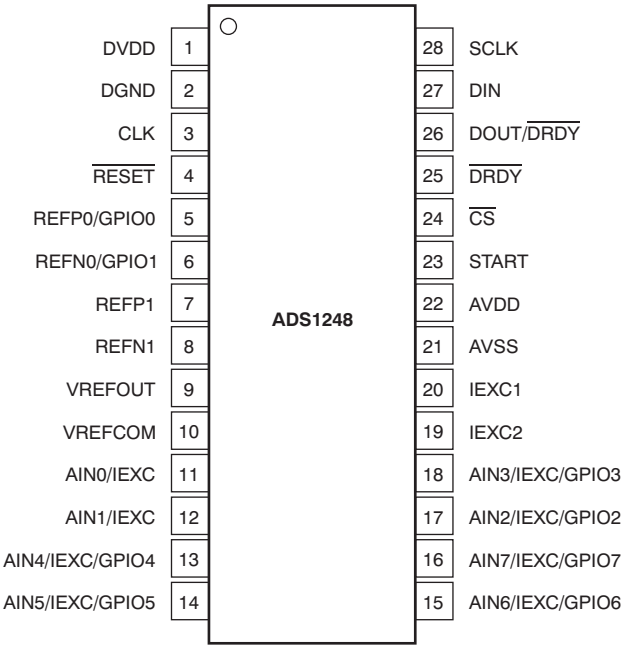
PIN CONFIGURATIONS

PW PACKAGE
TSSOP-28
(TOP VIEW)



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ADS1248 (TSSOP-28) PIN DESCRIPTIONS

NAME	PIN NO.	FUNCTION	DESCRIPTION
DVDD	1	Digital	Digital power supply
DGND	2	Digital	Digital ground
CLK	3	Digital input	External clock input. Tie this pin to DGND to activate the internal oscillator.
$\overline{\text{RESET}}$	4	Digital input	Chip reset (active low). Returns all register values to reset values.
REFP0/GPIO0	5	Analog input Digital in/out	Positive external reference input 0, or general-purpose digital input/output pin 0
REFN0/GPIO1	6	Analog input Digital in/out	Negative external reference 0 input, or general-purpose digital input/output pin 1
REFP1	7	Analog input	Positive external reference 1 input
REFN1	8	Analog input	Negative external reference 1 input
VREFOUT	9	Analog output	Positive internal reference voltage output
VREFCOM	10	Analog output	Negative internal reference voltage output. Connect this pin to AVSS when using a unipolar supply, or to the midvoltage of the power supply when using a bipolar supply.
AIN0/IEXC	11	Analog input	Analog input 0, optional excitation current output
AIN1/IEXC	12	Analog input	Analog input 1, optional excitation current output
AIN4/IEXC/GPIO4	13	Analog input Digital in/out	Analog input 4, optional excitation current output, or general-purpose digital input/output pin 4
AIN5/IEXC/GPIO5	14	Analog input Digital in/out	Analog input 5, optional excitation current output, or general-purpose digital input/output pin 5
AIN6/IEXC/GPIO6	15	Analog input Digital in/out	Analog input 6, optional excitation current output, or general-purpose digital input/output pin 6
AIN7/IEXC/GPIO7	16	Analog input Digital in/out	Analog input 7, optional excitation current output, or general-purpose digital input/output pin 7
AIN2/IEXC/GPIO2	17	Analog input Digital in/out	Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2
AIN3/IEXC/GPIO3	18	Analog input Digital in/out	Analog input 3, optional excitation current output, or general-purpose digital input/output pin 3
IOUT2	19	Analog output	Excitation current output 2
IOUT1	20	Analog output	Excitation current output 1
AVSS	21	Analog	Negative analog power supply
AVDD	22	Analog	Positive analog power supply
START	23	Digital input	Conversion start. See text for complete description.
$\overline{\text{CS}}$	24	Digital input	Chip select (active low)
$\overline{\text{DRDY}}$	25	Digital output	Data ready (active low)
DOUT/$\overline{\text{DRDY}}$	26	Digital output	Serial Data Out Output, or Data Out combined with Data Ready (active low when $\overline{\text{DRDY}}$ function enabled)
DIN	27	Digital input	Serial data input
SCLK	28	Digital input	Serial clock input

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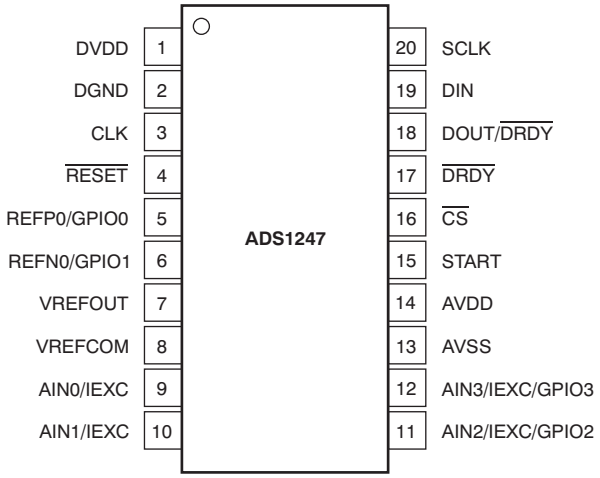
PW PACKAGE
TSSOP-20
(TOP VIEW)



ADS1247 (TSSOP-20) PIN DESCRIPTIONS

NAME	PIN NO.	FUNCTION	DESCRIPTION
DVDD	1	Digital	Digital power supply
DGND	2	Digital	Digital ground
CLK	3	Digital input	External clock input. Tie this pin to DGND to activate the internal oscillator.
$\overline{\text{RESET}}$	4	Digital input	Chip reset (active low). Returns all register values to reset values.
REFP0/GPIO0	5	Analog input Digital in/out	Positive external reference input, or general-purpose digital input/output pin 0
REFN0/GPIO1	6	Analog input Digital in/out	Negative external reference input, or general-purpose digital input/output pin 1
VREFOUT	7	Analog output	Positive internal reference voltage output
VREFCOM	8	Analog output	Negative internal reference voltage output. Connect this pin to AVSS when using a unipolar supply, or to the midvoltage of the power supply when using a bipolar supply.
AIN0/IEXC	9	Analog input	Analog input 0, optional excitation current output
AIN1/IEXC	10	Analog input	Analog input 1, optional excitation current output
AIN2/IEXC/GPIO2	11	Analog input Digital in/out	Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2
AIN3/IEXC/GPIO3	12	Analog input Digital in/out	Analog input 3, with or without excitation current output, or general-purpose digital input/output pin 3
AVSS	13	Analog	Negative analog power supply
AVDD	14	Analog	Positive analog power supply
START	15	Digital input	Conversion start. See text for description of use.
$\overline{\text{CS}}$	16	Digital input	Chip select (active low)
$\overline{\text{DRDY}}$	17	Digital output	Data ready (active low)
DOUT/$\overline{\text{DRDY}}$	18	Digital output	Serial data out output, or Data out combined with Data Ready (active low when $\overline{\text{DRDY}}$ function enabled)
DIN	19	Digital input	Serial data input
SCLK	20	Digital input	Serial clock input

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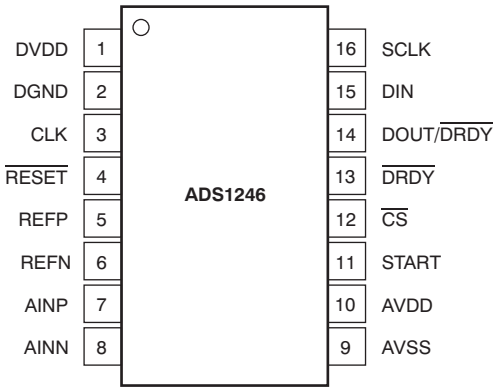
PW PACKAGE
TSSOP-16
(TOP VIEW)



ADS1246 (TSSOP-16) PIN DESCRIPTIONS

NAME	PIN NO.	FUNCTION	DESCRIPTION
DVDD	1	Digital	Digital power supply
DGND	2	Digital	Digital ground
CLK	3	Digital input	External clock input. Tie this pin to DGND to activate the internal oscillator.
$\overline{\text{RESET}}$	4	Digital input	Chip reset (active low). Returns all register values to reset values.
REFP	5	Analog input	Positive external reference input
REFN	6	Analog input	Negative external reference input
AINP	7	Analog input	Positive analog input
AINN	8	Analog input	Negative analog input
AVSS	9	Analog	Negative analog power supply
AVDD	10	Analog	Positive analog power supply
START	11	Digital input	Conversion start. See text for description of use.
$\overline{\text{CS}}$	12	Digital input	Chip select (active low)
$\overline{\text{DRDY}}$	13	Digital output	Data ready (active low)
DOUT/$\overline{\text{DRDY}}$	14	Digital output	Serial data out output, or Data out combined with Data Ready (active low when $\overline{\text{DRDY}}$ function enabled)
DIN	15	Digital input	Serial data input
SCLK	16	Digital input	Serial clock input

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TIMING DIAGRAMS

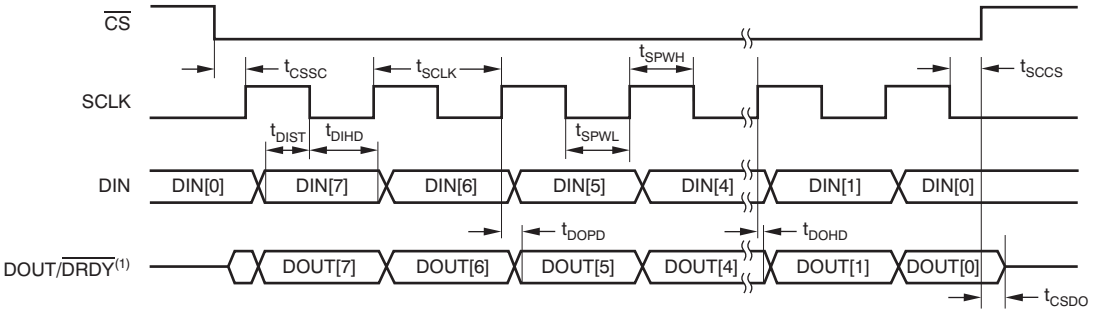

Figure 1. Serial Interface Timing

Table 1. Timing Characteristics for Figure 1(1)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to first SCLK high (set up time)	10		ns
t_{SCCS}	SCLK low to CS high (hold time)	7		t_{OSC}(2)
t_{DIST}	DIN set up time	5		ns
t_{DIHD}	DIN hold time	5		ns
t_{DOPD}	SCLK rising edge to new data valid		30	ns
t_{DOHD}	DOUT hold time	0		ns
t_{SCLK}	SCLK period	500		ns
			64	Conversions
t_{SPWH}	SCLK pulse width high	0.25	0.75	t_{SCLK}
t_{SPWL}	SCLK pulse width low	0.25	0.75	t_{SCLK}
t_{CSDO}	$\overline{CS}$ high to DOUT high impedance		10	ns

(1) DRDY MODE bit = 0.
(2) $t_{OSC} = 1/f_{CLK}$. The default clock frequency f_{CLK} = 4.096MHz.

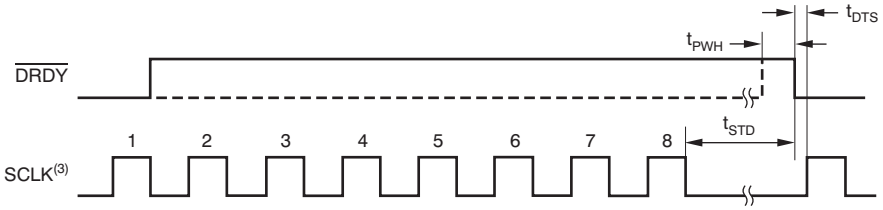

Figure 2. SPI Interface Timing to Allow Conversion Result Loading(3)(4)

Table 2. Timing Characteristics for Figure 2

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{PWH}	$\overline{DRDY}$ pulse width high	3		t_{OSC}
t_{STD}	SCLK low prior to $\overline{DRDY}$ low	5		t_{OSC}
t_{DTS}	$\overline{DRDY}$ falling edge to SCLK rising edge	30		ns

(3) This timing diagram is applicable only when the $\overline{CS}$ pin is low. SCLK need not be low during t_{STD} when $\overline{CS}$ is high.
(4) SCLK should only be sent in multiples of eight during partial retrieval of output data.

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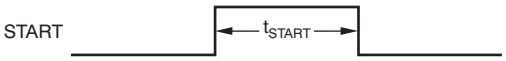

Figure 3. Minimum START Pulse Width

Table 3. Timing Characteristics for Figure 3

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{START}	START pulse width high	3		t_{OSC}

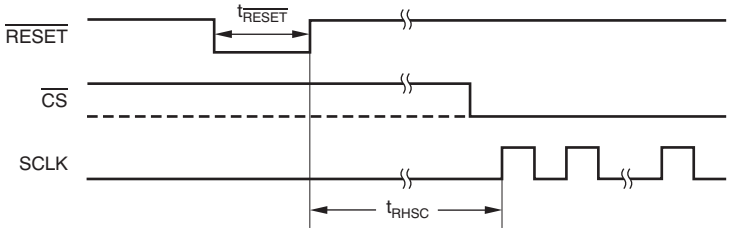

Figure 4. Reset Pulse Width and SPI Communication After Reset

Table 4. Timing Characteristics for Figure 4

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
$t_{\overline{RESET}}$	$\overline{RESET}$ pulse width low	4		t_{OSC}
t_{RHSC}	$\overline{RESET}$ high to SPI communication start	0.6(1)		ms

(1) Applicable only when f_{OSC} = 4.096MHz and scales proportionately with f_{OSC} frequency.

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NOISE PERFORMANCE

The ADS1246/7/8 noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, particularly useful when measuring low-level signals. Table 5 to Table 10 summarize noise performance of the ADS1246/7/8. The data are representative of typical noise performance at T = +25°C. The data shown are the result of averaging the readings from multiple devices and were measured with the inputs shorted together. A minimum of 128 consecutive readings were used to calculate the RMS and peak-to-peak noise for each reading.

Table 5, Table 7, and Table 9 list the input-referred noise in units of μV_{RMS} on μV_{PP} for the conditions shown. Table 6, Table 8, and Table 10 list the corresponding data in units of ENOB (effective number of bits) where:

ENOB = ln(Full-Scale Range/Noise)/ln(2)

Table 7 to Table 10 use the internal reference available on the ADS1247 and ADS1248. The data though are also representative of the ADS1246 noise performance when using a low-noise external reference such as the REF5020.

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Table 5. Noise in μV_{RMS} and (μV_{PP}) at AVDD = 5V, AVSS = 0V, and External Reference = 2.5V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	1.10 (4.99)	0.68 (3.80)	0.37 (1.90)	0.19 (0.98)	0.10 (0.44)	0.07 (0.31)	0.05 (0.27)	0.05 (0.21)
10	1.53 (8.82)	0.82 (3.71)	0.50 (2.69)	0.27 (1.33)	0.15 (0.67)	0.08 (0.50)	0.06 (0.36)	0.07 (0.34)
20	2.32 (13.37)	1.23 (6.69)	0.71 (3.83)	0.34 (1.90)	0.18 (1.01)	0.12 (0.71)	0.10 (0.51)	0.09 (0.54)
40	2.72 (17.35)	1.33 (7.65)	0.68 (3.83)	0.38 (2.21)	0.22 (1.13)	0.14 (0.77)	0.15 (0.78)	0.14 (0.76)
80	3.56 (22.67)	1.87 (12.30)	0.81 (5.27)	0.50 (3.49)	0.30 (1.99)	0.19 (1.24)	0.19 (1.16)	0.18 (1.04)
160	5.26 (42.03)	2.52 (17.57)	1.32 (9.22)	0.67 (5.25)	0.41 (2.89)	0.26 (1.91)	0.27 (1.74)	0.26 (1.74)
320	9.39 (74.91)	4.68 (39.48)	2.69 (18.95)	1.24 (9.94)	0.68 (5.25)	0.45 (3.08)	0.38 (2.71)	0.36 (2.46)
640	13.21 (119.66)	6.93 (59.31)	3.59 (28.55)	1.53 (10.68)	0.95 (8.70)	0.63 (4.94)	0.53 (3.74)	0.50 (3.55)
1000	32.34 (443.91)	16.11 (185.67)	11.54 (92.23)	4.65 (37.55)	2.02 (23.14)	1.15 (12.29)	0.77 (7.42)	0.64 (4.98)
2000	32.29 (372.54)	15.99 (182.27)	8.02 (91.73)	4.08 (45.89)	2.19 (24.14)	1.36 (12.32)	1.08 (8.03)	1.00 (6.93)

Table 6. Effective Number of Bits From RMS Noise and (Peak-to-Peak Noise) at AVDD = 5V, AVSS = 5V, and External Reference = 2.5V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	21.8 (19.6)	21.5 (19.0)	21.4 (19.0)	21.4 (19.0)	21.3 (19.2)	20.9 (18.7)	20.2 (17.8)	19.4 (17.2)
10	21.4 (18.8)	21.3 (19.1)	21.0 (18.5)	20.8 (18.6)	20.7 (18.6)	20.6 (18.0)	19.9 (17.5)	18.9 (16.5)
20	20.8 (18.2)	20.7 (18.2)	20.5 (18.0)	20.5 (18.0)	20.4 (18.0)	20.0 (17.5)	19.3 (16.9)	18.4 (15.9)
40	20.5 (17.8)	20.6 (18.0)	20.5 (18.0)	20.4 (17.8)	20.2 (17.8)	19.8 (17.4)	18.7 (16.3)	17.8 (15.4)
80	20.1 (17.5)	20.1 (17.3)	20.3 (17.6)	20.0 (17.2)	19.7 (17.0)	19.4 (16.7)	18.4 (15.7)	17.5 (14.9)
160	19.6 (16.6)	19.6 (16.8)	19.6 (16.8)	19.5 (16.6)	19.3 (16.4)	18.9 (16.0)	17.9 (15.2)	16.9 (14.2)
320	18.7 (15.7)	18.7 (15.7)	18.5 (15.7)	18.7 (15.7)	18.5 (15.6)	18.1 (15.3)	17.4 (14.5)	16.5 (13.7)
640	18.2 (15.1)	18.2 (15.1)	18.1 (15.1)	18.4 (15.5)	18.0 (14.8)	17.6 (14.7)	16.9 (14.1)	16.0 (13.1)
1000	17.0 (13.2)	17.0 (13.4)	16.4 (13.4)	16.7 (13.7)	17.0 (13.4)	16.8 (13.3)	16.4 (13.1)	15.6 (12.6)
2000	17.0 (13.4)	17.0 (13.5)	17.0 (13.4)	16.9 (13.4)	16.8 (13.4)	16.5 (13.3)	15.9 (13.0)	15.0 (12.2)

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Table 7. Noise in μV_{RMS} and (μV_{PP}) at AVDD = 5V, AVSS = 0V, and External Reference = 2.5V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	1.35 (7.78)	0.70 (4.17)	0.35 (2.03)	0.17 (0.95)	0.10 (0.53)	0.06 (0.32)	0.05 (0.31)	0.05 (0.29)
10	1.80 (10.82)	0.88 (5.26)	0.50 (2.75)	0.24 (1.47)	0.13 (0.80)	0.09 (0.49)	0.07 (0.39)	0.07 (0.40)
20	2.62 (14.32)	1.22 (7.05)	0.66 (3.88)	0.35 (2.05)	0.19 (1.09)	0.12 (0.66)	0.10 (0.61)	0.10 (0.55)
40	2.64 (16.29)	1.34 (7.75)	0.69 (4.06)	0.35 (2.07)	0.21 (1.15)	0.15 (0.85)	0.14 (0.81)	0.13 (0.75)
80	3.69 (23.62)	1.82 (10.81)	0.89 (5.48)	0.51 (2.68)	0.30 (1.69)	0.21 (1.32)	0.20 (1.09)	0.18 (0.98)
160	5.70 (35.74)	2.63 (16.90)	1.34 (8.82)	0.68 (4.24)	0.40 (2.65)	0.30 (1.92)	0.28 (1.88)	0.26 (1.57)
320	9.67 (67.44)	4.95 (35.30)	2.59 (17.52)	1.29 (8.86)	0.72 (4.35)	0.49 (3.03)	0.40 (2.44)	0.37 (2.34)
640	13.66 (93.06)	7.04 (45.20)	3.63 (18.73)	1.84 (12.97)	1.02 (6.51)	0.68 (4.20)	0.58 (3.69)	0.53 (3.50)
1000	31.18 (284.59)	16.00 (129.77)	7.58 (61.30)	3.98 (33.04)	2.08 (16.82)	1.16 (9.08)	0.83 (5.42)	0.68 (4.65)
2000	31.42 (273.39)	15.45 (130.68)	8.07 (67.13)	4.06 (36.16)	2.29 (19.22)	1.38 (9.87)	1.06 (6.93)	1.00 (6.48)

Table 8. Effective Number of Bits From RMS Noise and (Peak-to-Peak Noise) at AVDD = 5V, AVSS = 0V, and Internal Reference = 2.048V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	21.5 (19.0)	21.5 (18.9)	21.5 (18.9)	21.5 (19.0)	21.3 (18.9)	21.0 (18.6)	20.2 (17.7)	19.2 (16.8)
10	21.1 (18.5)	21.1 (18.6)	21.0 (18.5)	21.0 (18.4)	20.9 (18.3)	20.5 (18.0)	19.8 (17.3)	18.7 (16.3)
20	20.6 (18.1)	20.7 (18.1)	20.6 (18.0)	20.5 (17.9)	20.4 (17.8)	20.1 (17.6)	19.2 (16.7)	18.3 (15.8)
40	20.6 (17.9)	20.5 (18.0)	20.5 (17.9)	20.5 (17.9)	20.2 (17.8)	19.7 (17.2)	18.8 (16.3)	17.9 (15.4)
80	20.1 (17.4)	20.1 (17.5)	20.1 (17.5)	20.0 (17.5)	19.7 (17.2)	19.2 (16.6)	18.3 (15.8)	17.5 (15.0)
160	19.5 (16.8)	19.6 (16.9)	19.5 (16.8)	19.5 (16.9)	19.3 (16.6)	18.7 (16.0)	17.8 (15.1)	16.9 (14.3)
320	18.7 (15.9)	18.7 (15.8)	18.6 (15.8)	18.6 (15.8)	18.4 (15.8)	18.0 (15.4)	17.3 (14.7)	16.4 (13.7)
640	18.2 (15.4)	18.1 (15.5)	18.1 (15.7)	18.1 (15.3)	17.9 (15.3)	17.5 (14.9)	16.8 (14.1)	15.9 (13.2)
1000	17.0 (13.8)	17.0 (13.9)	17.0 (14.0)	17.0 (13.9)	16.9 (13.9)	16.8 (13.8)	16.2 (13.5)	15.5 (12.7)
2000	17.0 (13.9)	17.0 (13.9)	17.0 (13.9)	16.9 (13.8)	16.8 (13.7)	16.5 (13.7)	15.9 (13.2)	15.0 (12.3)

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Table 9. Noise in μV_{RMS} and (μV_{PP}) at AVDD = 3V, AVSS = 0V, and External Reference = 2.048V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	2.50 (14.24)	1.32 (6.92)	0.67 (3.48)	0.32 (1.68)	0.17 (0.90)	0.09 (0.51)	0.08 (0.42)	0.07 (0.39)
10	3.09 (16.85)	1.69 (9.32)	0.82 (4.68)	0.42 (2.41)	0.23 (1.18)	0.11 (0.63)	0.11 (0.66)	0.10 (0.55)
20	4.55 (24.74)	2.19 (12.82)	1.07 (5.94)	0.55 (3.38)	0.28 (1.66)	0.16 (1.00)	0.15 (0.92)	0.14 (0.87)
40	5.06 (34.59)	2.39 (14.49)	1.27 (7.75)	0.66 (4.01)	0.36 (2.18)	0.21 (1.16)	0.21 (1.27)	0.15 (0.84)
80	6.63 (43.46)	3.28 (20.22)	1.79 (10.64)	0.89 (5.48)	0.47 (2.95)	0.29 (1.63)	0.28 (1.64)	0.21 (1.24)
160	9.75 (68.28)	4.89 (32.19)	2.36 (17.74)	1.26 (9.87)	0.65 (4.77)	0.40 (2.60)	0.40 (2.70)	0.30 (2.12)
320	19.22 (140.06)	9.80 (82.24)	4.81 (32.74)	2.47 (18.59)	1.27 (9.45)	0.71 (5.83)	0.50 (3.36)	0.43 (2.86)
640	27.07 (192.96)	13.54 (100.26)	6.88 (49.07)	3.40 (25.93)	1.76 (12.49)	1.02 (7.49)	0.71 (4.81)	0.60 (4.06)
1000	40.83 (388.28)	20.39 (185.96)	10.39 (89.38)	5.09 (43.28)	2.66 (22.78)	1.45 (11.01)	0.93 (6.74)	0.74 (4.86)
2000	42.06 (322.85)	21.15 (166.75)	10.66 (92.68)	5.61 (44.08)	2.92 (23.06)	1.68 (11.71)	1.19 (8.23)	1.05 (6.97)

Table 10. Effective Number of Bits From RMS and (Peak-to-Peak Noise) at AVDD = 3V, AVSS = 0V, and Internal Reference = 2.048V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	20.6 (18.1)	20.6 (18.2)	20.5 (18.2)	20.6 (18.2)	20.5 (18.1)	20.4 (17.9)	19.6 (17.2)	18.8 (16.3)
10	20.3 (17.9)	20.2 (17.7)	20.3 (17.7)	20.2 (17.7)	20.1 (17.7)	20.1 (17.6)	19.1 (16.6)	18.3 (15.8)
20	19.8 (17.3)	19.8 (17.3)	19.9 (17.4)	19.8 (17.2)	19.8 (17.2)	19.6 (17.0)	18.7 (16.1)	17.8 (15.2)
40	19.6 (16.9)	19.7 (17.1)	19.6 (17.0)	19.6 (17.0)	19.5 (16.8)	19.2 (16.8)	18.2 (15.6)	17.7 (15.2)
80	19.2 (16.5)	19.3 (16.6)	19.1 (16.6)	19.1 (16.5)	19.0 (16.4)	18.7 (16.3)	17.8 (15.3)	17.2 (14.7)
160	18.7 (15.9)	18.7 (16.0)	18.7 (15.8)	18.6 (15.7)	18.6 (15.7)	18.3 (15.6)	17.3 (14.5)	16.7 (13.9)
320	17.7 (14.8)	17.7 (14.6)	17.7 (14.9)	17.7 (14.7)	17.6 (14.7)	17.5 (14.4)	17.0 (14.2)	16.2 (13.4)
640	17.2 (14.4)	17.2 (14.3)	17.2 (14.3)	17.2 (14.3)	17.1 (14.3)	16.9 (14.1)	16.5 (13.7)	15.7 (12.9)
1000	16.6 (13.4)	16.6 (13.4)	16.6 (13.5)	16.6 (13.5)	16.6 (13.5)	16.4 (13.5)	16.1 (13.2)	15.4 (12.7)
2000	16.6 (13.6)	16.6 (13.6)	16.6 (13.4)	16.5 (13.5)	16.4 (13.4)	16.2 (13.4)	15.7 (12.9)	14.9 (12.2)

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TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = 5V, V_{REF} = 2.5V, and AVSS = 0V, unless otherwise noted.

NOISE HISTOGRAM PLOT

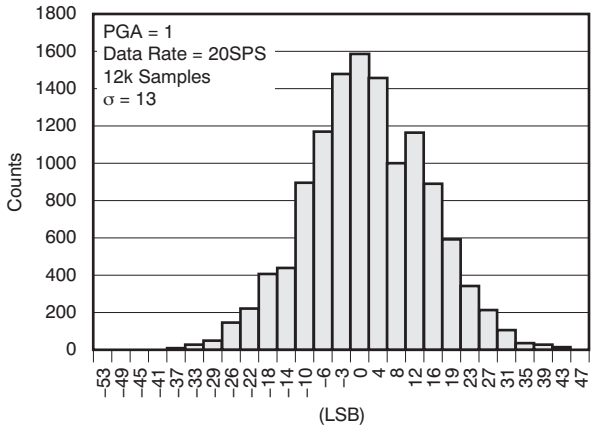

Figure 5.

NOISE HISTOGRAM PLOT

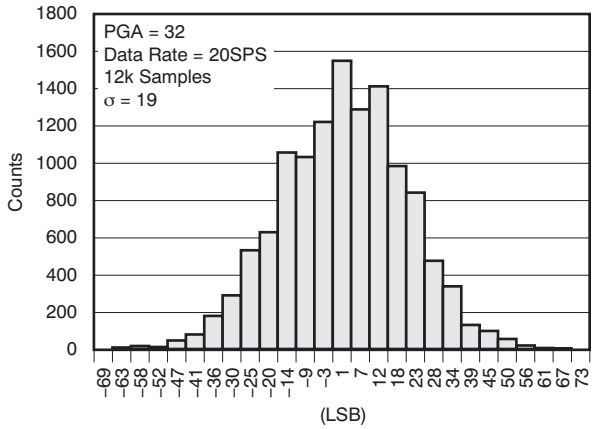

Figure 6.

RMS NOISE vs INPUT SIGNAL

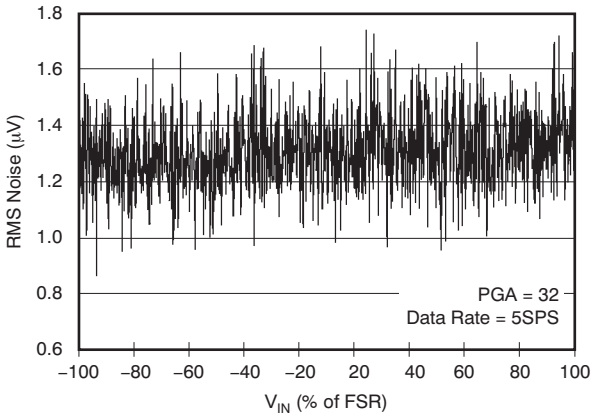

Figure 7.

OFFSET vs TEMPERATURE

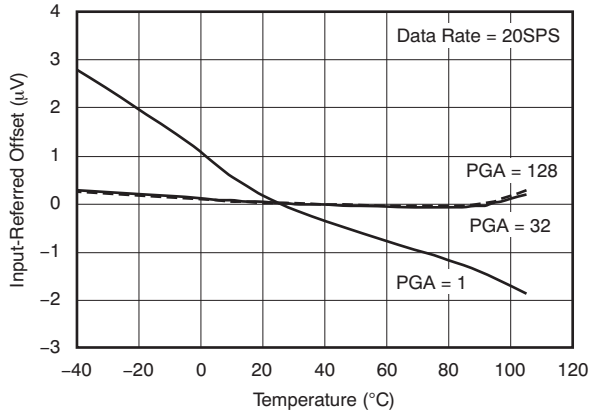

Figure 8.

OFFSET vs TEMPERATURE

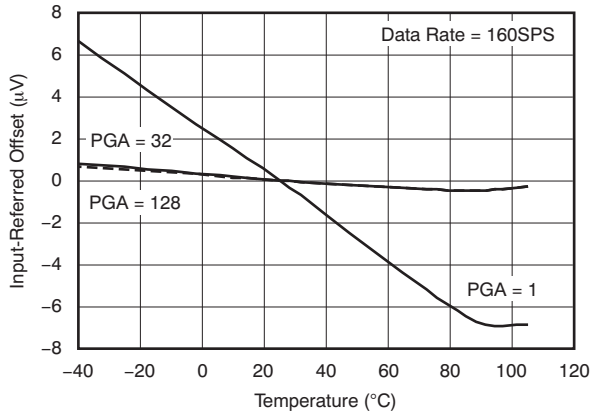

Figure 9.

OFFSET vs TEMPERATURE

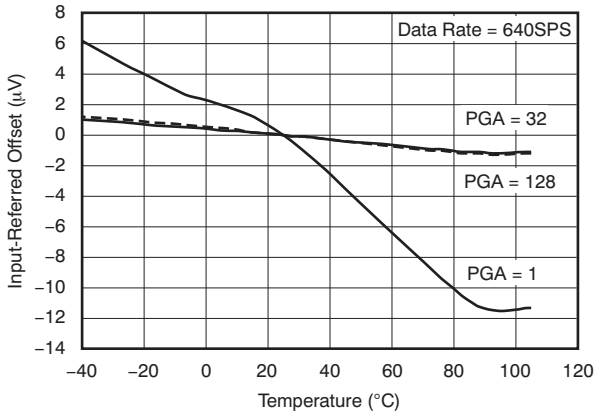

Figure 10.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 5V, V_{REF} = 2.5V, and AVSS = 0V, unless otherwise noted.

OFFSET vs TEMPERATURE

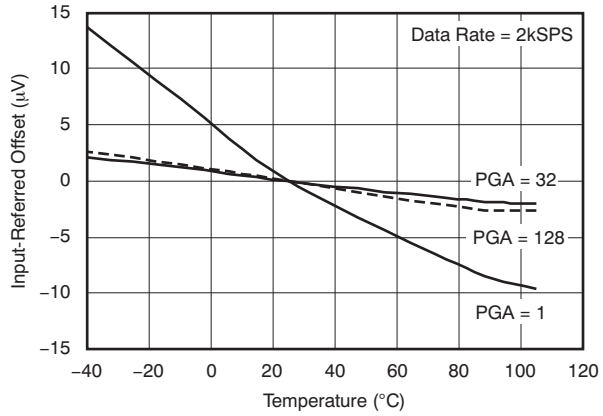

Figure 11.

GAIN vs TEMPERATURE

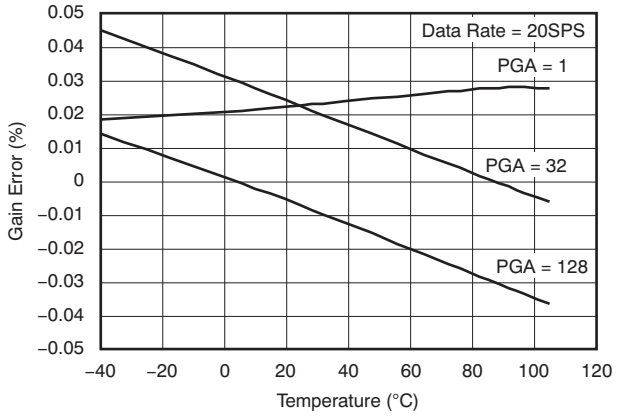

Figure 12.

GAIN vs TEMPERATURE

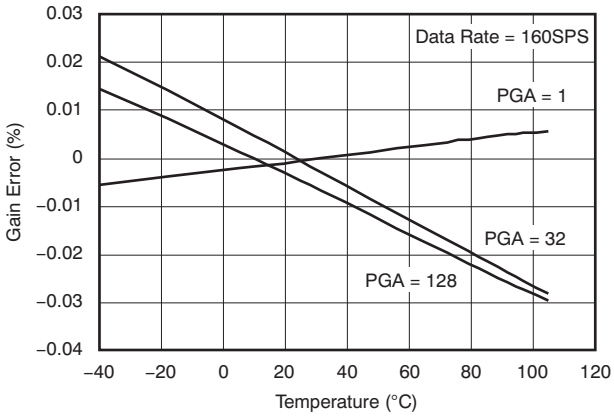

Figure 13.

GAIN vs TEMPERATURE

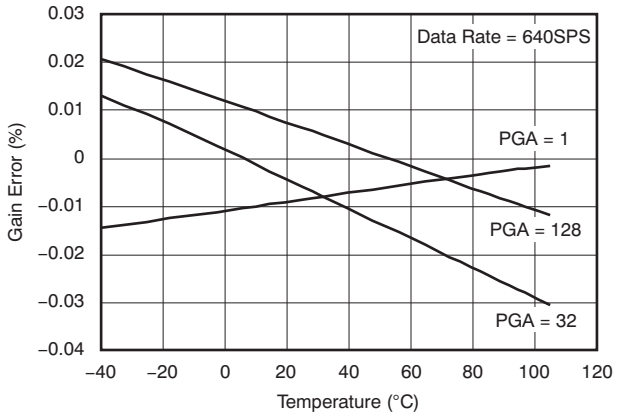

Figure 14.

GAIN vs TEMPERATURE

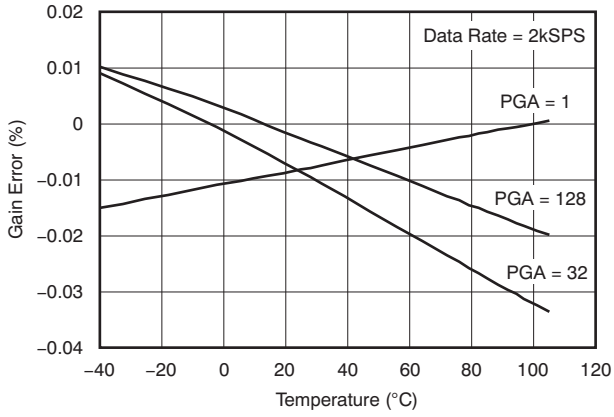

Figure 15.

ANALOG CURRENT vs DATA RATE

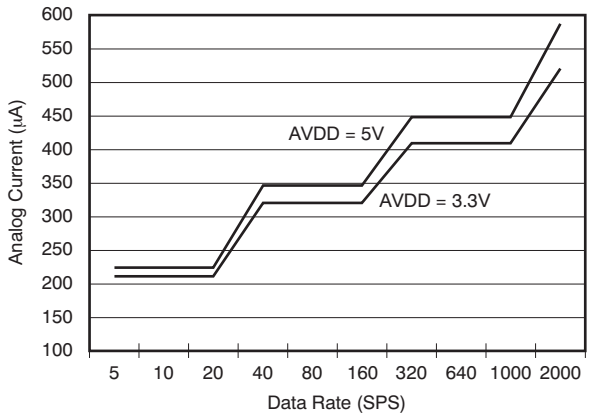

Figure 16.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 5V, V_{REF} = 2.5V, and AVSS = 0V, unless otherwise noted.

DIGITAL CURRENT vs DATA RATE

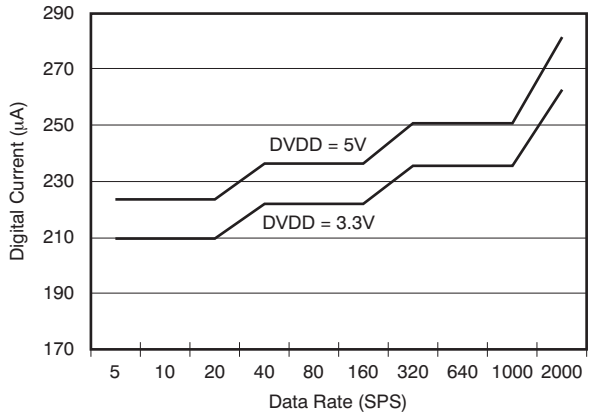

Figure 17.

ANALOG CURRENT vs TEMPERATURE

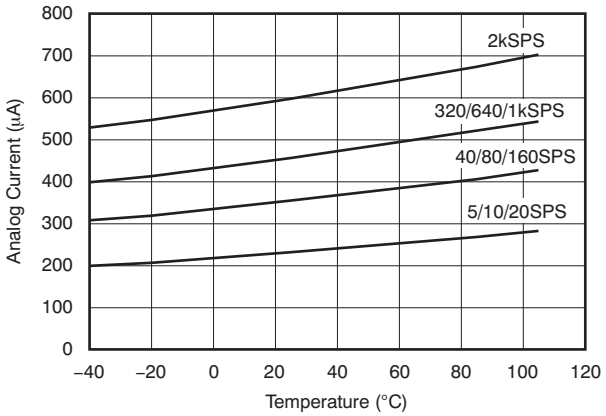

Figure 18.

DIGITAL CURRENT vs TEMPERATURE

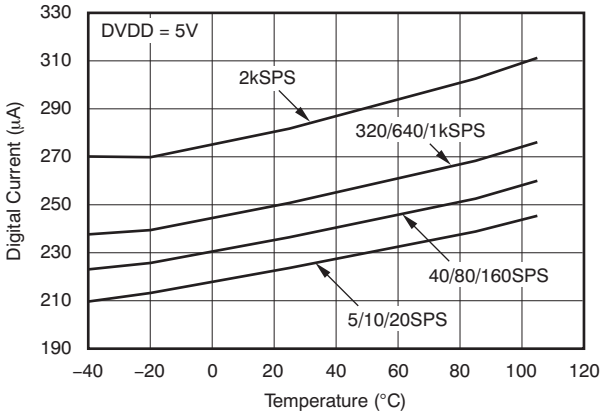

Figure 19.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

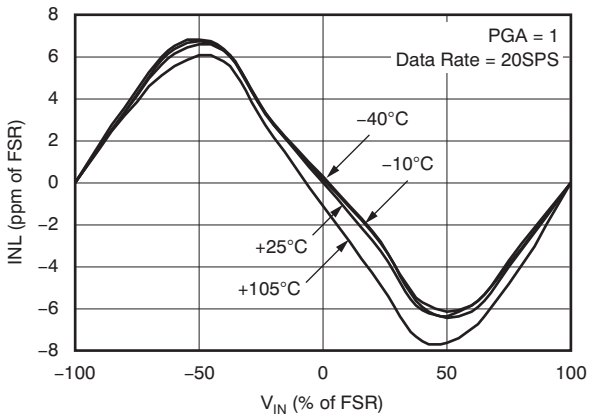

Figure 20.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

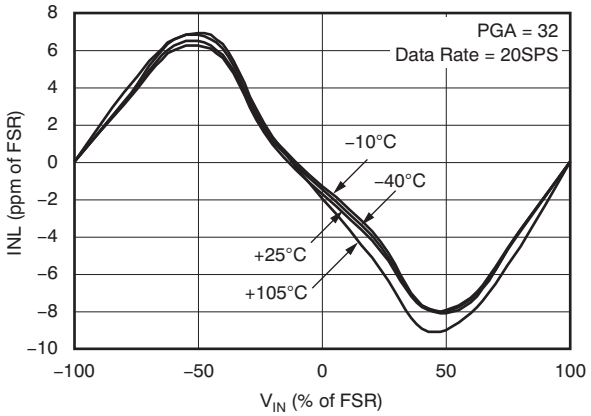

Figure 21.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

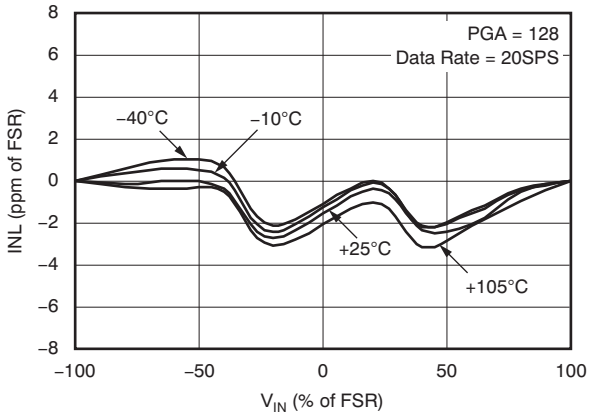

Figure 22.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 5V, V_{REF} = 2.5V, and AVSS = 0V, unless otherwise noted.

INTEGRAL NONLINEARITY vs INPUT SIGNAL

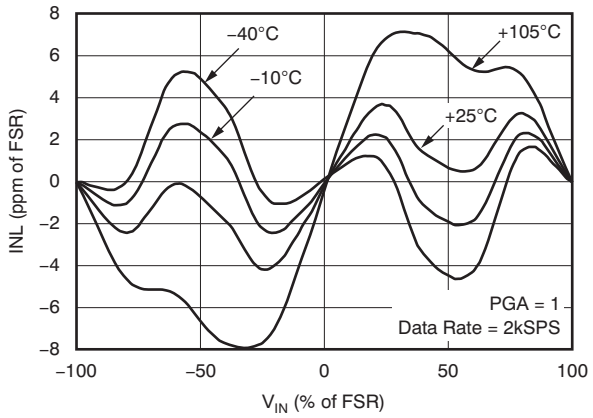

Figure 23.

DATA RATE ERROR vs TEMPERATURE (Using Internal Oscillator)

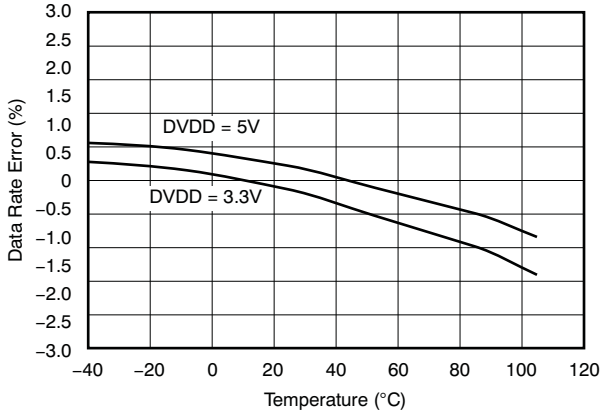

Figure 24.

CMRR vs TEMPERATURE

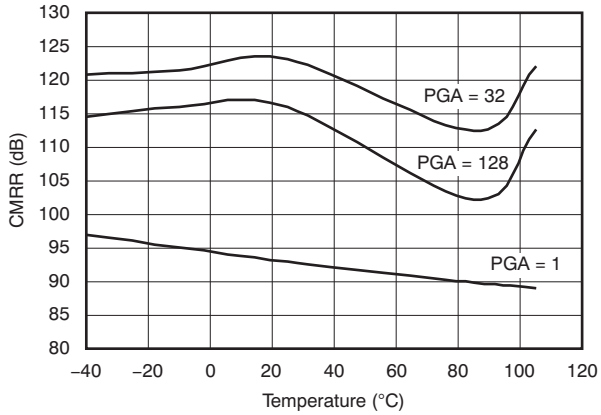

Figure 25.

INTERNAL V_{REF} vs TEMPERATURE

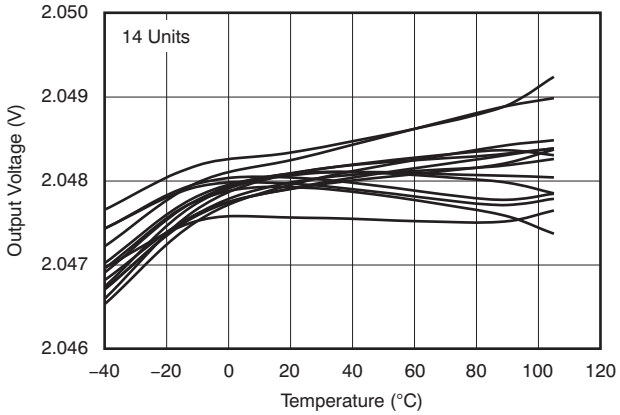

Figure 26.

IDAC LINE REGULATION

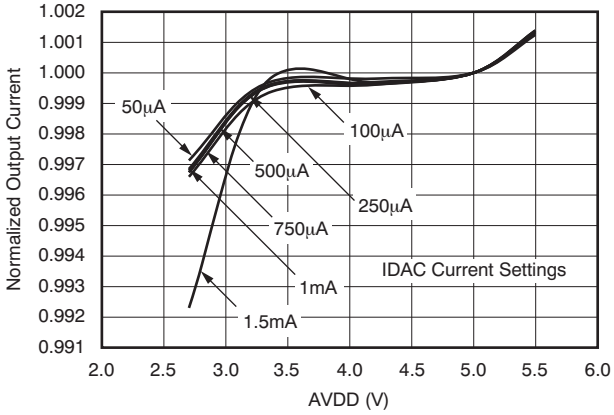

Figure 27.

IDAC DRIFT

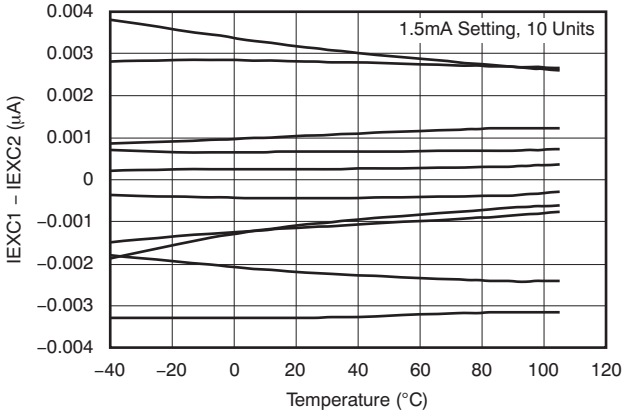

Figure 28.

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GENERAL DESCRIPTION

OVERVIEW

The ADS1246, ADS1247 and ADS1248 are highly integrated 24-bit data converters. They include a low-noise, high-impedance programmable gain amplifier (PGA), a delta-sigma (ΔΣ) ADC with an adjustable single-cycle settling digital filter, internal oscillator, and a simple but flexible SPI-compatible serial interface.

The ADS1247 and ADS1248 also include a flexible input multiplexer with system monitoring capability and general-purpose I/O settings, a very low-drift voltage reference, and two matched current sources for sensor excitation. Figure 29 and Figure 30 show the various functions incorporated in each device.

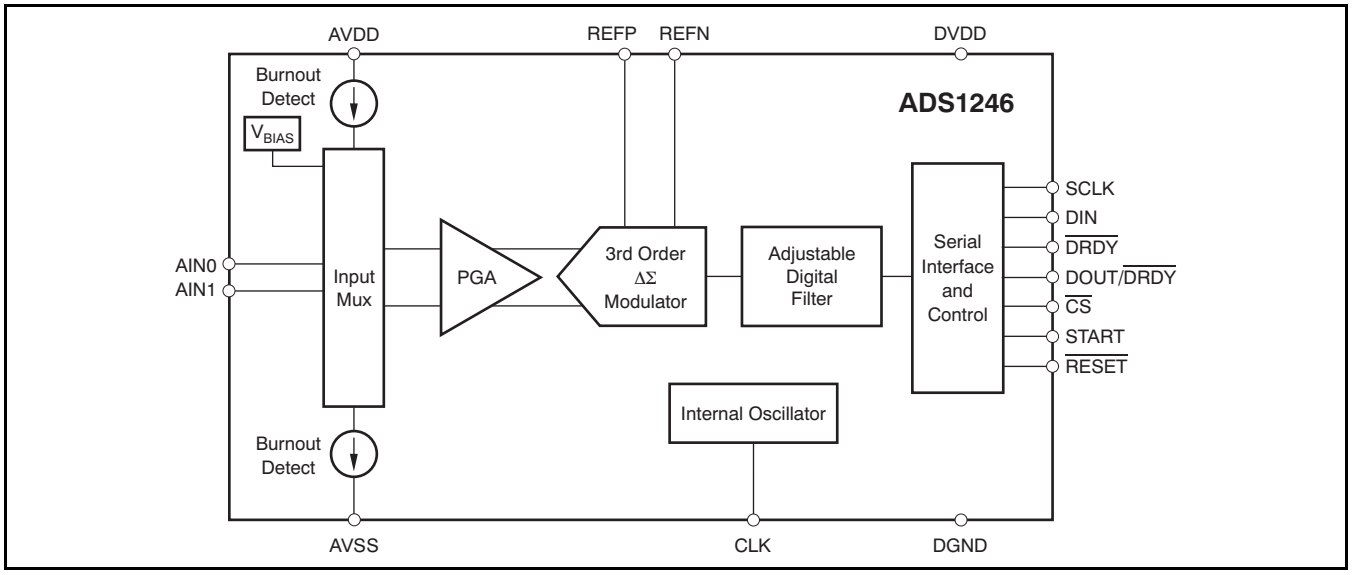

Figure 29. ADS1246 Diagram

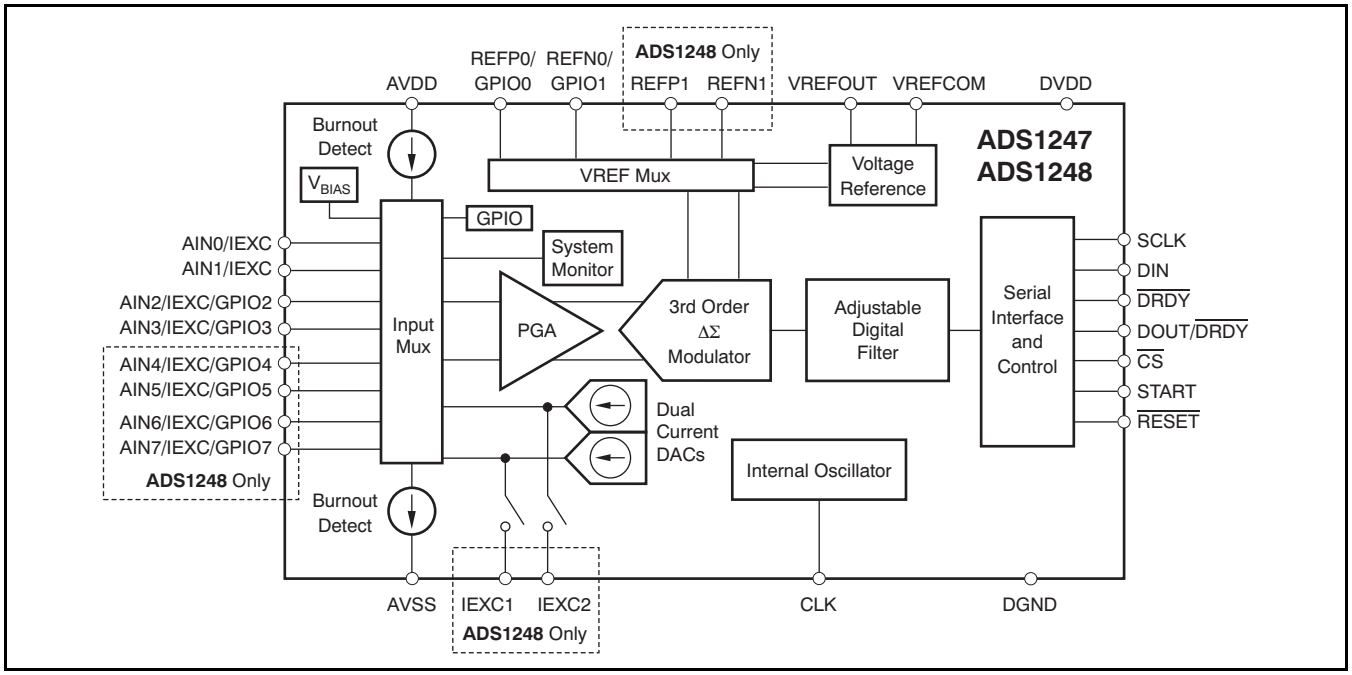

Figure 30. ADS1247, ADS1248 Diagram

ADC INPUT AND MULTIPLEXER

The ADS1246/7/8 ADC measures the input signal through the onboard PGA. All analog inputs are connected to the internal AIN_P or AIN_N analog inputs through the analog multiplexer. A block diagram of the analog input multiplexer is shown in Figure 31.

The input multiplexer connects to eight (ADS1248), four (ADS1247), or two (ADS1246) analog inputs that can be configured as single-ended inputs, differential inputs, or in a combination of single-ended and differential inputs. The multiplexer also allows the on-chip excitation current and/or bias voltage to be selected to a specific channel.

Any analog input pin can be selected as the positive input or negative input through the MUX0 register. The ADS1246/7/8 have a true fully differential mode, meaning that the input signal range can be from –2.5V to +2.5V (when AVDD = 2.5V and AVSS = –2.5V).

Through the input multiplexer, the ambient temperature (internal temperature sensor), AVDD, DVDD, and external reference can all be selected for measurement. Refer to the *System Monitor* section for details.

On the ADS1247 and ADS1248, the analog inputs can also be configured as general-purpose inputs/outputs (GPIOs). See the *General-Purpose Digital I/O* section for more details.

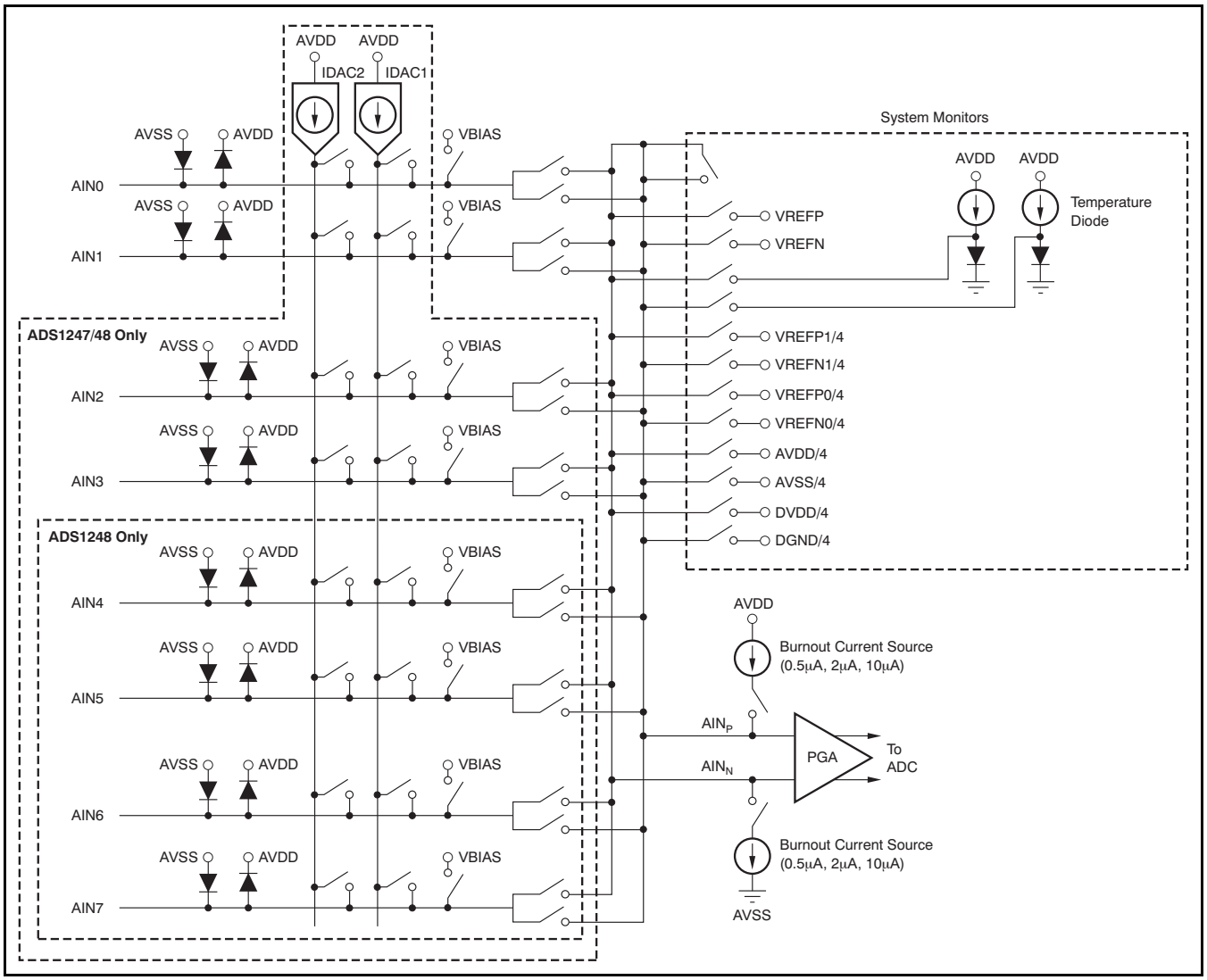

Figure 31. Analog Input Multiplexer Circuit

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ESD diodes protect the ADC inputs. To prevent these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100mV, and do not exceed AVDD by more than 100mV, as shown in Equation 2. Note that the same caution is true if the inputs are configured to be GPIOs.

$$AVSS - 100mV < (AINX) < AVDD + 100mV \quad (2)$$

Settling Time for Channel Multiplexing

The ADS1246/7/8 is a true single-cycle settling ΔΣ converter. The first data available after the start of a conversion are fully settled and valid for use. The time required to settle is roughly equal to the inverse of the data rate. The exact time depends on the specific data rate and the operation that resulted in the start of a conversion; see Table 19 for specific values.

VOLTAGE REFERENCE INPUT

The voltage reference for the ADS1246/7/8 is the differential voltage between REFP and REFN:

$$V_{REF} = V_{REFP} - V_{REFN}$$

In the case of the ADS1246, these pins are dedicated inputs. For the ADS1247 and ADS1248, there is a multiplexer that selects the reference inputs, as shown in Figure 32. The reference input uses a buffer to increase the input impedance.

As with the analog inputs, REFP0 and REFN0 can be configured as digital I/Os on the ADS1247/48.

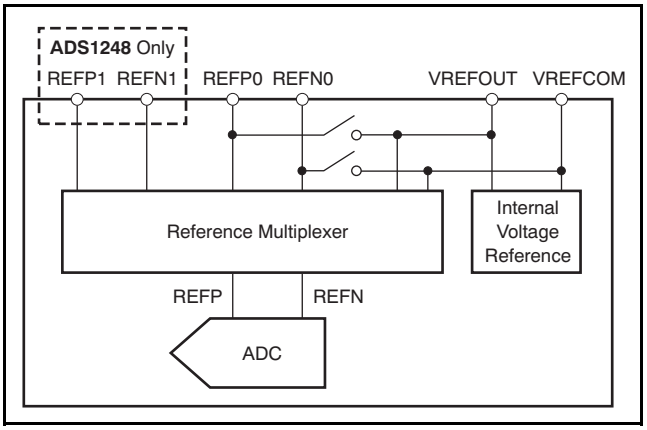

Figure 32. Reference Input Multiplexer

The reference input circuit has ESD diodes to protect the inputs. To prevent the diodes from turning on, make sure the voltage on the reference input pin is not less than AVSS – 100mV, and does not exceed AVDD + 100mV, as shown in Equation 3:

$$AVSS - 100mV < (V_{REFP} \text{ or } V_{REFN}) < AVDD + 100mV \quad (3)$$

LOW-NOISE PGA

The ADS1246/7/8 feature a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA can be set to gain of 1, 2, 4, 8, 16, 32, 64, or 128 by register SYS0. A simplified diagram of the PGA is shown in Figure 33.

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in Figure 33. Note that as with any PGA, it is necessary to ensure that the input voltage stays within the specified common-mode input range specified in the Electrical Characteristics. The common-mode input (V_{CMI}) must be within the range shown in Equation 4:

$$\left(AVSS + 0.1V + \frac{(V_{IN})(Gain)}{2}\right) \le V_{CMI} \le \left(AVDD - 0.1V - \frac{(V_{IN})(Gain)}{2}\right) \quad (4)$$

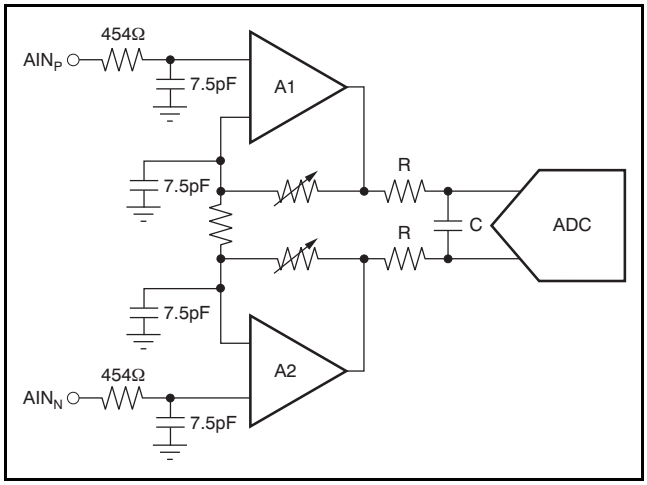

Figure 33. Simplified Diagram of the PGA

MODULATOR

A third-order modulator is used in the ADS1246/7/8. The modulator converts the analog input voltage into a pulse code modulated (PCM) data stream. To save power, the modulator clock runs from 32kHz up to 512kHz for different data rates, as shown in Table 11.

Table 11. Modulator Clock Frequency for Different Data Rates

DATA RATE (SPS)	f_{MOD} (kHz)
5, 10, 20	32
40, 80, 160	128
320, 640, 1000	256
2000	512

DIGITAL FILTER

The ADS1246/7/8 use linear-phase finite impulse response (FIR) digital filters that can be adjusted for different output data rates. The digital filter always settles in a single cycle.

Table 12 shows the exact data rates when an external oscillator equal to 4.096MHz is used. Also shown is the signal –3dB bandwidth, and the 50Hz and 60Hz attenuation. For good 50Hz or 60Hz rejection, use a data rate of 20SPS or slower.

The frequency responses of the digital filter are shown in Figure 34 to Figure 44. Figure 37 shows a detailed view of the filter frequency response from 48Hz to 62Hz for a 20SPS data rate. All filter plots are generated with 4.096MHz external clock.

Table 12. Digital Filter Specifications(1)

NOMINAL DATA RATE	ACTUAL DATA RATE	–3dB BANDWIDTH	ATTENUATION			
			f_{IN} = 50Hz ±0.3Hz	f_{IN} = 60Hz ±0.3Hz	f_{IN} = 50Hz ±1Hz	f_{IN} = 60Hz ±1Hz
5SPS	5.018SPS	2.26Hz	–106dB	–74dB	–81dB	–69dB
10SPS	10.037SPS	4.76Hz	–106dB	–74dB	–80dB	–69dB
20SPS	20.075SPS	14.8Hz	–71dB	–74dB	–66dB	–68dB
40SPS	40.15SPS	9.03Hz				
80SPS	80.301SPS	19.8Hz				
160SPS	160.6SPS	118Hz				
320SPS	321.608SPS	154Hz				
640SPS	643.21SPS	495Hz				
1000SPS	1000SPS	732Hz				
2000SPS	2000SPS	1465Hz				

(1) Values shown for f_{OSC} = 4.096MHz.

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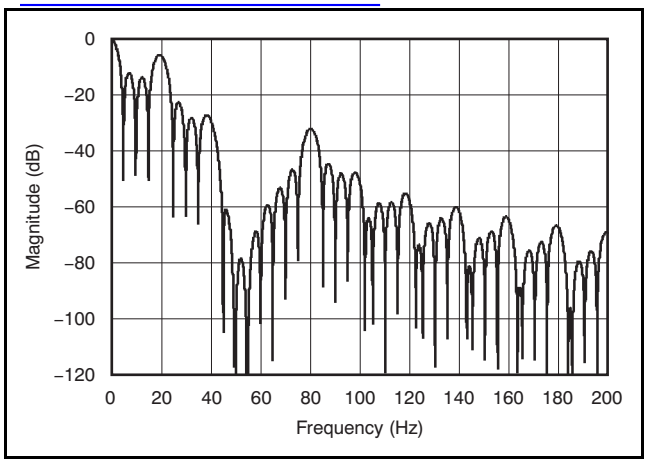

Figure 34. Filter Profile with Data Rate = 5SPS

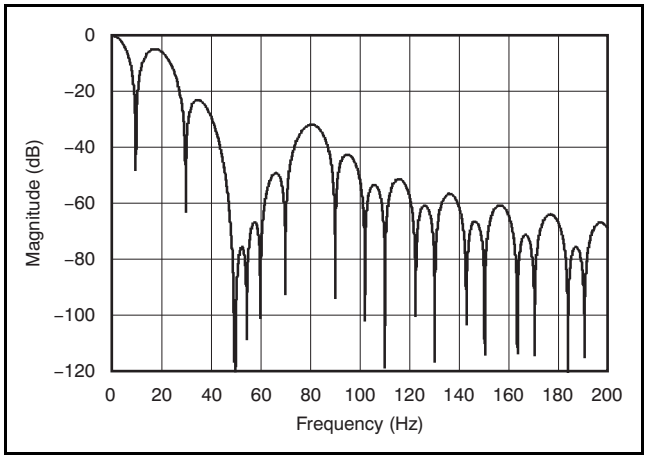

Figure 35. Filter Profile with Data Rate = 10SPS

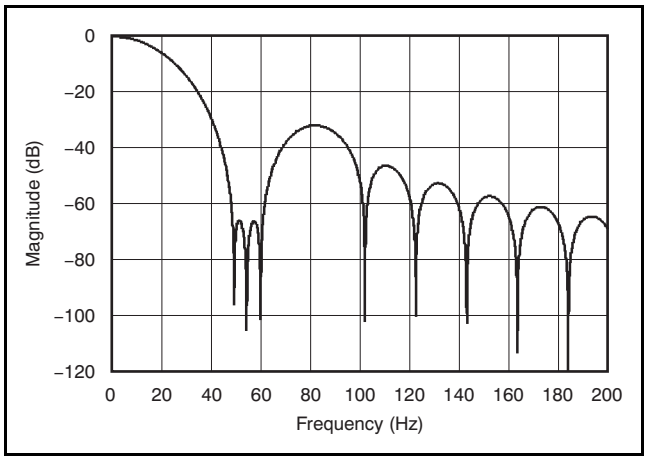

Figure 36. Filter Profile with Data Rate = 20SPS

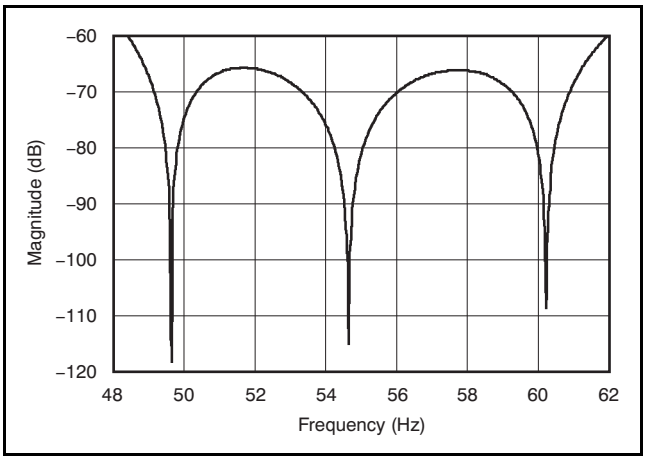

Figure 37. Detailed View of Filter Profile with Data Rate = 20SPS between 48Hz and 62Hz

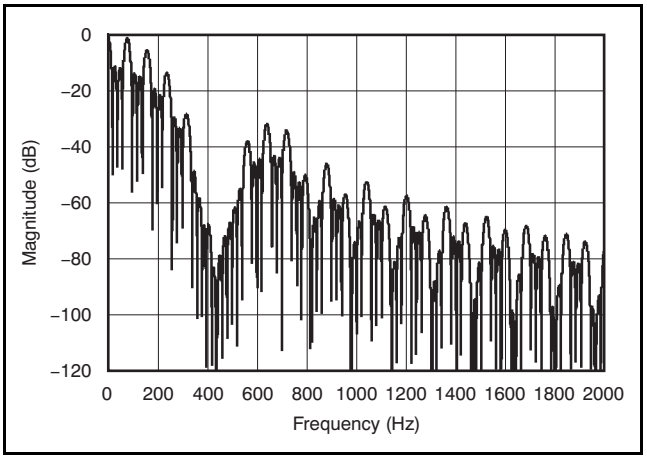

Figure 38. Filter Profile with Data Rate = 40SPS

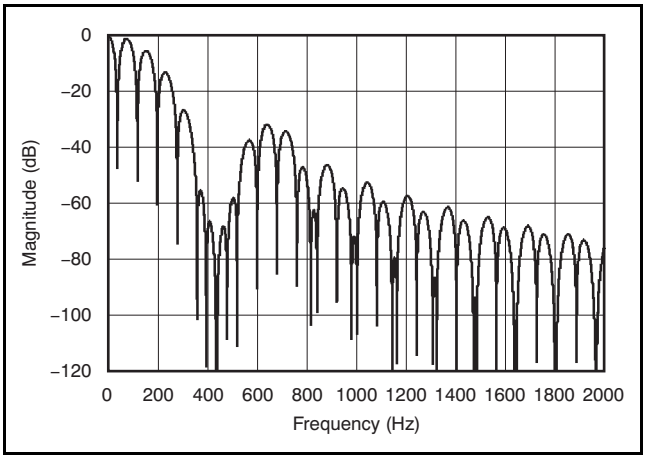

Figure 39. Filter Profile with Data Rate = 80SPS

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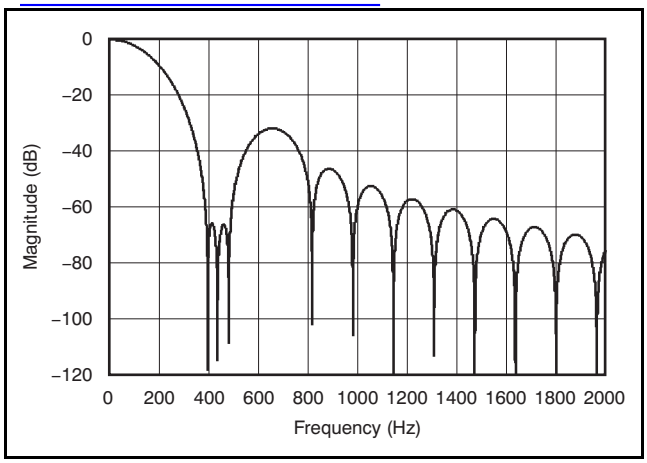

Figure 40. Filter Profile with Data Rate = 160SPS

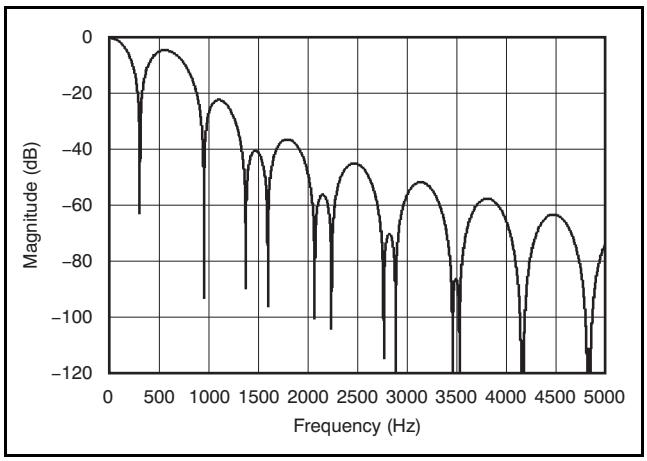

Figure 41. Filter Profile with Data Rate = 320SPS

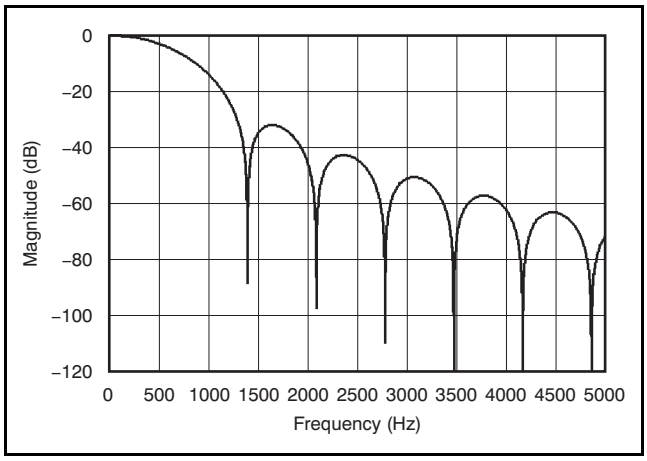

Figure 42. Filter Profile with Data Rate = 640SPS

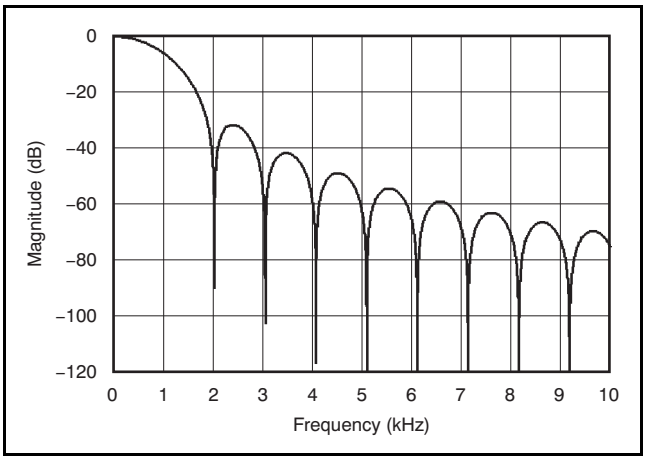

Figure 43. Filter Profile with Data Rate = 1kSPS

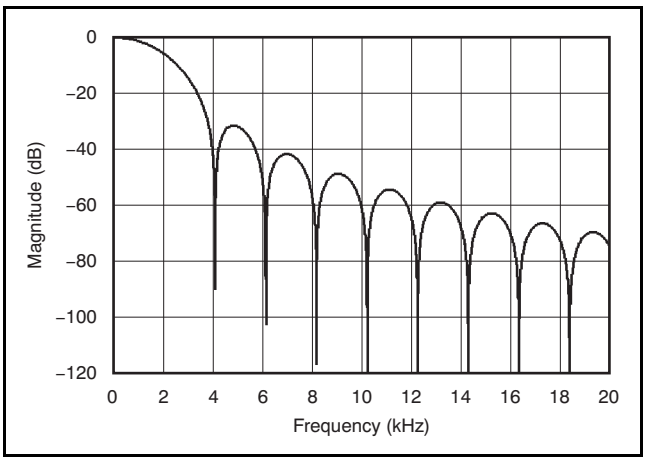

Figure 44. Filter Profile with Data Rate = 2kSPS

CLOCK SOURCE

The ADS1246/7/8 can use either the internal oscillator or an external clock. Connect the CLK pin to DGND before power-on or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator, with the device then operating on the external clock. After the device switches to the external clock, it cannot be switched back to the internal oscillator without cycling the power supplies or resetting the device.

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INTERNAL VOLTAGE REFERENCE

The ADS1247/48 includes an onboard voltage reference with a low temperature coefficient. The output of the voltage reference is 2.048V with the capability of both sourcing and sinking up to 10mA of current.

The voltage reference must have a capacitor connected between VREFOUT and VREFCOM. The value of the capacitance should be in the range of 1µF to 47µF. Large values provide more filtering of the reference; however, the turn-on time increases with capacitance, as shown in Table 13. For stability reasons, VREFCOM must have a path with an impedance less than 10Ω to ac ground nodes, such as AVSS (for a 0V to 5V analog power supply), or GND (for a ±2.5V analog power supply). In case this impedance is higher than 10Ω, a capacitor of at least 0.1µF should be connected between VREFCOM and an ac ground node (for example, GND). Note that because it takes time for the voltage reference to settle to the final voltage, care must be taken when the device is turned off between conversions. Allow adequate time for the internal reference to fully settle.

Table 13. Internal Reference Settling Time

VREFOUT CAPACITOR	SETTLING ERROR	TIME TO REACH THE SETTLING ERROR
1µF	±0.5%	70µs
	±0.1%	110µs
4.7µF	±0.5%	290µs
	±0.1%	375µs
47µF	±0.5%	2.2ms
	±0.1%	2.4ms

The onboard reference is controlled by the registers; by default, it is off after startup (see the *ADS1247/48 Detailed Register Definitions* section for more details). Therefore, the internal reference must first be turned on and then connected via the internal reference multiplexer. Because the onboard reference is used to generate the current reference for the excitation current sources, it must be turned on before the excitation currents become available.

EXCITATION CURRENT SOURCE DACS

The ADS1247/48 provide two matched excitation current sources for RTD applications. For three- or four-wire RTD applications, the matched current sources can be used to cancel the errors caused by sensor lead resistance. The output current of the current source DACs can be programmed to 50µA, 100µA, 250µA, 500µA, 750µA, 1000µA, or 1500µA.

The two matched current sources can be connected to dedicated current output pins IOUT1 and IOUT2 (ADS1248 only), or to any AIN pin (ADS1247/48); refer to the *ADS1247/48 Detailed Register Definitions* section for more information. It is possible to connect both current sources to the same pin. Note that the internal reference must be turned on and properly compensated when using the excitation current source DACs.

SENSOR DETECTION

The ADS1246/7/8 provide a selectable current (0.5µA, 2µA, or 10µA) to help detect a possible sensor malfunction.

When enabled, two burnout current sources flow through the selected pair of analog inputs to the sensor. One sources the current to the positive input channel, and the other sinks the same current from the negative input channel.

When the burnout current sources are enabled, a full-scale reading may indicate an open circuit in the front-end sensor, or that the sensor is overloaded. It may also indicate that the reference voltage is absent. A near-zero reading may indicate a short-circuit in the sensor.

BIAS VOLTAGE GENERATION

A selectable bias voltage is provided for use with ungrounded thermocouples. The bias voltage is (AVDD + AVSS)/2 and can applied to any analog input channel through internal input multiplexer. The bias voltage turn-on times for different sensor capacitances are listed in Table 14.

Table 14. Bias Voltage Settling Time

SENSOR CAPACITANCE	SETTLING TIME
0.1µF	220µs
1µF	2.2ms
10µF	22ms
200µF	450ms

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GENERAL-PURPOSE DIGITAL I/O

The ADS1248 has eight pins and the ADS1247 has four pins that serve a dual purpose as either analog inputs or general-purpose digital inputs/outputs (GPIOs).

Figure 45 shows a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the ADS1247/48 are operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken loading the GPIO pins when used as outputs because large currents can cause droop or noise on the analog supplies.

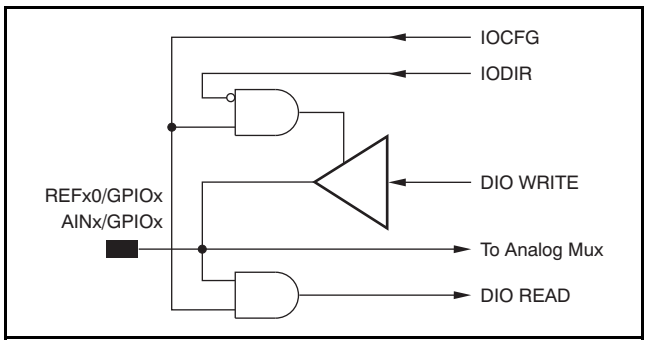

Figure 45. Analog/Data Interface Pin

SYSTEM MONITOR

The ADS1247 and ADS1248 provide a system monitor function. This function can measure the analog power supply, digital power supply, external voltage reference, or ambient temperature. Note that the system monitor function provides a coarse result. When the system monitor is enabled, the analog inputs are disconnected.

Power-Supply Monitor

The system monitor can measure the analog or digital power supply. When measuring the power supply, the resulting conversion is approximately 1/4 of the actual power supply voltage.

$$\text{Conversion Result} = (V_{SP}/4)/V_{REF} \quad (5)$$

Where V_{SP} is the selected supply to be measured.

External Voltage Reference Monitor

The ADS1246/7/8 can be selected to measure the external voltage reference. In this configuration, the monitored external voltage reference is connected to the analog input. The result (conversion code) is approximately 1/4 of the actual reference voltage.

$$\text{Conversion Result} = (V_{REX}/4)/V_{REF} \quad (6)$$

Where V_{REX} is the external reference to be monitored.

NOTE: The internal reference voltage must be enabled when measuring an external voltage reference using the system monitor.

Ambient Temperature Monitor

On-chip diodes provide temperature-sensing capability. When selecting the temperature monitor function, the anodes of two diodes are connected to the ADC. Typically, the difference in diode voltage is 118mV at +25°C with a temperature coefficient of 405µV/°C.

Note that when the onboard temperature monitor is selected, the PGA is automatically set to '1'. However, the PGA register bits in are not affected and the PGA returns to its set value when the temperature monitor is turned off.

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CALIBRATION

The conversion data are scaled by offset and gain registers before yielding the final output code. As shown in Figure 46, the output of the digital filter is first subtracted by the offset register (OSC) and then multiplied by the full-scale register (OSC). A digital clipping circuit ensures that the output code does not exceed 24 bits. Equation 7 shows the scaling.

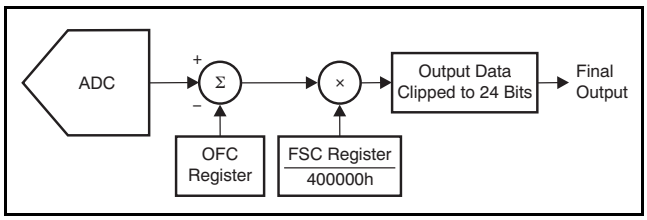

Figure 46. Calibration Block Diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:0]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (7)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

Offset Calibration Register: OFC[2:0]

The offset calibration is a 24-bit word, composed of three 8-bit registers. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. This value is subtracted from the conversion data. A register value of 000000h provides no offset correction. Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 15), make sure to avoid overloading the analog inputs.

Table 15. Final Output Code versus Offset Calibration Register Setting

OFFSET REGISTER	FINAL OUTPUT CODE WITH V_{IN} = 0(1)
7FFFFFh	8000000h
000001h	FFFFFFh
000000h	000000h
FFFFFFh	000000h
8000000h	7FFFFFh

1. Excludes effects of noise and inherent offset errors.

Full-Scale Calibration Register: FSC[2:0]

The full-scale or gain calibration is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is 24-bit, straight binary, normalized to 1.0 at code 400000h. Table 16 summarizes the scaling of the full-scale register. Note that while the full-scale calibration register can correct gain errors > 1 (with gain scaling < 1), make sure to avoid overloading the analog inputs. The default or reset value of FSC depends on the PGA setting. A different factory-trimmed FSC Reset value is stored for each PGA setting which provides outstanding gain accuracy over all the ADS1246/7/8 input ranges. **Note:** The factory-trimmed FSC reset value loads automatically loaded whenever the PGA setting changes.

Table 16. Gain Correction Factor versus Full-Scale Calibration Register Setting

FULL-SCALE REGISTER	GAIN SCALING
800000h	2.0
400000h	1.0
200000h	0.5
000000h	0

Calibration Commands

The ADS1246/7/8 provide commands for three types of calibration: system gain calibration, system offset calibration and self offset calibration. Where absolute accuracy is needed, it is recommended that calibration be performed after power on, a change in temperature, a change of PGA and in some cases a change in channel. At the completion of calibration, the $\overline{\text{DRDY}}$ signal goes low indicating the calibration is finished. The first data after calibration are always valid. If the START pin is taken low or a SLEEP command is issued after any calibration command, the devices goes to sleep after completing calibration.

System Gain Calibration

System gain calibration corrects for gain error in the signal path. The system gain calibration is initiated by sending the SYSGCAL command while applying a full-scale input to the selected analog inputs. Afterwards the full-scale calibration register (FSC) is updated. When a system gain calibration command is issued, the ADS1246/7/8 stop the current conversion and start the calibration procedure immediately.

System Offset and Self Offset Calibration

System offset calibration corrects both internal and external offset errors. The system offset calibration is initiated by sending the SYSGOCAL command while applying a zero differential input (V_{IN} = 0) to the selected analog inputs. The self offset calibration is initiated by sending the SELFOCAL command. During self offset calibration, the selected inputs are disconnected from the internal circuitry and a zero differential signal is applied internally. With both offset

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calibrations the offset calibration register (OFC) is updated afterwards. When either offset calibration command is issued, the ADS1246/7/8 stop the current conversion and start the calibration procedure immediately.

Calibration Timing

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This provides a more accurate calibration value. The time required for calibration is shown in Table 17 and can be calculated using Equation 8:

$$\text{Calibration Time} = \frac{50}{f_{OSC}} + \frac{32}{f_{MOD}} + \frac{16}{f_{DATA}} \quad (8)$$

Table 17. Calibration Time versus Data Rate

DATA RATE (SPS)	CALIBRATION TIME (ms)(1)
5	3201.01
10	1601.01
20	801.012
40	400.26
80	200.26
160	100.14
320	50.14
640	25.14
1000	16.14
2000	8.07

1. For f_{OSC} = 4.096MHz.

ADC SLEEP MODE

Power consumption can be dramatically reduced by placing the ADS1246/7/8 into sleep mode. There are two ways to put the device into sleep mode: the sleep command (SLEEP) and through the START pin.

During sleep mode, the internal reference status depends on the setting of the VREFCON bits in the MUX1 register; see the *Register Descriptions* section for details.

ADC CONTROL

ADC Conversion Control

The START pin provides easy and precise control of conversions. Pulse the START pin high to begin a conversion, as shown in Figure 47 and Table 18. The conversion completion is indicated by the DOUT/DRDY pin going low. When the conversion completes, the ADS1246/7/8 automatically shuts down to save power. During shutdown, the conversion result can be retrieved; however, START must be taken high before communicating with the configuration registers. The device stays shut down until the START pin is once again taken high to begin a new conversion. When the START pin is taken back high again, the decimation filter is held in a reset state for 32 modulator clock cycles internally to allow the analog circuits to settle.

The ADS1246/7/8 can be configured to convert continuously by holding the START pin high, as shown in Figure 48. With the START pin held high, the ADC converts the selected input channels continuously. This configuration continues until the START pin is taken low.

The START pin can also be used to perform the synchronized measurement for the multi-channel applications by pulsing the START pin.

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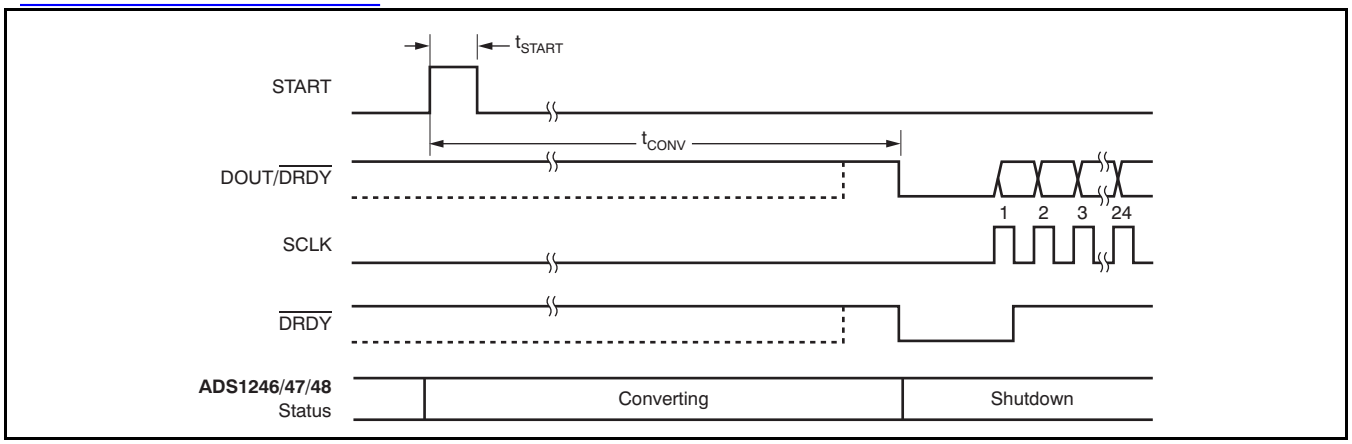
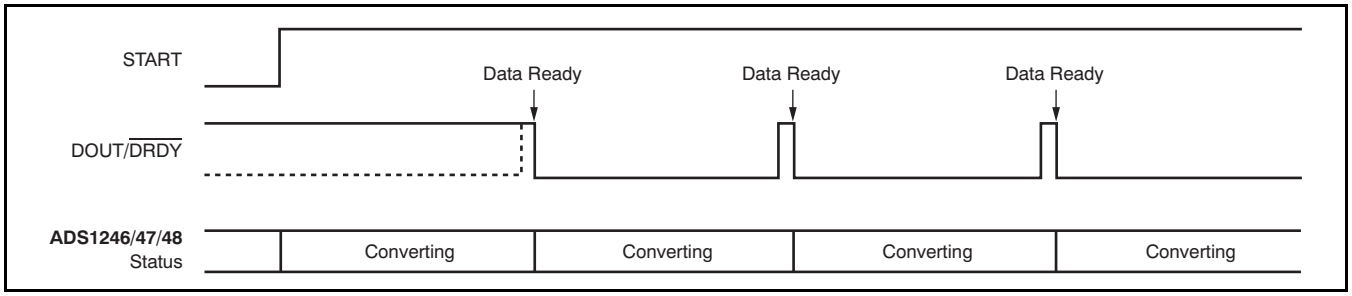


Figure 47. Timing for Single Conversion Using START Pin

Table 18. START Pin Conversion Times for Figure 47

SYMBOL	DESCRIPTION	DATA RATE (SPS)	VALUE	UNIT
t_{CONV}	Time from START pulse to $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ going low	5	200.295	ms
		10	100.644	ms
		20	50.825	ms
		40	25.169	ms
		80	12.716	ms
		160	6.489	ms
		320	3.247	ms
		640	1.692	ms
		1000	1.138	ms
		2000	0.575	ms



NOTE: SCLK held low in this example.

Figure 48. Timing for Conversion with START Pin High

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RESET

When the RESET pin goes low, the device is immediately reset. All the registers are restored to default values. The device stays in reset mode as long as the RESET pin stays low. When it goes high, the ADC comes out of reset mode and is able to convert data. After the RESET pin goes high, and when the system clock frequency is 4.096MHz, the digital filter and the registers are held in a reset state for 0.6ms when f_{OSC} = 4.096MHz. Therefore, valid SPI communication can only be resumed 0.6ms after the RESET pin goes high, as shown in Figure 4. When the RESET pin goes low, the clock selection is reset to the internal oscillator.

Digital Filter Reset Operation

Apart from the RESET command and the RESET pin, the digital filter is reset automatically when either a write operation to the MUX0, VBIAS, MUX1, or SYS0 registers is performed, when a SYNC command is issued, or the START pin is taken high.

The filter is reset two system clocks after the last bit of the SYNC command is sent. The reset pulse created internally lasts for two multiplier clock cycles. If any write operation takes place in the MUX0 register, the filter is reset regardless of whether the value changed or not. Internally, the filter pulse lasts for two system clock periods. If any write activity takes place in the VBIAS, MUX1, or SYS0 registers, the filter is reset as well, regardless of whether the value changed or not. The reset pulse lasts for 32 modulator clocks after the write operation. If there are multiple write operations, the resulting reset pulse may be viewed as the ANDed result of the different active low pulses created individually by each action.

Table 19 shows the conversion time after a filter reset. Note that this time depends on the operation initiating the reset. Also, the first conversion after a filter reset has a slightly different time than the second and subsequent conversions.

Table 19. Data Conversion Time

NOMINAL DATA RATE (SPS)	EXACT DATA RATE (SPS)	FIRST DATA CONVERSION TIME AFTER FILTER RESET				SECOND AND SUBSEQUENT CONVERSION TIME AFTER FILTER RESET	
		SYNC COMMAND, MUX0 REGISTER WRITE		HARDWARE RESET, RESET COMMAND, START PIN HIGH, WAKEUP COMMAND, VBIAS, MUX1, or SYS0 REGISTER WRITE			
		(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)	NO. OF SYSTEM CLOCK CYCLES
5	5.019	199.264	816188	200.266	820290	199.250	816128
10	10.038	99.639	408124	100.641	412226	99.625	408064
20	20.075	49.827	204092	50.828	208194	49.812	204032
40	40.151	24.920	102076	25.172	103106	24.906	102016
80	80.301	12.467	51068	12.719	52098	12.453	51008
160	160.602	6.241	25564	6.492	26594	6.226	25504
320	321.608	3.124	12796	3.250	13314	3.109	12736
640	643.216	1.569	6428	1.695	6946	1.554	6368
1000	1000.000	1.014	4156	1.141	4674	1.000	4096
2000	2000.000	0.514	2108	0.578	2370	0.500	2048

(1) For f_{OSC} = 4.096MHz.

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Data Format

The ADS1246/7/8 output 24 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(V_{REF}/PGA)/(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 20 summarizes the ideal output codes for different input signals.

Table 20. Ideal Output Code vs Input Signal

INPUT SIGNAL, V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE(1)
≥ $+V_{REF}/PGA$	7FFFFFh
$(+V_{REF}/PGA)/(2^{23} - 1)$	000001h
0	000000h
$(-V_{REF}/PGA)/(2^{23} - 1)$	FFFFFFh
≤ $-(V_{REF}/PGA) \times (2^{23}/2^{23} - 1)$	800000h

(1) Excludes effects of noise, linearity, offset, and gain errors.

Digital Interface

The ADS1246/7/8 provide a standard SPI serial communication interface plus a data ready signal ($\overline{DRDY}$). Communication is full-duplex with the exception of a few limitations in regards to the RREG command and the RDATA command. These limitations are explained in detail in the *SPI Commands* section of this data sheet. For the basic serial interface timing characteristics, see Figure 1 and Figure 2 of this datasheet.

$\overline{CS}$

The chip select pin (active low). The $\overline{CS}$ pin activates SPI communication. $\overline{CS}$ must be low before data transactions and must stay low for the entire SPI communication period. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin enters a high-impedance state. Therefore, reading and writing to the serial interface are ignored and the serial interface is reset. $\overline{DRDY}$ pin operation is independent of $\overline{CS}$.

Taking $\overline{CS}$ high deactivates only the SPI communication with the device. Data conversion continues and the $\overline{DRDY}$ signal can be monitored to check if a new conversion result is ready. A master device monitoring the $\overline{DRDY}$ signal can select the appropriate slave device by pulling the $\overline{CS}$ pin low.

SCLK

The serial clock signal. SCLK provides the clock for serial communication. It is a Schmitt-trigger input, but it is highly recommended that SCLK be kept as clean as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the falling edge of SCLK and shifted out of DOUT on the rising edge of SCLK.

DIN

The data input pin. DIN is used along with SCLK to send data to the device. Data on DIN are shifted into the device on the falling edge of SCLK.

The communication of this device is full-duplex in nature. The device monitors commands shifted in even when data are being shifted out. Data that are present in the output shift register are shifted out when sending in a command. Therefore, it is important to make sure that whatever is being sent on the DIN pin is valid when shifting out data. When no command is to be sent to the device when reading out data, the NOP command should be sent on DIN.

$\overline{DRDY}$

The data ready pin. The $\overline{DRDY}$ pin goes low to indicate a new conversion is complete, and the conversion result is stored in the conversion result buffer. The SPI clock must be low in a short time frame around the $\overline{DRDY}$ low transition (see Figure 2) so that the conversion result is loaded into both the result buffer and the output shift register. Therefore, no commands should be issued during this time frame if the conversion result is to be read out later. This constraint applies only when $\overline{CS}$ is asserted. When $\overline{CS}$ is not asserted, SPI communication with other devices on the SPI bus does not affect loading of the conversion result. After the $\overline{DRDY}$ pin goes low, it is forced high on the first falling edge of SCLK (so that the $\overline{DRDY}$ pin can be polled for '0' instead of waiting for a falling edge). If the $\overline{DRDY}$ pin is not taken high after it falls low, a short high pulse is created on it to indicate the next data are ready.

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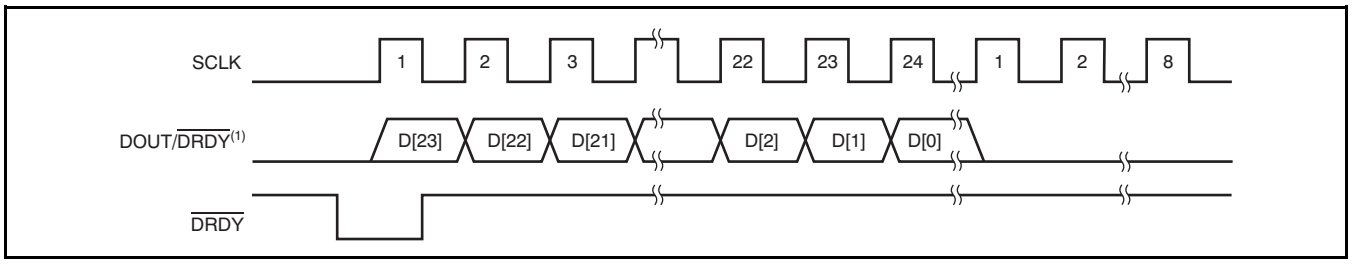
DOUT/$\overline{\text{DRDY}}$

This pin has two modes: data out (DOUT) only, or data out (DOUT) combined with data ready ($\overline{\text{DRDY}}$). The DRDY MODE bit determines the function of this pin. In either mode, the DOUT/$\overline{\text{DRDY}}$ pin goes to a high-impedance state when $\overline{\text{CS}}$ is taken high.

When the DRDY MODE bit is set to '0', this pin functions as DOUT only. Data are clocked out at rising edge of SCLK, MSB first (see Figure 49).

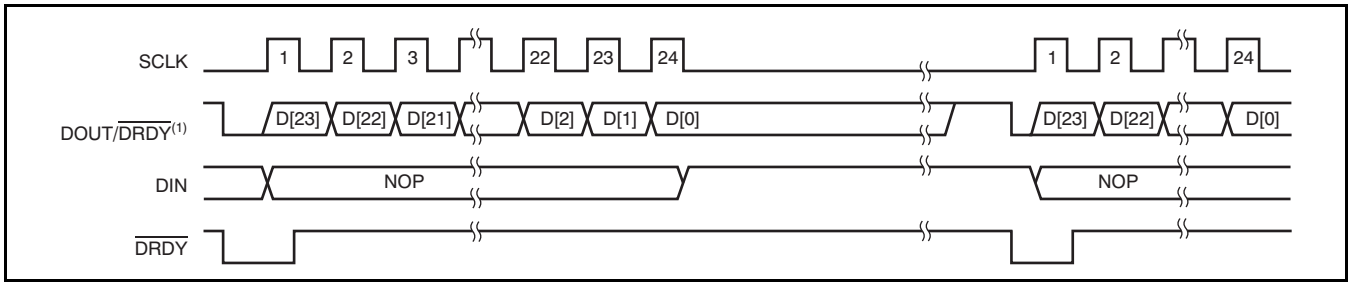
When the DRDY MODE bit is set to '1', this pin functions as both DOUT and $\overline{\text{DRDY}}$. Data are shifted out from this pin, MSB first, at the rising edge of SCLK. This combined pin allows for the same control but with fewer pins.

When the DRDY MODE bit is enabled and a new conversion is complete, DOUT/$\overline{\text{DRDY}}$ goes low if it is high. If it is already low, then DOUT/$\overline{\text{DRDY}}$ goes high and then goes low (see Figure 50). Similar to the $\overline{\text{DRDY}}$ pin, a falling edge on the DOUT/$\overline{\text{DRDY}}$ pin signals that a new conversion result is ready. After DOUT/$\overline{\text{DRDY}}$ goes low, the data can be clocked out by providing 24 SCLKs. In order to force DOUT/$\overline{\text{DRDY}}$ high (so that DOUT/$\overline{\text{DRDY}}$ can be polled for a '0' instead of waiting for a falling edge), a no operation command (NOP) or any other command that does not load the data output register can be sent after reading out the data. Because SCLKs can only be sent in multiples of eight, a NOP can be sent to force DOUT/$\overline{\text{DRDY}}$ high if no other command is pending. The DOUT/$\overline{\text{DRDY}}$ pin goes high after the first rising edge of SCLK after reading the conversion result completely (see Figure 51). The same condition also applies after an RREG command. After all the register bits have been read out, the rising edge of SCLK forces DOUT/$\overline{\text{DRDY}}$ high. Figure 52 illustrates an example where sending four NOP commands after an RREG command forces the DOUT/$\overline{\text{DRDY}}$ pin high.



(1) $\overline{\text{CS}}$ tied low.

Figure 49. Data Retrieval with the DRDY MODE Bit = 0 (Disabled)



(1) $\overline{\text{CS}}$ tied low.

Figure 50. Data Retrieval with the DRDY MODE Bit = 1 (Enabled)

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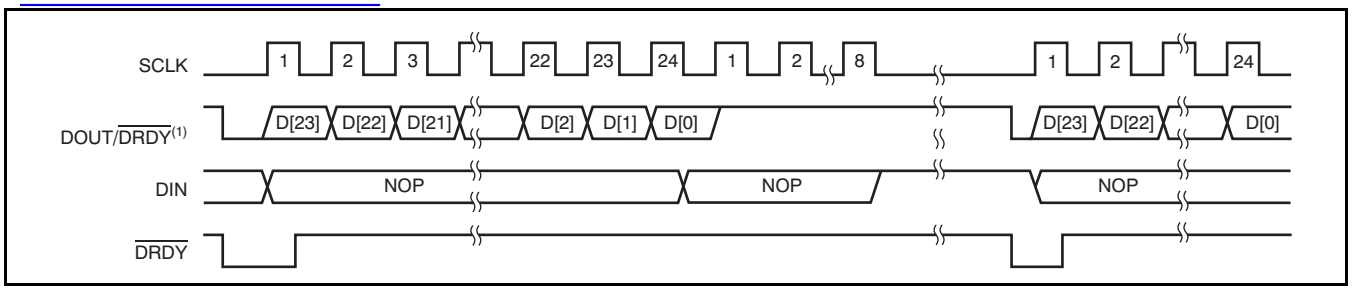
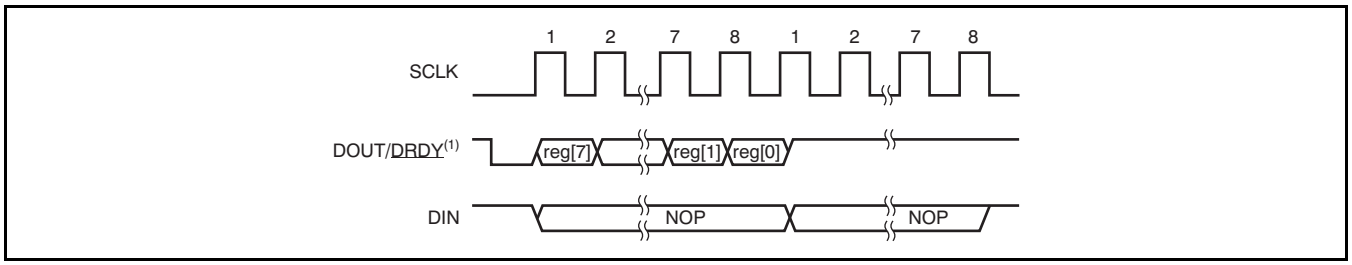


(1) DRDY MODE bit enabled, $\overline{CS}$ tied low.

Figure 51. DOUT/$\overline{DRDY}$ Forced High After Retrieving the Conversion Result



(1) DRDY MODE bit enabled, $\overline{CS}$ tied low.

Figure 52. DOUT/$\overline{DRDY}$ Forced High After Reading Register Data

The DRDY MODE bit modifies only the DOUT/$\overline{DRDY}$ pin functionality. The $\overline{DRDY}$ pin functionality remains unaffected.

SPI Reset

SPI communication can be reset in several ways. In order to reset the SPI interface (without resetting the registers or the digital filter), the $\overline{CS}$ pin can be pulled high. Taking the $\overline{RESET}$ pin low causes the SPI interface to be reset along with all the other digital functions. In this case, the registers and the conversion are reset.

SPI Communication During Sleep Mode

When the START pin is low or the device is in sleep mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result during sleep mode. Other commands do not function because the internal clock is shut down to save power during sleep mode.

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REGISTER DESCRIPTIONS

ADS1246 REGISTER MAP

Table 21. ADS1246 Register Map

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	BCS	BCS1	BCS0	0	0	0	0	0	1
01h	VBIAS	0	0	0	0	0	0	VBIAS1	VBIAS0
02h	MUX1	CLKSTAT	0	0	0	0	MUXCAL2	MUXCAL1	MUXCAL0
03h	SYS0	0	PGA2	PGA1	PGA0	DR3	DR2	DR1	DR0
04h	OFC0	OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0
05h	OFC1	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC9	OFC8
06h	OFC2	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
07h	FSC0	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0
08h	FSC1	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8
09h	FSC2	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
0Ah	ID	ID3	ID2	ID1	ID0	DRDY MODE	0	0	0

ADS1246 DETAILED REGISTER DEFINITIONS

BCS—Burnout Current Source Register. These bits control the settling of the sensor burnout detect current source.

BCS - ADDRESS 00h							RESET VALUE = 01h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BCS1	BCS0	0	0	0	0	0	1

Bits 7:6 **BCS1:0**
These bits select the magnitude of the sensor burnout detect current source.
00 = Burnout current source off (default)
01 = Burnout current source on, 0.5µA
10 = Burnout current source on, 2µA
11 = Burnout current source on, 10µA

Bits 5:0 **These bits must always be set to '000001'.**

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ADS1246 DETAILED REGISTER DEFINITIONS (continued)

VBIAS—Bias Voltage Register. This register enables a bias voltage on the analog inputs.

VBIAS - ADDRESS 01h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	VBIAS1	VBIAS0

Bits 7:2 **These bits must always be set to '000000'.**

Bits 1:0 **VBIAS1:0**
These bits apply a bias voltage of midsupply (AVDD + AVSS)/2 to the selected analog input. Bit 0 is for AIN0, and bit 1 is for AIN1.
0 = Bias voltage not enabled (default)
1 = Bias voltage is applied to the analog input

MUX—Multiplexer Control Register.

MUX - ADDRESS 02h							RESET VALUE = x0h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLKSTAT	0	0	0	0	MUXCAL2	MUXCAL1	MUXCAL0

Bit 7 **CLKSTAT**
This bit is read-only and indicates whether the internal or external oscillator is being used.
0 = Internal oscillator in use
1 = External oscillator in use

Bits 6:3 **These bits must always be set to '0000'.**

Bits 2:0 **MUXCAL2:0**
These bits are used to select a system monitor. The MUXCAL selection supercedes selections from the VBIAS register.
000 = Normal operation (default)
001 = Offset calibration. The analog inputs are disconnected and AINP and AINN are internally connected to midsupply (AVDD + AVSS)/2.
010 = Gain calibration. The analog inputs are connected to the voltage reference.
011 = Temperature measurement. The inputs are connected to a diode circuit that produces a voltage proportional to the ambient temperature of the device..

Table 22 lists the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

Table 22. MUXCAL Settings

MUXCAL[2:0]	PGA GAIN SETTING	ADC INPUT
000	Set by SYS0 register	Normal operation
001	Set by SYS0 register	Offset calibration: inputs shorted to midsupply (AVDD + AVSS)/2
010	Forced to 1	Gain calibration: $V_{REFP} – V_{REFN}$ (full-scale)
011	Forced to 1	Temperature measurement diode

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ADS1246 DETAILED REGISTER DEFINITIONS (continued)

SYS0—System Control Register 0.

SYS0 - ADDRESS 03h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	PGA2	PGA1	PGA0	DOR3	DOR2	DOR1	DOR0

Bit 7 **These bits must always be set to '0'.**

Bits 6:4 **PGA2:0**
These bits determine the gain of the PGA.
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

Bits 3:0 **DOR3:0**
These bits select the output data rate of the ADC. Bits with a value higher than 1001 select the highest data rate of 2kSPS.
0000 = 5SPS (default)
0001 = 10SPS
0010 = 20SPS
0011 = 40SPS
0100 = 80SPS
0101 = 160SPS
0110 = 320SPS
0111 = 640SPS
1000 = 1000SPS
1001 to 1111 = 2000SPS

OFC23:0

These bits make up the offset calibration coefficient register of the ADS1248.

OFC0—Offset Calibration Coefficient Register 0

OFC0 - ADDRESS 04h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0

OFC1—Offset Calibration Coefficient Register 1

OFC1 - ADDRESS 05h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC9	OFC8

OFC2—Offset Calibration Coefficient Register 2

OFC2 - ADDRESS 06h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

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ADS1246 DETAILED REGISTER DEFINITIONS (continued)

FSC23:0

These bits make up the full-scale calibration coefficient register.

FSC0—Full-Scale Calibration Coefficient Register 0

FSC0 - ADDRESS 07h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC1—Full-Scale Calibration Coefficient Register 1

FSC1 - ADDRESS 08h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC2—Full-Scale Calibration Coefficient Register 2

FSC2 - ADDRESS 09h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

ID—ID Register

IDAC0 - ADDRESS 0Ah							RESET VALUE = x0h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ID3	ID2	ID1	ID0	DRDY MODE	0	0	0

Bits 7:4 **ID3:0**
Read-only, factory-programmed bits; used for revision identification.

Bit 3 **DRDY MODE**
This bit sets the DOUT/$\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low.
0 = DOUT/$\overline{\text{DRDY}}$ pin functions only as Data Out (default)
1 = DOUT/$\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low

Bits 2:0 **These bits must always be set to '000'.**

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ADS1247 AND ADS1248 REGISTER MAP

Table 23. ADS1247 and ADS1248 Register Map

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MUX0	BCS1	BCS0	MUX_SP2	MUX_SP1	MUX_SP0	MUX_SN2	MUX_SN1	MUX_SN0
01h	VBIAS	VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0
02h	MUX1	CLKSTAT	VREFCON1	VREFCON0	REFSELT1	REFSELT0	MUXCAL2	MUXCAL1	MUXCAL0
03h	SYS0	0	PGA2	PGA1	PGA0	DR3	DR2	DR1	DR0
04h	OFC0	OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0
05h	OFC1	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC9	OFC8
06h	OFC2	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
07h	FSC0	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0
08h	FSC1	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8
09h	FSC2	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
0Ah	IDAC0	ID3	ID2	ID1	ID0	DRDY MODE	IMAG2	IMAG1	IMAG0
0Bh	IDAC1	I1DIR3	I1DIR2	I1DIR1	I1DIR0	I2DIR3	I2DIR2	I2DIR1	I2DIR0
0Ch	GPIOCFG	IOCFG7	IOCFG6	IOCFG5	IOCFG4	IOCFG3	IOCFG2	IOCFG1	IOCFG0
0Dh	GPIODIR	IODIR7	IODIR6	IODIR5	IODIR4	IODIR3	IODIR2	IODIR1	IODIR0
0Eh	GPIODAT	IODAT7	IODAT6	IODAT5	IODAT4	IODAT3	IODAT2	IODAT1	IODAT0

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS

MUX0—Multiplexer Control Register 0. This register allows any combination of differential inputs to be selected on any of the input channels. Note that this setting can be superceded by the MUXCAL and VBIAS bits.

MUX0 - ADDRESS 00h							RESET VALUE = 01h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BCS1	BCS0	MUX_SP2	MUX_SP1	MUX_SP0	MUX_SN2	MUX_SN1	MUX_SN0

Bits 7:6 **BCS1:0**
These bits select the magnitude of the sensor detect current source.
00 = Burnout current source off (default)
01 = Burnout current source on, 0.5µA
10 = Burnout current source on, 2µA
11 = Burnout current source on, 10µA

Bits 5:3 **MUX_SP2:0**
Positive input channel selection bits.
000 = AIN0 (default)
001 = AIN1
010 = AIN2
011 = AIN3
100 = AIN4 (ADS1248 only)
101 = AIN5 (ADS1248 only)
110 = AIN6 (ADS1248 only)
111 = AIN7 (ADS1248 only)

Bits 2:0 **MUX_SN2:0**
Negative input channel selection bits.
000 = AIN0
001 = AIN1 (default)
010 = AIN2
011 = AIN3
100 = AIN4 (ADS1248 only)
101 = AIN5 (ADS1248 only)
110 = AIN6 (ADS1248 only)
111 = AIN7 (ADS1248 only)

VBIAS—Bias Voltage Register

VBIAS - ADDRESS 01h								RESET VALUE = 00h
DEVICE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ADS1248	VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0
ADS1247	0	0	0	0	VBIAS3	VBIAS2	VBIAS1	VBIAS0

Bits 7:0 **VBIAS7:0**
These bits apply a bias voltage of midsupply (AVDD + AVSS)/2 to the selected analog input.
0 = Bias voltage not enabled (default)
1 = Bias voltage is applied on the corresponding analog input (bit 0 corresponds to AIN0, etc.).

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS (continued)

MUX1—Multiplexer Control Register 1

MUX1 - ADDRESS 02h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLKSTAT	VREFCON1	VREFCON0	REFSELT1	REFSELT0	MUXCAL2	MUXCAL1	MUXCAL0

Bit 7 **CLKSTAT**
This bit is read-only and indicates whether the internal or external oscillator is being used.
0 = Internal oscillator in use
1 = External oscillator in use

Bits 6:5 **VREFCON1:0**
These bits control the internal voltage reference. These bits allow the reference to be turned on or off completely, or allow the reference state to follow the state of the device. Note that the internal reference is required for operation of the IDAC functions.
00 = Internal reference is always off (default)
01 = Internal reference is always on
10 or 11 = Internal reference is on when a conversion is in progress and shuts down when the device receives a shutdown opcode or the START pin is taken low

Bits 4:3 **REFSELT1:0**
These bits select the reference input for the ADC.
00 = REF0 input pair selected (default)
01 = REF1 input pair selected (ADS1248 only)
10 = Onboard reference selected
11 = Onboard reference selected and internally connected to REF0 input pair

Bits 2:0 **MUXCAL2:0**
These bits are used to select a system monitor. The MUXCAL selection supercedes selections from registers MUX0 and MUX1 (MUX_SP, MUX_SN, and VBIAS).
000 = Normal operation (default)
001 = Offset measurement
010 = Gain measurement
011 = Temperature diode
100 = External REF1 measurement (ADS1248 only)
101 = External REF0 measurement
110 = AVDD measurement
111 = DVDD measurement

Table 24 provides the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

Table 24. MUXCAL Settings

MUXCAL[2:0]	PGA GAIN SETTING	ADC INPUT
000	Set by SYS0 register	Normal operation
001	Set by SYS0 register	Inputs shorted to midsupply (AVDD + AVSS)/2
010	Forced to 1	$V_{REFP} – V_{REFN}$ (full-scale)
011	Forced to 1	Temperature measurement diode
100	Forced to 1	$(V_{REFP1} – V_{REFN1})/4$
101	Forced to 1	$(V_{REFP0} – V_{REFN0})/4$
110	Forced to 1	(AVDD – AVSS)/4
111	Forced to 1	(DVDD – DVSS)/4

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS (continued)

SYS0—System Control Register 0

SYS0 - ADDRESS 03h							RESET VALUE = 00h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	PGA2	PGA1	PGA0	DOR3	DOR2	DOR1	DOR0

Bit 7 **This bit must always be set to '0'**

Bits 6:4 **PGA2:0**
These bits determine the gain of the PGA.
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

Bits 3:0 **DOR3:0**
These bits select the output data rate of the ADC. Bits with a value higher than 1001 select the highest data rate of 2000SPS.
0000 = 5SPS (default)
0001 = 10SPS
0010 = 20SPS
0011 = 40SPS
0100 = 80SPS
0101 = 160SPS
0110 = 320SPS
0111 = 640SPS
1000 = 1000SPS
1001 to 1111 = 2000SPS

OFC23:0

These bits make up the offset calibration coefficient register of the ADS1248.

OFC0—Offset Calibration Coefficient Register 0

OFC0 - ADDRESS 04h							RESET VALUE = 000000h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC7	OFC6	OFC5	OFC4	OFC3	OFC2	OFC1	OFC0

OFC1—Offset Calibration Coefficient Register 1

OFC1 - ADDRESS 05h							RESET VALUE = 000000h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC9	OFC8

OFC2—Offset Calibration Coefficient Register 2

OFC2 - ADDRESS 06h							RESET VALUE = 000000h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS (continued)

FSC23:0

These bits make up the full-scale calibration coefficient register.

FSC0—Full-Scale Calibration Coefficient Register 0

FSC0 - ADDRESS 07h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC1—Full-Scale Calibration Coefficient Register 1

FSC1 - ADDRESS 08h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC2—Full-Scale Calibration Coefficient Register 2

FSC2 - ADDRESS 09h							RESET VALUE IS PGA DEPENDENT(1)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note: the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

IDAC0—IDAC Control Register 0

IDAC0 - ADDRESS 0Ah							RESET VALUE = x0h
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ID3	ID2	ID1	ID0	DRDY MODE	IMAG2	IMAG1	IMAG0

Bits 7:4 **ID3:0**
Read-only, factory-programmed bits; used for revision identification.

Bit 3 **DRDY MODE**
This bit sets the DOUT/$\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low.
0 = DOUT/$\overline{\text{DRDY}}$ pin functions only as Data Out (default)
1 = DOUT/$\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low

Bits 2:0 **IMAG2:0**
The ADS1247/48 have two programmable current source DACs that can be used for sensor excitation. The IMAG bits control the magnitude of the excitation current. The IDACs require the internal reference to be on.
000 = off (default)
001 = 50µA
010 = 100µA
011 = 250µA
100 = 500µA
101 = 750µA
110 = 1000µA
111 = 1500µA

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS (continued)

IDAC1—IDAC Control Register 1

IDAC1 - ADDRESS 0Bh								RESET VALUE = FFh
DEVICE	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ADS1248	I1DIR3	I1DIR2	I1DIR1	I1DIR0	I2DIR3	I2DIR2	I2DIR1	I2DIR0
ADS1247	0	0	I1DIR1	I1DIR0	0	0	I2DIR1	I2DIR0

The two IDACs on the ADS1247/48 can be routed to either the IEXC1 and IEXC2 output pins or directly to the analog inputs.

Bits 7:4 **I1DIR3:0**

These bits select the output pin for the first current source DAC.
0000 = AIN0
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4 (ADS1248 only)
0101 = AIN5 (ADS1248 only)
0110 = AIN6 (ADS1248 only)
0111 = AIN7 (ADS1248 only)
10x0 = IEXT1 (ADS1248 only)
10x1 = IEXT2 (ADS1248 only)
11xx = Disconnected (default)

Bits 3:0 **I2DIR3:0**

These bits select the output pin for the second current source DAC.
0000 = AIN0
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4 (ADS1248 only)
0101 = AIN5 (ADS1248 only)
0110 = AIN6 (ADS1248 only)
0111 = AIN7 (ADS1248 only)
10x0 = IEXT1 (ADS1248 only)
10x1 = IEXT2 (ADS1248 only)
11xx = Disconnected (default)

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ADS1247 and ADS1248 DETAILED REGISTER DEFINITIONS (continued)

GPIOCFG—GPIO Configuration Register. The GPIO and analog pins are shared as follows:

GPIO0 shared with REFP0
GPIO1 shared with REFN0
GPIO2 shared with AIN2
GPIO3 shared with AIN3
GPIO4 shared with AIN4 (ADS1248)
GPIO5 shared with AIN5 (ADS1248)
GPIO6 shared with AIN6 (ADS1248)
GPIO7 shared with AIN7 (ADS1248)

GPIOCFG - ADDRESS 0Ch								RESET VALUE = 00h
DEVICE	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ADS1248	IOCFG7	IOCFG6	IOCFG5	IOCFG4	IOCFG3	IOCFG2	IOCFG1	IOCFG0
ADS1247	0	0	0	0	IOCFG3	IOCFG2	IOCFG1	IOCFG0

Bits 7:0 IOCFG7:0
These bits enable the GPIO because the GPIO pins are shared with the analog pins. Note that the ADS1248 uses all the IOCFG bits, whereas the ADS1247 uses only bits 3:0.
0 = The pin is used as an analog input (default)
1 = The pin is used as a GPIO pin

GPIODIR—GPIO Direction Register

GPIODIR - ADDRESS 0Dh								RESET VALUE = 00h
DEVICE	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ADS1248	IODIR7	IODIR6	IODIR5	IODIR4	IODIR3	IODIR2	IODIR1	IODIR0
ADS1247	0	0	0	0	IODIR3	IODIR2	IODIR1	IODIR0

Bits 7:0 IODIR7:0
These bits control the direction of the GPIO when enabled by the IOCFG bits. Note that the ADS1248 uses all the IODIR bits, whereas the ADS1247 uses only bits 3:0.
0 = The GPIO is an output (default)
1 = The GPIO is an input

GPIODAT—GPIO Data Register

GPIODAT - ADDRESS 0Eh								RESET VALUE = 00h
DEVICE	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
ADS1248	IODAT7	IODAT6	IODAT5	IODAT4	IODAT3	IODAT2	IODAT1	IODAT0
ADS1247	0	0	0	0	IODAT3	IODAT2	IODAT1	IODAT0

Bits 7:0 IODAT7:0
If a GPIO pin is enabled in the GPIOCFG register and configured as an output in the GPIO Direction register (GPIODIR), the value written to this register appears on the appropriate GPIO pin. If a GPIO pin is configured as an input in GPIODIR, reading this register returns the value of the digital I/O pins. Note that the ADS1248 uses all eight IODAT bits, while the ADS1247 uses only bits 3:0.

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SPI COMMANDS

SPI COMMAND DEFINITIONS

The commands shown in Table 25 control the operation of the ADS1246/7/8. Some of the commands are stand-alone commands (for example, RESET), whereas others require additional bytes (for example, WREG requires command, count, and the data bytes).

Operands:

n = number of registers to be read or written (number of bytes – 1)

r = register (0 to 15)

x = don't care

Table 25. SPI Commands

COMMAND TYPE	COMMAND	DESCRIPTION	1st COMMAND BYTE	2nd COMMAND BYTE
System Control	WAKEUP	Exit sleep mode	0000 000x (00h, 01h)	
	SLEEP	Enter sleep mode	0000 001x (02h, 03h)	
	SYNC	Synchronize the A/D conversion	0000 010x (04h, 05h)	0000-010x (04,05h)
	RESET	Reset to power-up values	0000 011x (06h, 07h)	
	NOP	No operation	1111 1111 (FFh)	
Data Read	RDATA	Read data once	0001 001x (12h, 13h)	
	RDATAC	Read data continuously	0001 010x (14h, 15h)	
	SDATAC	Stop reading data continuously	0001 011x (16h, 17h)	
Read Register	RREG	Read from register *rrrr*	0010 rrrr (2xh)	0000_nnnn
Write Register	WREG	Write to register *rrrr*	0100 rrrr (4xh)	0000_nnnn
Calibration	SYSOCAL	System offset calibration	0110 0000 (60h)	
	SYSGCAL	System gain calibration	0110 0001 (61h)	
	SELFOCAL	Self offset calibration	0110 0010 (62h)	

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SYSTEM CONTROL COMMANDS

WAKEUP—Wake up from sleep mode that is set by the SLEEP command.

Use this command to awaken the device from sleep mode. After execution of the WAKEUP command, the device wakes up on the rising edge of the eighth SCLK.

SLEEP—Set the device to sleep mode; can only be awakened by the WAKEUP command.

This command places the part into a sleep (power-saving) mode. When the SLEEP command is issued, the device completes the current conversion and then goes into sleep mode. Note that this command does not automatically power-down the internal voltage reference; see the VREFCON bits in the MUX1 register for each device for further details.

To exit sleep mode, issue the WAKEUP command. Single conversions can be performed by issuing a WAKEUP command followed by a SLEEP command.

Both WAKEUP and SLEEP are the software command equivalents of using the START pin to control the device.

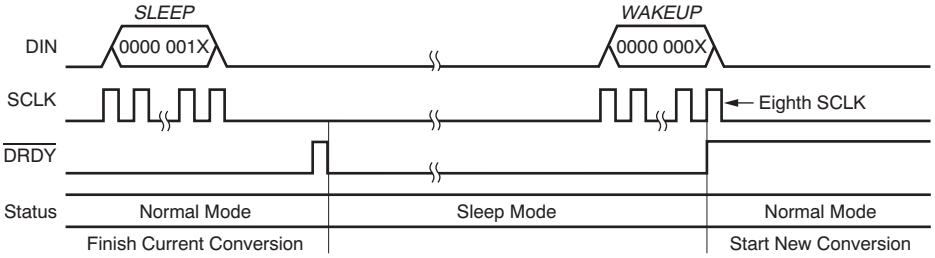

Figure 53. SLEEP and WAKEUP Commands Operation

SYNC—Synchronize $\overline{\text{DRDY}}$.

This command resets the ADC digital filter and starts a new conversion. The $\overline{\text{DRDY}}$ pin from multiple devices connected to the same SPI bus can be synchronized by issuing a SYNC command to all of devices simultaneously.

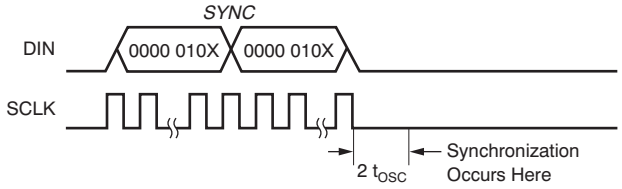

Figure 54. SYNC Command Operation

RESET—Reset the device to power-up state.

This command restores the registers to the respective power-up values. This command also resets the digital filter. RESET is the command equivalent of using the $\overline{\text{RESET}}$ pin to reset the device. However, the RESET command does not reset the SPI interface. If the RESET command is issued when the SPI interface is in the wrong state, the device does not reset. The $\overline{\text{CS}}$ pin can be used to reset SPI interface first, and then a RESET command can be issued to reset the device. The RESET command holds the registers and the decimation filter in a reset state for 0.6ms when the system clock frequency is 4.096MHz, similar to the hardware reset. Therefore, SPI communication can be only be started 0.6ms after the RESET command is issued, as shown in Figure 55.

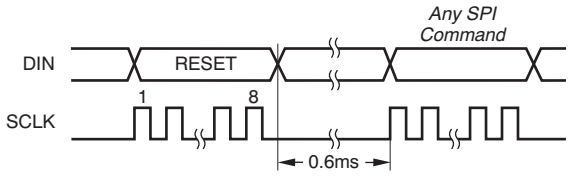

Figure 55. SPI Communication After an SPI Reset

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DATA RETRIEVAL COMMANDS

RDATAC—Read data continuously.

The RDATAC command enables the automatic loading of a new conversion result into the output data register. In this mode, the conversion result can be received once from the device after the $\overline{\text{DRDY}}$ signal goes low by sending 24 SCLKs. It is not necessary to read back all the bits, as long as the number of bits read out is a multiple of eight. The RDATAC command must be issued after $\overline{\text{DRDY}}$ goes low, and the command takes effect on the next $\overline{\text{DRDY}}$.

Be sure to complete data retrieval (conversion result or register read-back) before $\overline{\text{DRDY}}$ goes low, or the resulting data will be corrupt. Successful register read operations in RDATAC mode require the knowledge of when the next $\overline{\text{DRDY}}$ falling edge occurs.

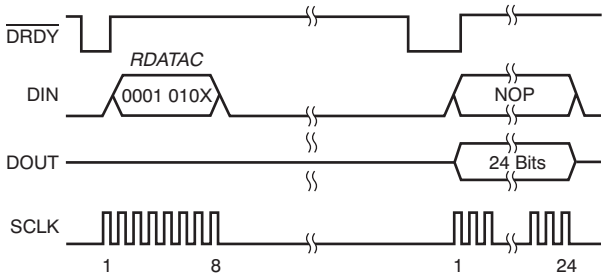

Figure 56. Read Data Continuously

SDATAC—Stop reading data continuously.

The SDATAC command terminates the RDATAC mode. Afterwards, the conversion result is not automatically loaded into the output shift register when $\overline{\text{DRDY}}$ goes low, and register read operations can be performed without interruption from new conversion results being loaded into the output shift register. Use the RDATA command to retrieve conversion data. The SDATAC command takes effect after the next $\overline{\text{DRDY}}$.

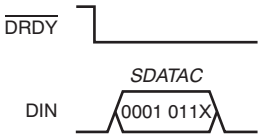

Figure 57. Stop Reading Data Continuously

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RDATA—Read data once.

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result can be read out by sending 24 SCLKs, as shown in Figure 58. This command also works in RDATAC mode.

When performing multiple reads of the conversion result, the RDATA command can be sent when the last eight bits of the conversion result are being shifted out during the course of the first read operation by taking advantage of the duplex communication nature of the SPI interface, as shown in Figure 59.

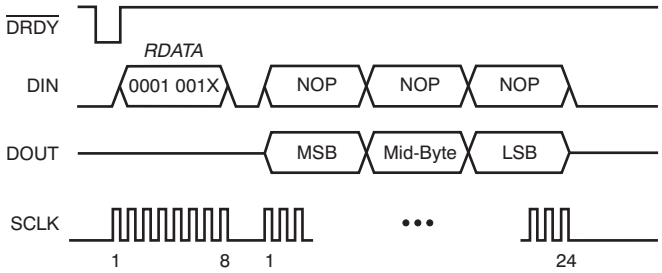

Figure 58. Read Data Once

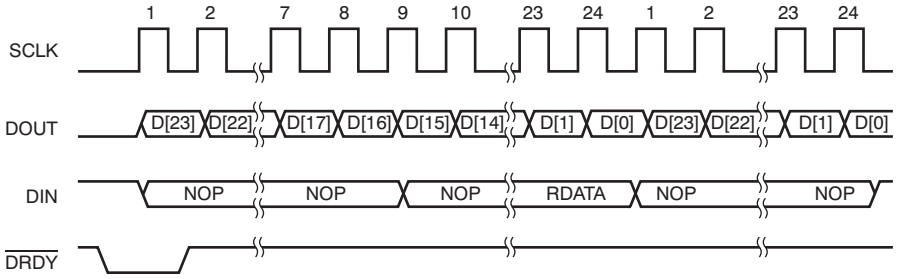

Figure 59. Using RDATA in Full-Duplex Mode

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USER REGISTER READ AND WRITE COMMANDS

RREG—Read from registers.

This command outputs the data from up to 16 registers, starting with the register address specified as part of the instruction. The number of registers read is one plus the second byte. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

First Command Byte: 0010 *rrrr*, where *rrrr* is the address of the first register to read.

Second Command Byte: 0000 *nnnn*, where *nnnn* is the number of bytes to read –1.

It is not possible to use the full-duplex nature of the SPI interface when reading out the register data. For example, a SYNC command cannot be issued when reading out the VBIAS and MUX1 data, as shown in Figure 60. Any command sent during the readout of the register data is ignored. Thus, it is advisable to send NOP through the DIN when reading out the register data.

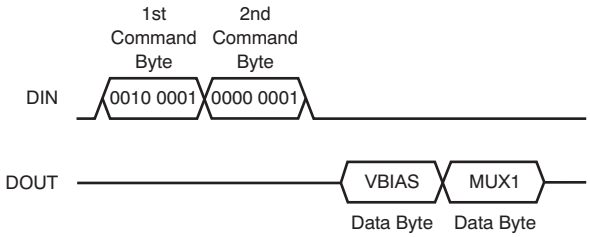

Figure 60. Read from Register

WREG—Write to registers.

This command writes to the registers, starting with the register specified as part of the instruction. The number of registers that are written is one plus the value of the second byte.

First Command Byte: 0100 *rrrr*, where *rrrr* is the address of the first register to be written.

Second Command Byte: 0000 *nnnn*, where *nnnn* is the number of bytes to be written – 1.

Data Byte(s): data to be written to the registers.

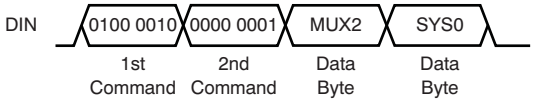

Figure 61. Write to Register

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CALIBRATION COMMANDS

The ADS1246/7/8 provide system and offset calibration commands and a system gain calibration command.

SYSOCAL—Offset system calibration.

This command initiates a system offset calibration. For a system offset calibration, the input should be externally set to zero. The OFC register is updated when this operation completes.

SYSGCAL—System gain calibration.

This command initiates the system gain calibration. For a system gain calibration, the input should be set to full-scale. The FSC register is updated after this operation.

SELFOCAL—Self offset calibration.

This command initiates a self-calibration for offset. The device internally shorts the inputs and performs the calibration. The OFC register is updated after this operation.

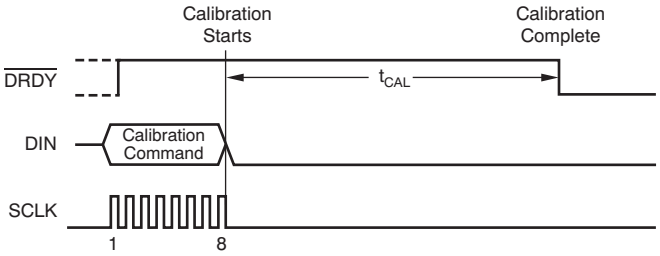

Figure 62. Calibration Command

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APPLICATION INFORMATION

SPI COMMUNICATION EXAMPLES

This section contains several examples of SPI communication with the ADS1246/7/8, including the power-up sequence.

Channel Multiplexing Example

This first example applies only to the ADS1247 and ADS1248. It explains a method to use the device with two sensors connected to two different analog channels. Figure 63 shows the sequence of SPI operations performed on the device. After power-up, the initial ADC setup cannot be carried out before the power-on reset sequence completes internally after t_{PWOR}. In this example, one of the sensors is connected to channels AIN0 and AIN1 and the other sensor is connected to channels AIN2 and AIN3. The ADC is operated at a data rate of 2kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the negative terminal of both sensors (that is, channels AIN1 and AIN3). All these settings can be changed by performing a block write operation on the first four registers of the device. After the DRDY pin goes low, the conversion result can be immediately retrieved by sending in 24 SPI clock pulses because the device defaults to RDATAC mode. As the conversion result is being retrieved, the active input channels can be switched to AIN2 and AIN3 by writing into the MUX0 register in a full-duplex manner, as shown in Figure 63. The write operation is completed in the same 24 SPI clock pulses. The time from the write operation into the MUX0 register to the next DRDY low transition is shown in Figure 63 and is 0.513ms in this case. After DRDY goes low, the conversion result can be retrieved and the active channel can be switched as before.

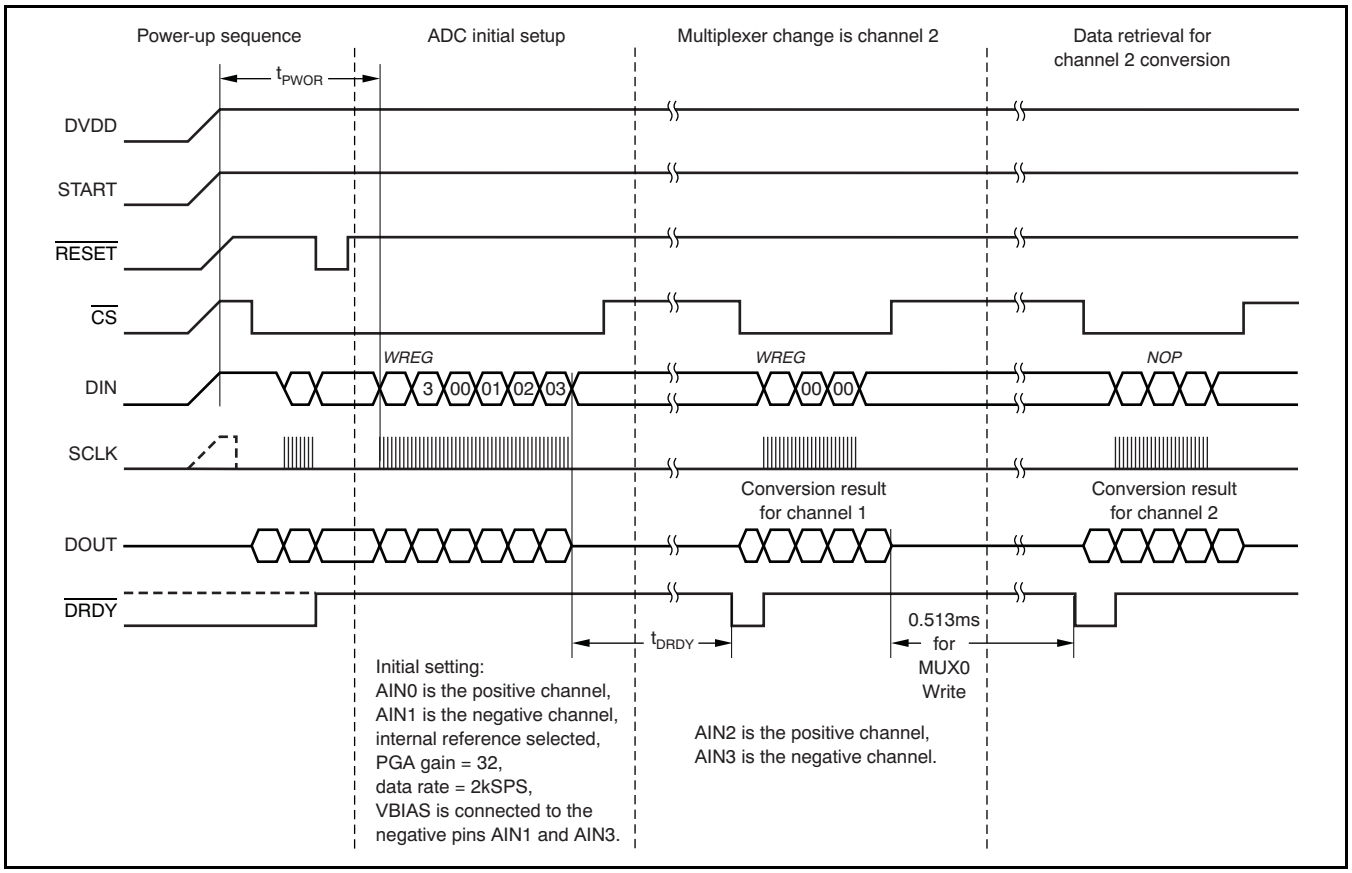

Figure 63. SPI Communication Sequence for Channel Multiplexing

Sleep Mode Example

This second example deals with performing one conversion after power-up and then entering into the power-saving sleep mode. In this example, a sensor is connected to input channels AIN0 and AIN1. After powering up the device with the power-up sequence shown in Figure 64, the commands to setup the ADC are issued after t_{PWOR}. The ADC operates at a data rate of 2kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the negative terminal of both the sensors (that is, channel AIN1). All these settings can be changed by performing a block write operation on the first four registers of the device. After performing the block write operation, the START pin can be taken low. The device enters the power-saving sleep mode as soon as DRDY goes low 0.575ms after writing into the SYS0 register. The conversion result can be retrieved even after the device enters sleep mode by sending 24 SPI clock pulses.

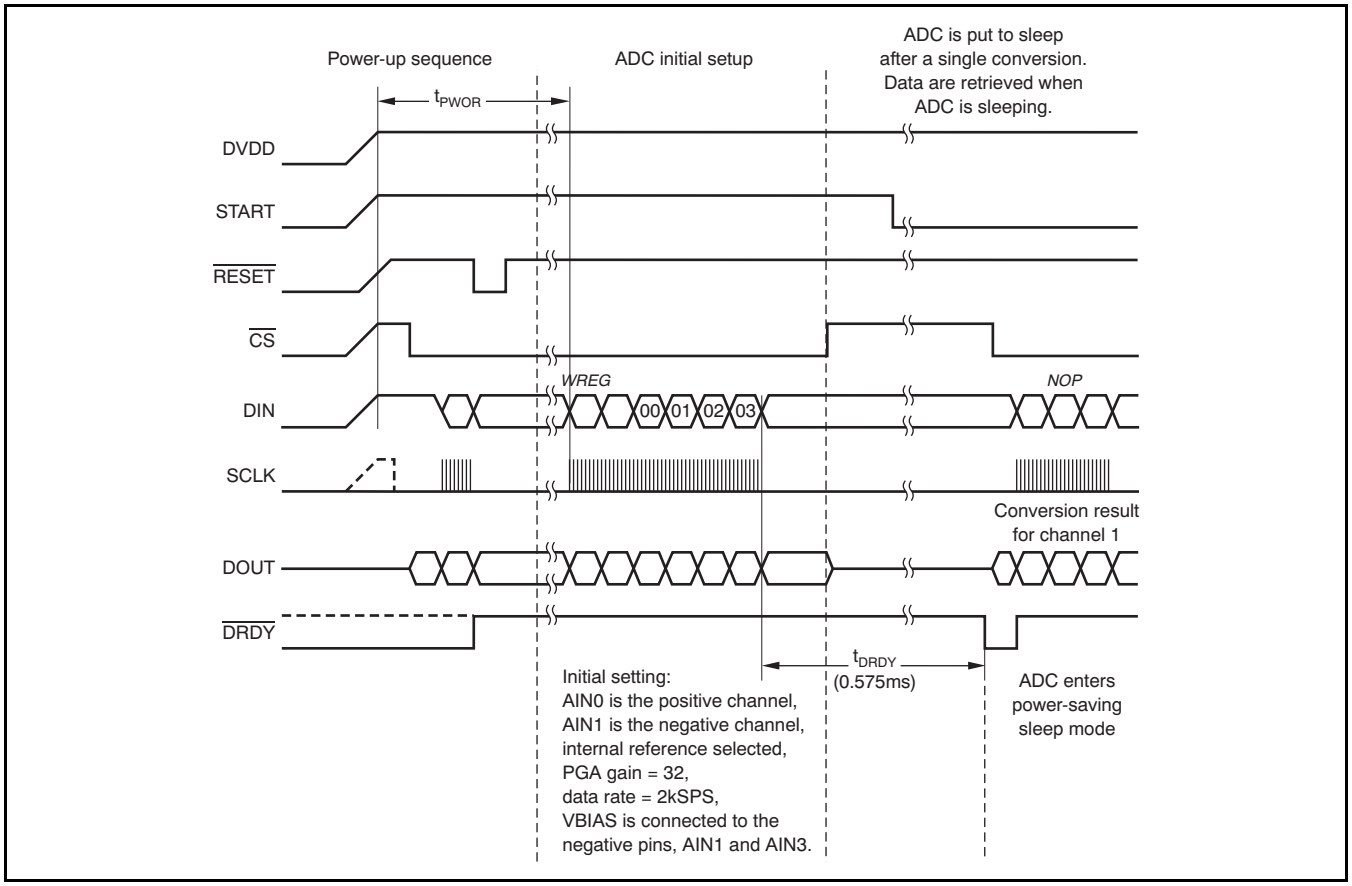

Figure 64. SPI Communication Sequence for Entering Sleep Mode After a Conversion

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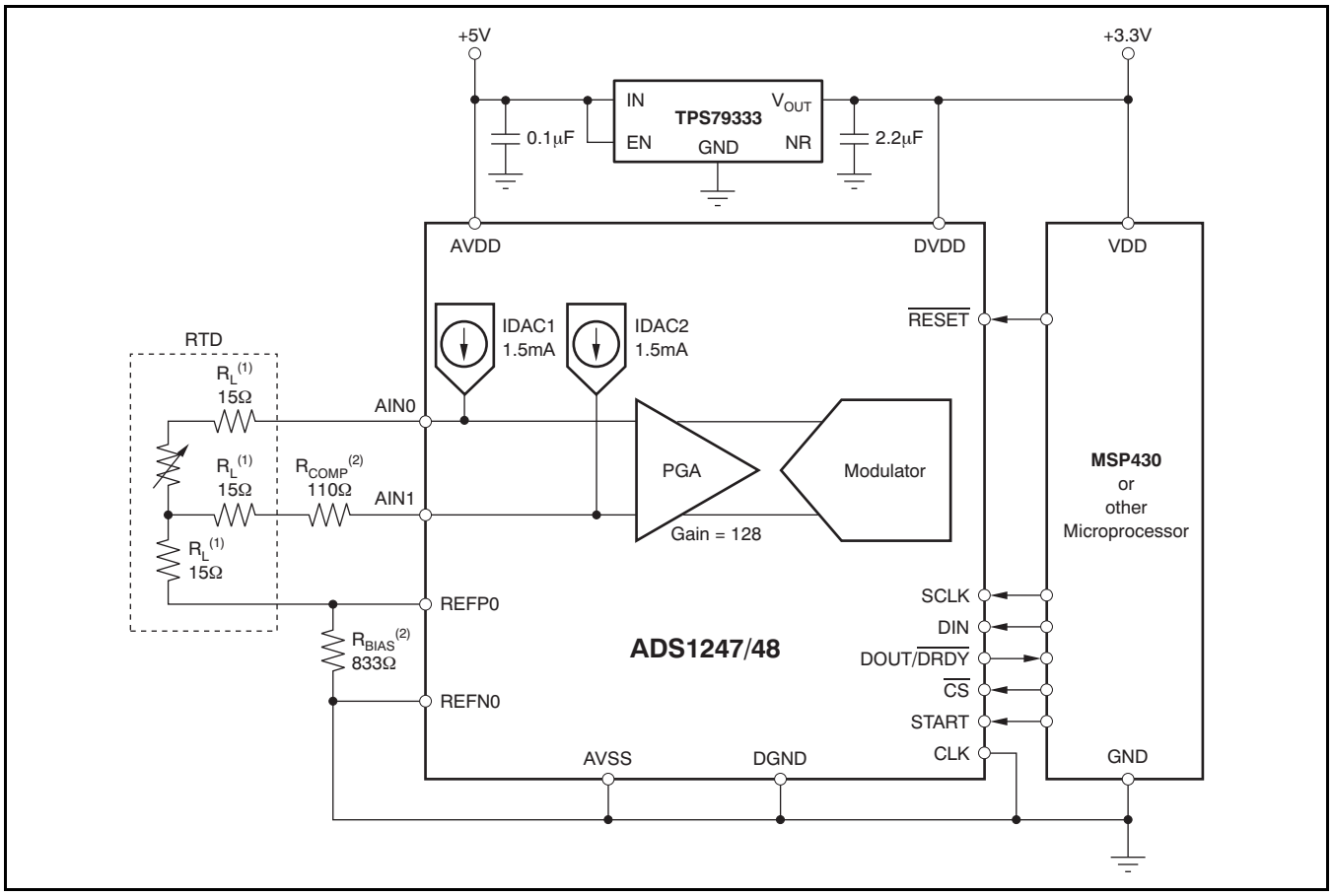
Hardware-Compensated, Three-Wire RTD Measurement Example

Figure 65 is an application circuit to measure temperatures in the range of 0°C to +50°C using a PT-100 RTD and the ADS1247 or ADS1248 in a three-wire, hardware-compensated topology. The two onboard matched current DACs of the ADS1247/48 are ideally suited for implementing the three-wire RTD topology. This circuit uses a ratiometric approach, where the reference is derived from the IDAC currents in order to achieve excellent noise performance. The resistance of the PT-100 changes from 100Ω at 0°C to 119.6Ω at +50°C. The compensating resistor (R_{COMP}) has been chosen to be equal to the resistance of the PT-100 sensor at +25°C (approximately 110Ω). The IDAC current is set to 1.5mA. This setting results in a differential input swing of ±14.7mV at the inputs of the ADC. The PGA gain is set to 128. The full-scale input for the ADC is ±19.53mV. Fixing R_{BIAS} at 833Ω fixes the reference at 2.5V and the input common-mode at approximately 2.7V, ensuring that the voltage at AIN0 is far away from the IDAC compliance voltage.

The maximum number of noise-free output codes for this circuit in the 0°C to +50°C temperature range is $(2^{ENOB})(14.7mV)/19.53mV$.



(1) RTD line resistances.

(2) R_{BIAS} and R_{COMP} should be as close to the ADC as possible.

Figure 65. Three-Wire RTD Application with Hardware Compensation

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2009) to Revision C **Page**

- Changed 13th, 16th, and 17th Features bullets 1
- Updated front page graphic 1
- Changed Electrical Characteristics conditions 3
- Changed conditions for INL, *System Performance* parameter of Electrical Characteristics 3
- Changed conditions of System Performance, *Gain error* parameter of Electrical Characteristics 3
- Deleted conditions of System Performance, *Gain drift* parameter of Electrical Characteristics 3
- Deleted *Quiescent current* parameter from On-Chip Voltage Reference of Electrical Characteristics 3
- Changed Electrical Characteristics conditions 4
- Changed typical specifications for *System Monitors* section of Electrical Characteristics 4
- Changed minimum specification for DVDD and AVDD, *Power Supply* parameters in the Electrical Characteristics 4
- Changed normal mode, DVDD = 5V conditions of Power Supply, *DVDD current* parameter of Electrical Characteristics 4
- Changed converting conditions of Power Supply, *AVDD current* parameter of Electrical Characteristics 4
- Added additional current condition to Power Supply, *AVDD current* parameter of Electrical Characteristics 4
- Changed conditions of Power Supply, *Power dissipation* parameter of Electrical Characteristics 4
- Changed power dissipation specification for AVDD = DVDD = 3.3V 4
- Changed name of FUNCTION column in ADS1248 Pin Descriptions table 6
- Changed name of FUNCTION column in ADS1247 Pin Descriptions table 7
- Changed name of FUNCTION column in ADS1246 Pin Descriptions table 8
- Changed footnote 2 of Table 1 9
- Added body text to *Noise Performance* section 11
- Changed Table 5 through Table 8 12
- Added Table 9 and Table 10 14
- Changed conditions for Typical Characteristics: 5V 15
- Changed conditions for Typical Characteristics: 5V 16
- Updated Figure 15 16
- Changed conditions for Typical Characteristics: 5V 17
- Updated Figure 18 17
- Updated Figure 19 17
- Changed conditions for Typical Characteristics: 5V 18
- Changed Figure 24 18
- Changed *Overview* section 19
- Updated Figure 29 19
- Updated Figure 31 20
- Changed *Settling Time for Channel Multiplexing* section 21
- Changed *Digital Filter* section 22
- Changed the last sentence of the *Clock Source* section 24
- Changed devices discussed in the *System Monitor* section 26
- Deleted the *Power-Up Sequence* section 26
- Changed third sentence of first paragraph if *Ambient Temperature Monitor* section 26
- Changed *Calibration* section 27
- Changed the *ADC Conversion Control* title of *ADC Control* 28
- Changed *Digital Filter Reset Operation* section 30
- Moved *Data Format* location 31
- Changed title of *Digital Interface* section 31
- Updated Figure 49 32
- Updated Figure 50 32

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- Updated Figure 51 33
- Updated ADS1246 FSC0 Register, added footnote 1 37
- Updated ADS1246 FSC1 Register, added footnote 1 37
- Updated ADS1246 FSC2 Register, added footnote 1 37
- Defined device compatibility for *100* setting of MUXCAL2:0 of the MUX1 control register 40
- Updated ADS1247/ADS1248 FSC0 Register, added footnote 1 42
- Updated ADS1247/ADS1248 FSC1 Register, added footnote 1 42
- Updated ADS1247/ADS1248 FSC2 Register, added footnote 1 42
- Defined device compatibility for *0100* setting of I1DIR3:0 of the IDAC1 control register 43
- Deleted *PO INIT* command from Table 25 45
- Deleted *PO INIT* command from *System Control Commands* section 46
- Updated *Calibration Commands* section 50

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS1246IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1246IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ADS1247IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1247IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1248IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1248IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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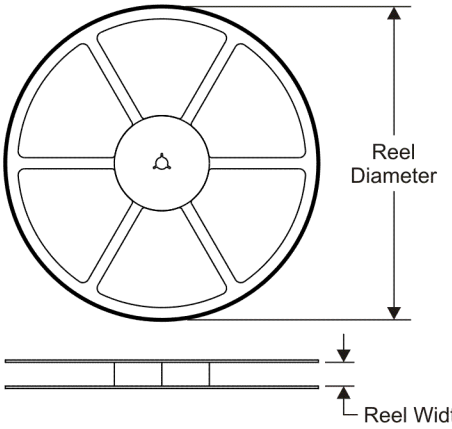
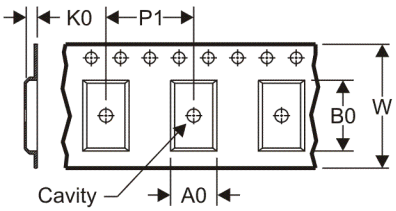
TAPE AND REEL INFORMATION

REEL DIMENSIONS

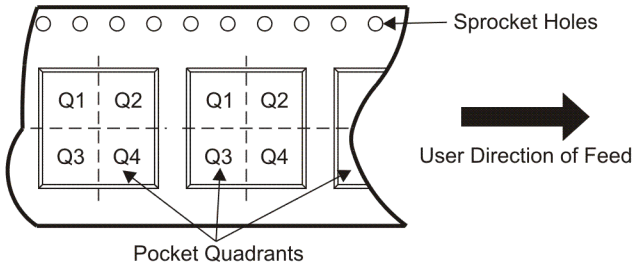


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1246IPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
ADS1247IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
ADS1248IPWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1

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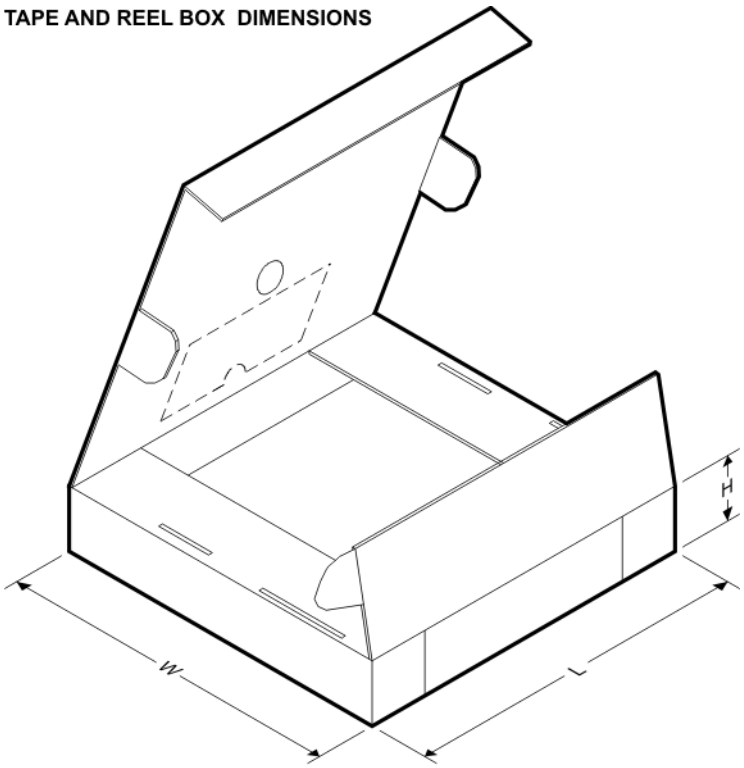
PACKAGE MATERIALS INFORMATION

23-Jun-2009

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1246IPWR	TSSOP	PW	16	2000	346.0	346.0	29.0
ADS1247IPWR	TSSOP	PW	20	2000	346.0	346.0	33.0
ADS1248IPWR	TSSOP	PW	28	2000	346.0	346.0	33.0

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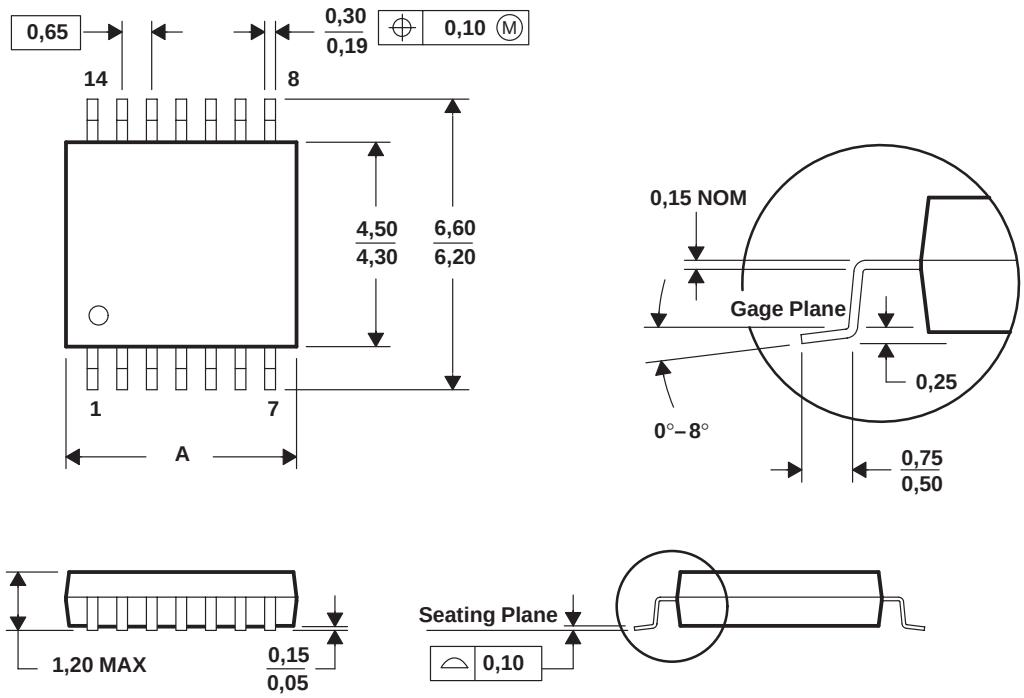
PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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