



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

SM7511

**3W STEREO AUDIO POWER AMPLIFIER
WITH ADVANCED DC VOLUME CONTROL**

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3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

GENERAL DESCRIPTION

The SM7511 is a stereo audio power amplifier that drives 3 W/channel of continuous RMS power into a 3- Ω load. Advanced dc volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a dc voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a dc voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a dc voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

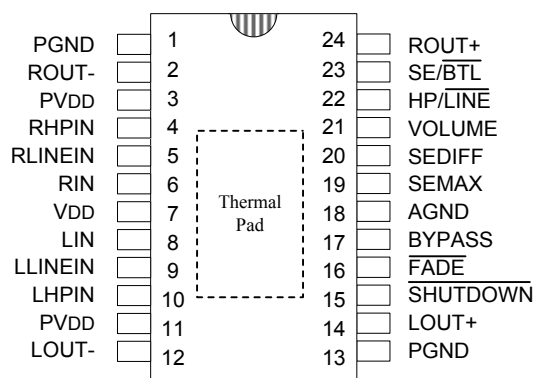
FEATURES

- * Advanced DC Volume Control With 2-dB Steps From -40 dB to 20 dB
 - Fade Mode
 - Maximum Volume Setting for SE Mode
 - Adjustable SE Volume control Referenced to BTL Volume Control
- * 3 W Into 3 - Ω Speakers
- * Stereo Input MUX
- * Differential Inputs

APPLICATIONS

- * Notebook PC
- * LCD Monitors
- * Pocket PC
- * Portable DVD
- * Mini speaker

PIN ASSIGNMENTS (TOP VIEW)



SM7511 24PIN

**3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL****PIN DESCRIPTIONS**

No.	Pin Name	I / O	Function
1.13	PGND	-	Power ground
2	ROUT-	O	Right channel negative audio output
3.11	PVDD	-	Supply voltage terminal for power stage
4	RHPIN	I	Right channel headphone input,selected when HP/ $\overline{\text{LINE}}$ is held high
5	RLINEIN	I	Right channel line input, selected when HP/ $\overline{\text{LINE}}$ is held low
6	RIN	I	Common right channel input for fully defferential input. AC ground for single-ended inputs.
7	VDD	-	Supply voltage terminal
8	LIN	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
9	LLINEIN	I	Left channel line input, selected when HP/ $\overline{\text{LINE}}$ is held low
10	LHPIN	I	Left channel headphone input,selected when HP/ $\overline{\text{LINE}}$ is held high.
12	LOUT-	O	Left channel negative audio output
14	LOUT+	O	Left channel positive audio output.
15	$\overline{\text{SHUTDOWN}}$	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal.
16	$\overline{\text{FADE}}$	I	Places the amplifier in fade mode if a logic low is placed on this termnal; normal operation if a logic high is placed on this terminal.
17	BYPASS	I	Tap to voltage divider for internal midsupply bias generator used for analog reference.
18	AGND	-	Analog power supply ground
19	SEMAX	I	Sets the maximum volume for single ended operation.DC voltage range is 0 to VDD
20	SEDIFF	I	Sets the difference between BTL volume and SE volme. DC voltage range is 0 to VDD
21	VOLUME	I	Terminal for dc volume control. DC voltage range is 0 to VDD
22	HP/ $\overline{\text{LINE}}$	I	Input MUX control. When logic high,RHPIN and LHPIN inputs are selected. When logic low,RLINEIN and LLINEIN inputs are selected
23	SE/ $\overline{\text{BTL}}$	I	Output MUX control. When this terminal is high,SE outputs are selected.When this terminal is low, BTL outputs are selected
24	ROUT+	O	Right channel positive audio output.



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MAXIMUM RATINGS (Ta = 40~85°C)

over operating free-air temperature range (unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Supply Voltage, VDD, PVDD	VSS	-0.3 ~ 6	V
Input Voltage	VI	- 0.3 ~ VDD +0.3	V
Continuous total power dissipation	-	See Dissipation Rating Table	-
Operating free-air temperature range	TA	- 40 ~ 85	°C
Operating junction temperature range	TJ	- 40 ~ 150	°C
Storage temperature range	Tstg	- 65 ~ 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	-	260	°C

(Note) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	TA≤25°C Power Rating	Derating Factor Above TA=25°C	TA=70°C Power Rating	TA=85°C Power Rating
SOP /SSOP	2.7mW	21.8 mW/°C	1.7W	1.4W

RECOMMENDED OPERATING CONDITION

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage, VDD, PVDD	VSS	--	4.0		5.5	V
High-level input voltage	VIH	SE/BTL, HP/LINE, FADE	0.8 VDD			V
		SHUTDOWN	2.0			
Low-level input voltage	VIL	SE/BTL, HP/LINE, FADE			0.6 VDD	V
		SHUTDOWN			0.85	
Operating free-air temperature	TA	--	-40		85	°C


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ELECTRICAL CHARACTERISTICS ($V_{DD} = PV_{DD} = 5.5V$, $T_a = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Output offset voltage (measured differentially)	$ V_{OO} $	$V_{DD}=5.5V$, Gain=20dB, SE/ $\overline{BTL}$ =0V			60	mV
Power supply rejection ratio	PSRR	$V_{DD}=PV_{DD}=4.0V$ to 5.5V	-42	-70		dB
High-level input current(SE/ $\overline{BTL}$, $\overline{FADE}$ HP/LINE,SHUTDOWN,SEMAX)	$ I_{IH} $	$V_{DD}=PV_{DD}=5.5V$, $V_I=V_{DD}=PV_{DD}$			1	μA
High-level input current (SEDIFF,VOLUME)	$ I_{IH} $				150	μA
Low-level input current(SE/ $\overline{BTL}$, $\overline{FADE}$ HP/LINE,SHUTDOWN,SEMAX)	$ I_{IL} $	$V_{DD}=PV_{DD}=5.5V$, $V_I=0V$			1	μA
Supply current, no load	I_{DD}	$V_{DD}=PV_{DD}=5.5V$, SE/ $\overline{BTL}$ =0V, SHUTDOWN=2V	5.5	8.0	10	mA
		$V_{DD}=PV_{DD}=5.5V$, SE/ $\overline{BTL}$ =5.5V, SHUTDOWN=2V	3.0	5.0	6.0	
Supply current,max power into a 3 Ω load	I_{DD}	$V_{DD}=5V=PV_{DD}$, SE/ $\overline{BTL}$ =0V, SHUTDOWN=2V, $R_L=3\Omega$, $P_o=2W$, Stereo		1.5		ARMS
Supply current,shutdown mode	$I_{DD}(SD)$	SHUTDOWN=0.0V		1	20	μA

OPERATING CHARACTERISTICS

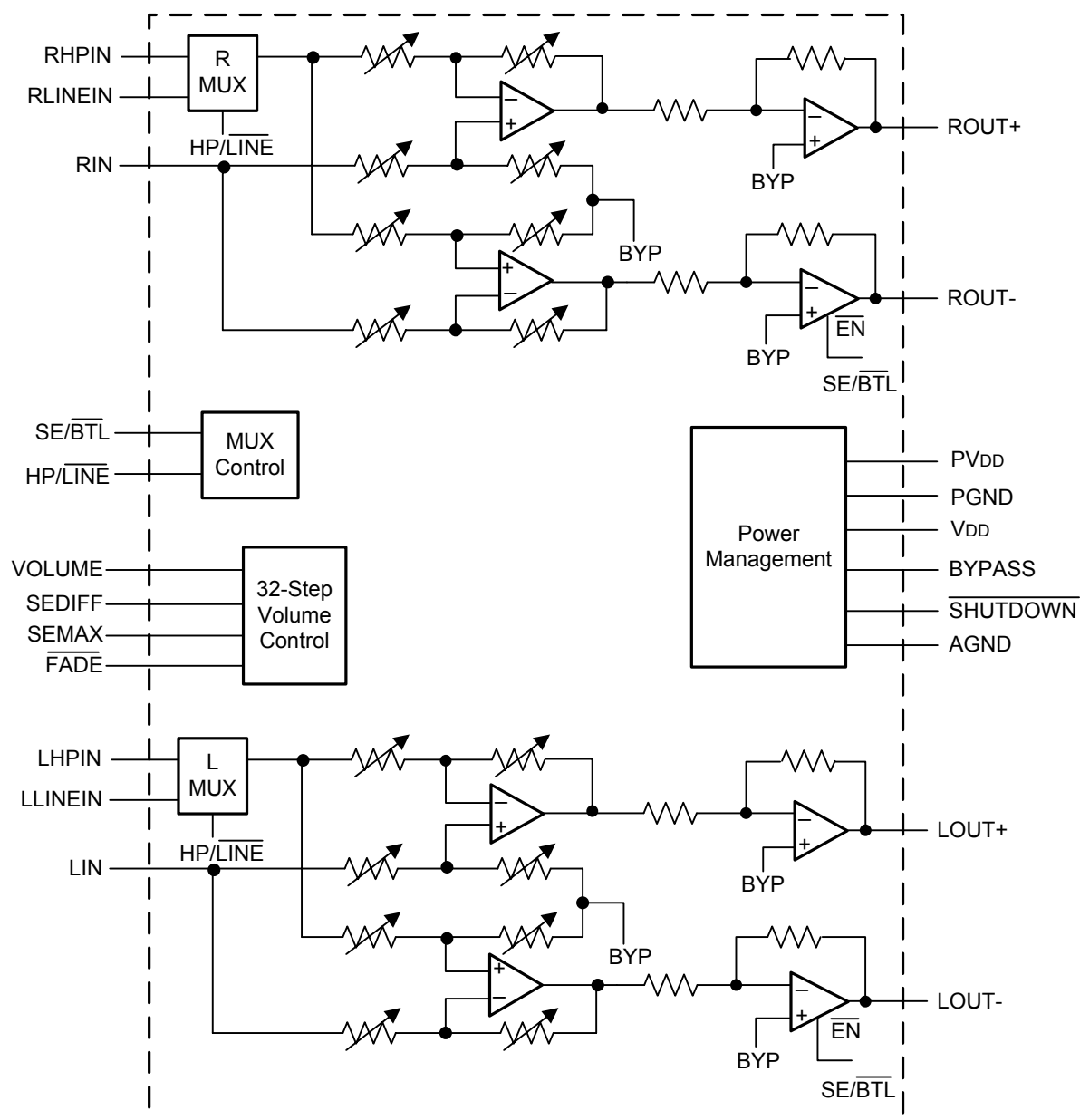
 ($V_{DD} = PV_{DD} = 5V$, $R_L = 3\Omega$, Gain = 6dB, $T_a = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Power	P_o	THD=1%, f=1 kHz		2		W
		THD=10%, f=1 kHz, $V_{DD}=5.5V$		3		
Total harmonic distortion+noise	THD+N	$P_o = 1W$, $R_L=8\Omega$, f=20Hz to 20kHz		<0.6		%
High-level output voltage	V_{OH}	$R_L=8\Omega$, Measured between output and V_{DD}			500	mV
Low-level output voltage	V_{OL}	$R_L=8\Omega$, Measured between output and GND			400	mV
Bypass voltage(Nominally $V_{DD}/2$)	$V_{(BYPASS)}$	Measured at pin 17, No load, $V_{DD}=5.5V$	2.65	2.75	2.85	V
Maximum output power bandwidth	BOM	THD=5%		>20		kHz
Supply ripple rejection ratio		f=1 kHz, Gain = 0 dB, $C_{(BYP)} = 1.0\mu F$	$\overline{BTL}$	-63		dB
			SE	-57		
Noise output voltage		f= 20 Hz to 20 kHz, Gain=0 dB, $C_{(BYP)}= 1.0\mu F$	$\overline{BTL}$	40		μV_{RMS}



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FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor wipers are adjusted with 32 step volume control.

**3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL****Table 1. DC Volume Control (BTL Mode, $V_{DD}=5V$)**

VOLUME (PIN 21)		GAIN OF AMPLIFIER (Typ.)
FROM (V)	TO (V)	
0.00	0.23	-85
0.31	0.34	-40
0.42	0.46	-38
0.54	0.56	-36
0.65	0.67	-34
0.76	0.79	-32
0.87	0.90	-30
0.98	1.01	-28
1.10	1.12	-26
1.21	1.24	-24
1.32	1.35	-22
1.43	1.46	-20
1.54	1.57	-18
1.66	1.68	-16
1.77	1.79	-14
1.88	1.91	-12
1.99	2.02	-10
2.10	2.13	-8
2.21	2.24	-6
2.33	2.35	-4
2.44	2.47	-2
2.55	2.57	0
2.67	2.70	2
2.77	2.80	4
2.89	2.92	6
3.00	3.03	8
3.11	3.14	10
3.22	3.26	12
3.33	3.37	14
3.44	3.48	16
3.55	3.60	18
3.67	5.00	20

**3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL****Table 2. DC Volume Control (SE Mode, $V_{DD}=5V$)**

SE_VOLUME=VOLUME-SEDIFF or SEMAX		GAIN OF AMPLIFIER (Typ.)
FROM (V)	TO (V)	
0.00	0.23	-85
0.31	0.34	-46
0.42	0.46	-44
0.54	0.56	-42
0.65	0.67	-40
0.76	0.79	-38
0.87	0.90	-36
0.98	1.01	-34
1.10	1.12	-32
1.21	1.24	-30
1.32	1.35	-28
1.43	1.46	-26
1.54	1.57	-24
1.66	1.68	-22
1.77	1.79	-20
1.88	1.91	-18
1.99	2.02	-16
2.10	2.13	-14
2.21	2.24	-12
2.33	2.35	-10
2.44	2.47	-8
2.55	2.57	-6
2.67	2.70	-4
2.77	2.80	-2
2.89	2.92	0
3.00	3.03	2
3.11	3.14	4
3.22	3.26	6
3.33	3.37	8
3.44	3.48	10
3.55	3.60	12
3.67	5.00	14

APPLICATION INFORMATION

The schematic diagram illustrates the AD1875 audio codec IC, a 28-pin CMOS device, and its external connections for a stereo audio system. The IC is shown in a top-down view with pins numbered 1 through 28.

Internal IC Structure:

- Power and Ground Pins:**
 - PGND (1, 13):** Power Ground.
 - PVDD (3, 11):** Positive Supply Voltage.
 - AGND (18):** Analog Ground.
- Audio Input/Output Pins:**
 - ROUT+ (24), ROUT- (2):** Right Channel Output.
 - LOUT+ (14), LOUT- (12):** Left Channel Output.
 - RHPIN (4), RLINEIN (5):** Right Channel Input.
 - RIN (6), LLINEIN (9):** Line Input.
 - LHPIN (10):** Left Channel Input.
- Control and Status Pins:**
 - SE/BTL (23):** Selects between Single-Ended and Bridge-Tied Load mode.
 - HP/LINE (22):** Headphone/Line output mode select.
 - VOLUME (21), SEDIFF (20), SEMAX (19):** Volume control pins.
 - AGND (18):** Analog Ground.
 - BYPASS (17):** Bypasses the volume control.
 - FADE (16):** Fade control.
 - SHUTDOWN (15):** Shutdown control.

External Components and Connections:

- Power Supply:**
 - VDD:** Connected to pins 7 and 11. A decoupling capacitor C_s is connected between VDD and ground.
 - PGND:** Connected to pins 1 and 13.
- Audio Sources:**
 - Right HP Audio Source:** Connected to pin 4 (RHPIN) through a coupling capacitor C_i .
 - Right Line Audio Source:** Connected to pin 5 (RLINEIN) through a coupling capacitor C_i .
 - Left Line Audio Source:** Connected to pin 9 (LLINEIN) through a coupling capacitor C_i .
 - Left HP Audio Source:** Connected to pin 10 (LHPIN) through a coupling capacitor C_i .
- Outputs and Load:**
 - Right Speaker:** Connected to pin 24 (ROUT+). A 100kΩ resistor is connected between pin 24 and VDD. A coupling capacitor C_c is connected between pin 24 and the speaker.
 - Left Speaker:** Connected to pin 14 (LOUT+). A coupling capacitor C_c is connected between pin 14 and the speaker.
 - Headphones:** Connected to pins 21 (VOLUME), 20 (SEDIFF), and 19 (SEMAX). A 1kΩ resistor is connected between pin 21 and ground. A potentiometer (DC Voltage) is connected between pins 20 and 19.
- Control and Status:**
 - BYPASS (17):** Connected to ground through a capacitor $C_{(BYP)}$.
 - FADE (16):** Connected to ground.
 - SHUTDOWN (15):** Connected to ground.
 - System Control:** Connected to pin 15 (SHUTDOWN).

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APPLICATION INFORMATION (continued)

The figure is schematic diagrams of typical notebook computer application circuits.

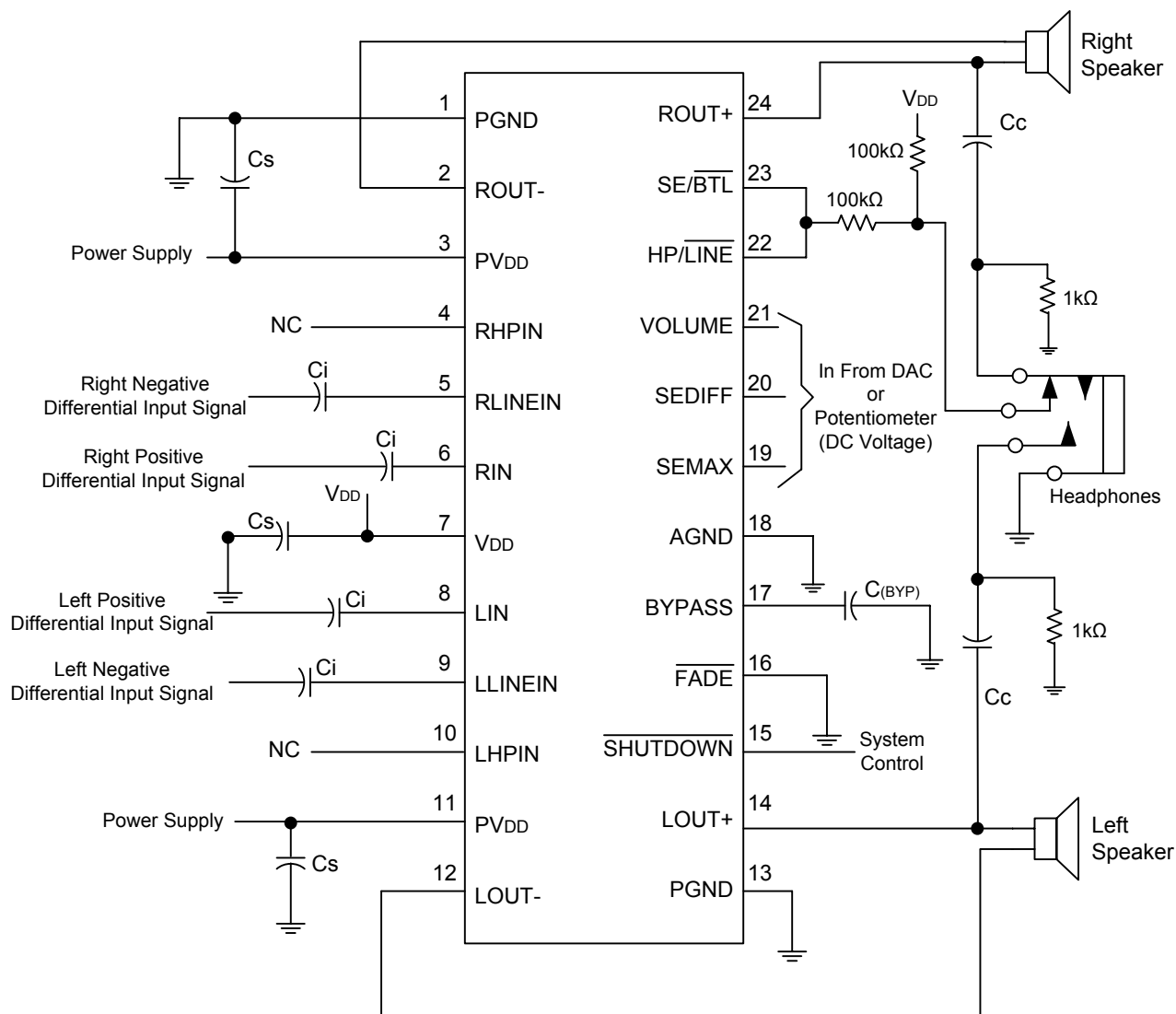


Figure 2. SM7511 Application Circuit Using Differential Inputs



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SE/BTL OPERATION

The ability of the SM7511 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the SM7511, two separate amplifiers drive OUT+ and OUT-. The SE/BTL input controls the operation of the follower amplifier that drives LOUT- and ROUT-. When SE/BTL is held low, the amplifier is on and the SM7511 is in the BTL mode. When SE/BTL is held high, the OUT- amplifiers are in a high output impedance state, which configures the SM7511 as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/BTL input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in Figure 3. The trip level for the SE/BTL input can be found in the recommended operating condition table.

APPLICATION INFORMATION (continued)

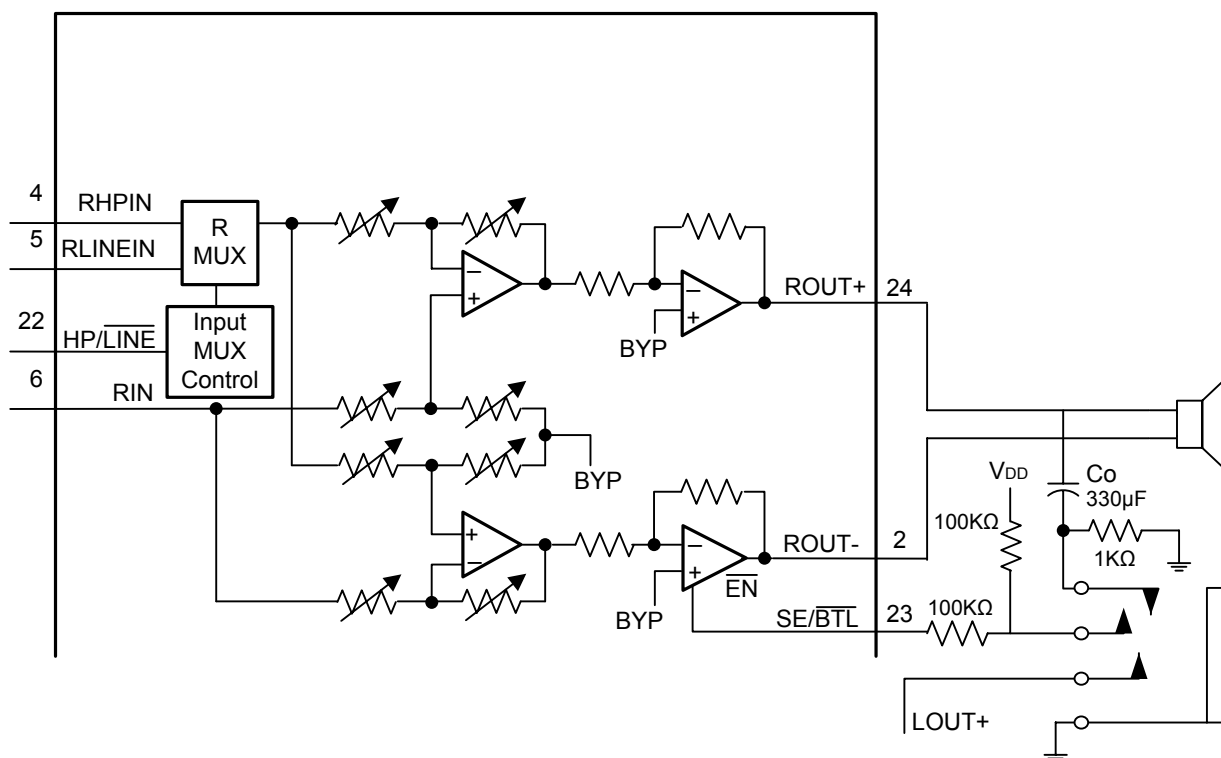


Figure 3. SM7511 Resistor Divider Network Circuit

Using a 1/8-in. (3.5mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100KΩ/1KΩ divider pulls the SE/BTL input low. When a plug is inserted, the 1KΩ resistor is disconnected and SE/BTL input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (Co) into the headphone jack.



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HP/LINE OPERATION

The HP/LINE input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure 3. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the HP/LINE control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/BTL pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/BTL control input to the HP/LINE input.

When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 3 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

Table 3. HP/LINE, SE/BTL, and Shutdown Functions

INPUTS ⁽¹⁾			AMPLIFIER STATE	
HP/LINE	SE/BTL	SHUTDOWN	INPUT	OUTPUT
X	X	Low	X	MUTE
Low	Low	High	LINE	BTL
Low	High	High	LINE	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Inputs should never be left unconnected

SHUTDOWN MODES

The SM7511 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held high during normal operation when the amplifier is in use. Pulling SHUTDOWN low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} = 20\mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable.

FADE OPERATION

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the FADE input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the *recommended operating conditions* table.

When a logic low is applied to the FADE pin and a logic low is then applied on the SHUTDOWN pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58Hz, this equates to 34 ms per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34 ms.



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After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of $V_{DD}/2$ to ground. This time is dependent on the value of the bypass capacitor. For a $0.47\mu\text{F}$ capacitor that is used in the application diagram in Figure 1, the time is approximately 500 ms. This time scales linearly with the value of bypass capacitor. For example, if a $1\mu\text{F}$ capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the $0.47\mu\text{F}$ capacitor, or 1 seconds. Figure 3 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{\text{SHUTDOWN}}$ pin and the $\overline{\text{FADE}}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$, the gain increases in 2 dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequences. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 4 below is a waveform captured at the output during the shutdown sequence when this part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{\text{FADE}}$ pin does not change the power-up sequence. Upon a power-up condition, the SM7511 begins in the lowest gain setting and steps up 2 dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF and SEMAX pins.

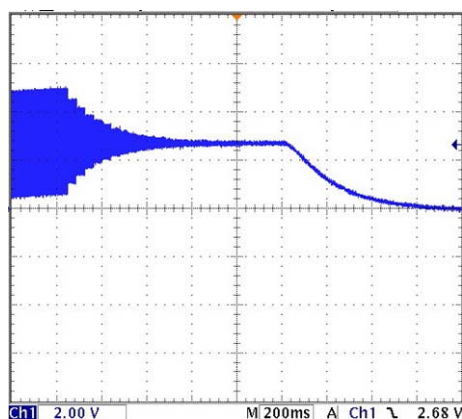


Figure 4. Shutdown Sequence in the Fade-on mode

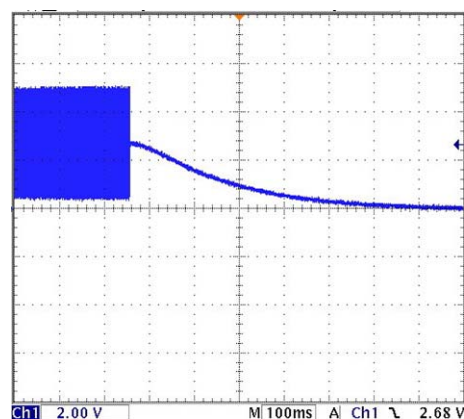


Figure 5. Shutdown Sequence in the Fade-off mode

VOLUME, SEDIFF AND SEMAX OPERATION

Three pins labeled VOLUME, SEDIFF and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD} .

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltage listed in the table are for $V_{DD}=5\text{V}$. For a different V_{DD} , the values in the table scale linearly. If $V_{DD}=4\text{V}$, multiply all the voltages in the table by $4\text{V}/5\text{V}$ or 0.8.



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The SM7511 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the single-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF = 0V, the difference between the BTL gain and the SE gain is 6dB. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20 dB, the gain in the headphone channel is fixed at 14 dB. The level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 6. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltage listed in the table are for VDD=5V. The values must be scaled for other values of VDD.

Table 1 and Table 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 7. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

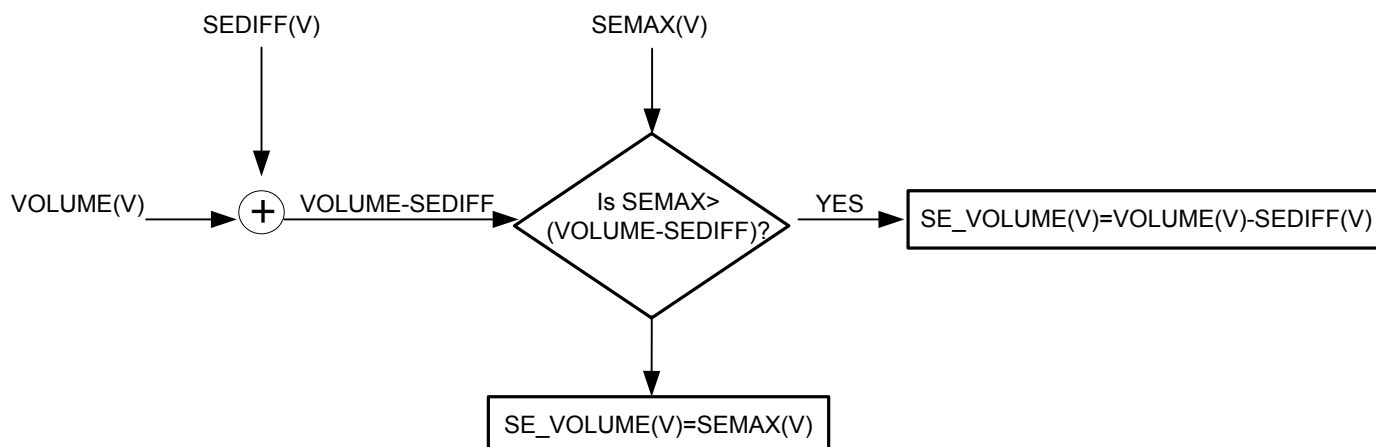


Figure 6. Block Diagram of SE Volume Control



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

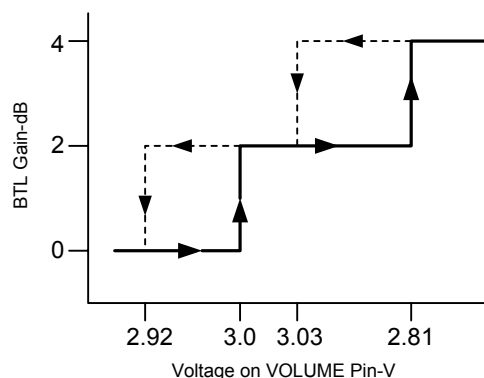


Figure 7. DC Volume Control Operation

TABLE OF GRAPHS

		FIGURE
THD+N Total harmonic distortion plus noise(BTL)	vs Frequency	8,9,10
	vs Output power	12,13,14,15,16,17,18,19
THD+N Total harmonic distortion plus noise(SE)	vs Frequency	11
	vs Output power	21,22,23
Closed loop response		24,25
Crosstalk		26,27
PSRR Power supply ripple rejection(BTL)	vs Frequency	28
PSRR Power supply ripple rejection(SE)	vs Frequency	29
Vn Output noise voltage	vs Frequency	30

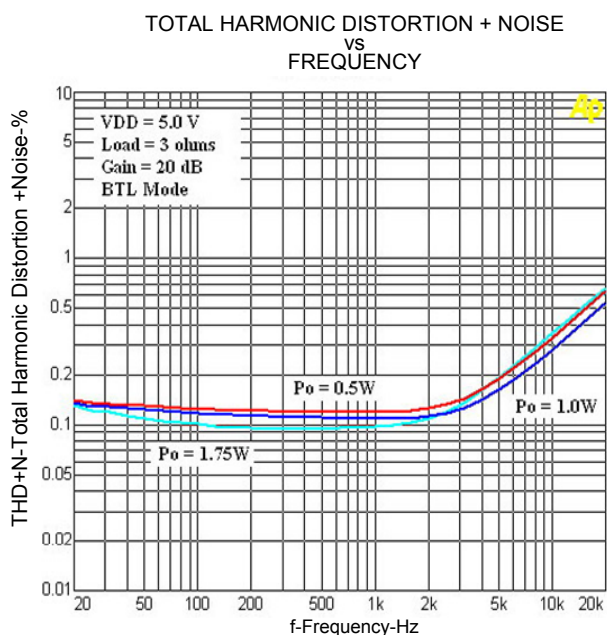


Figure-8

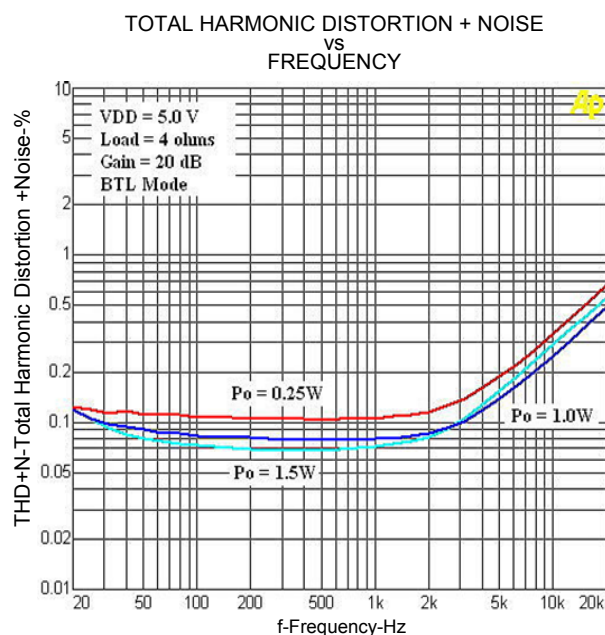


Figure-9



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

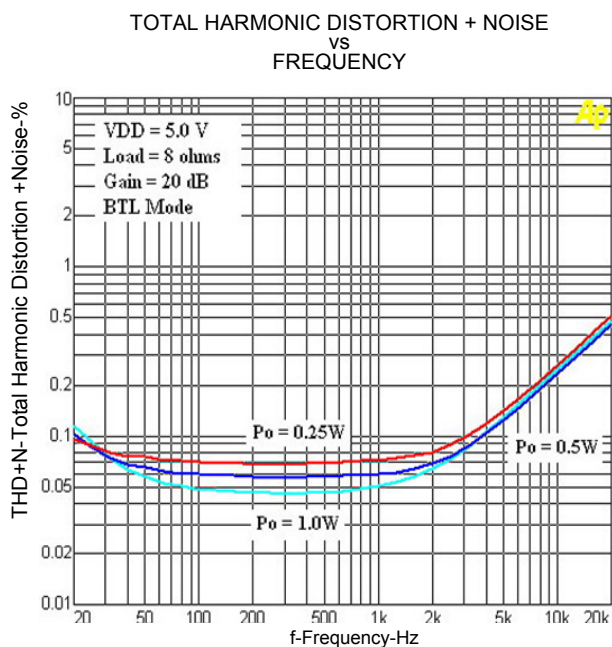


Figure-10

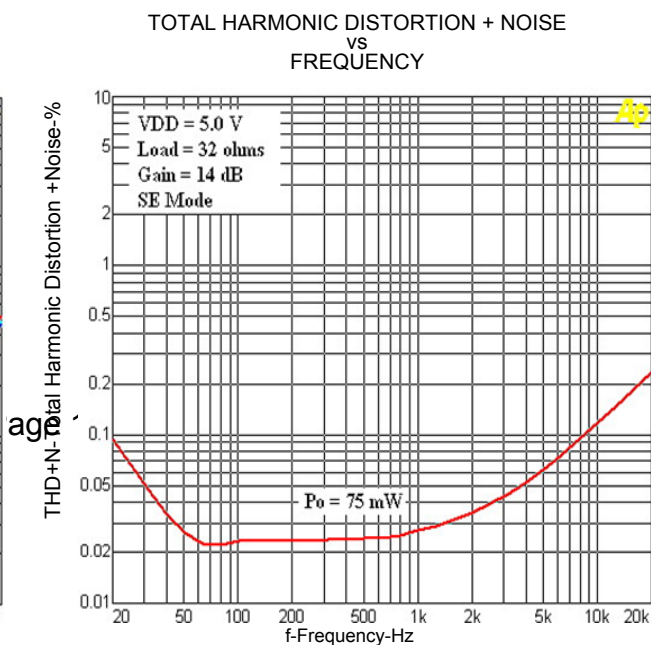


Figure-11

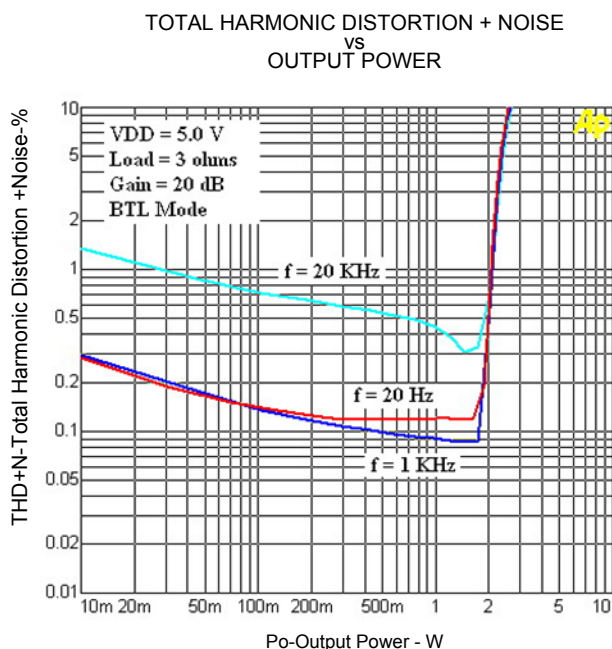


Figure-12

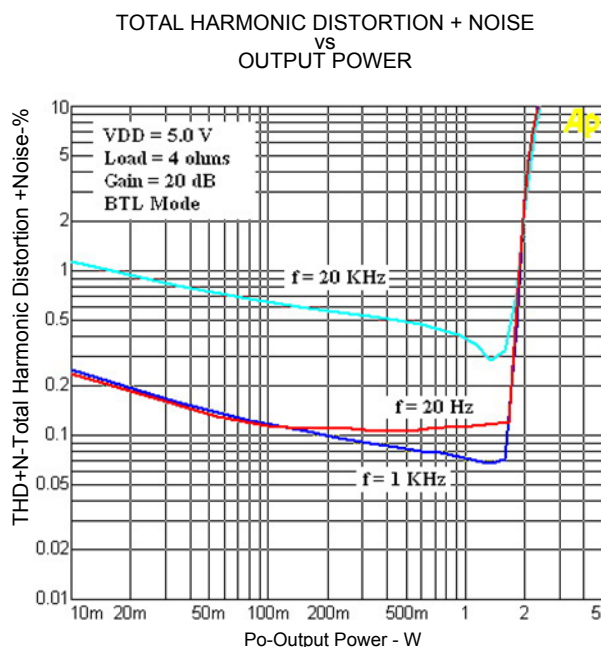


Figure-13



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

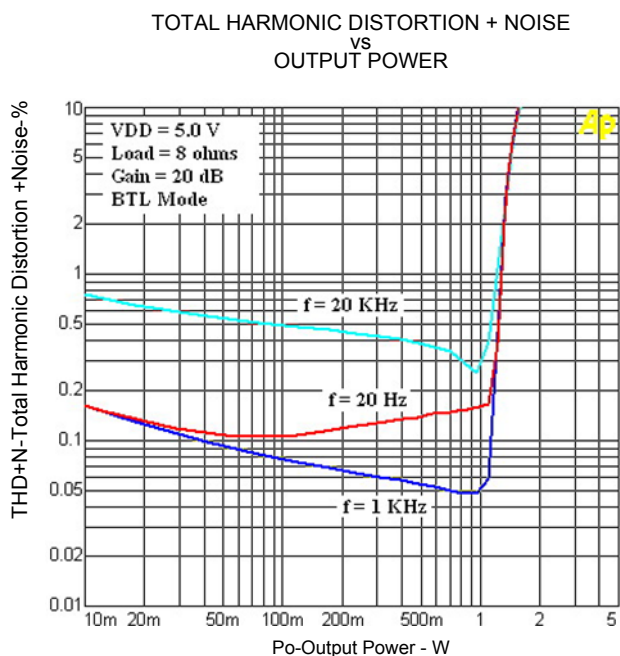


Figure-14

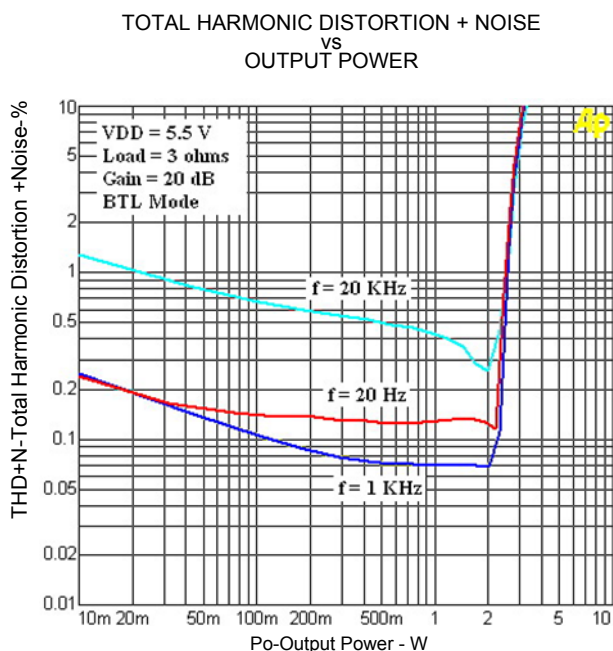


Figure-15

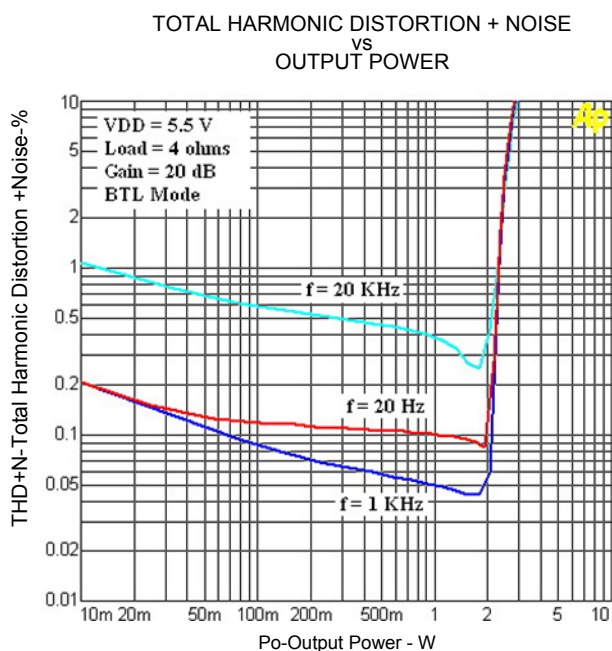


Figure-16

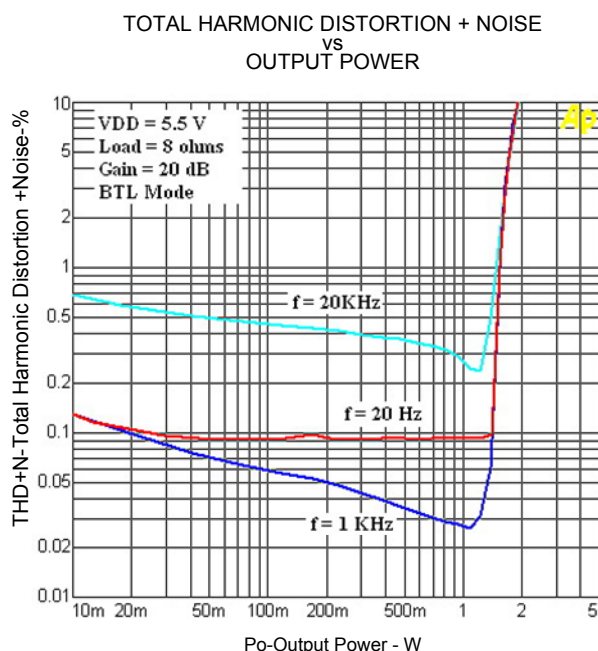


Figure-17



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

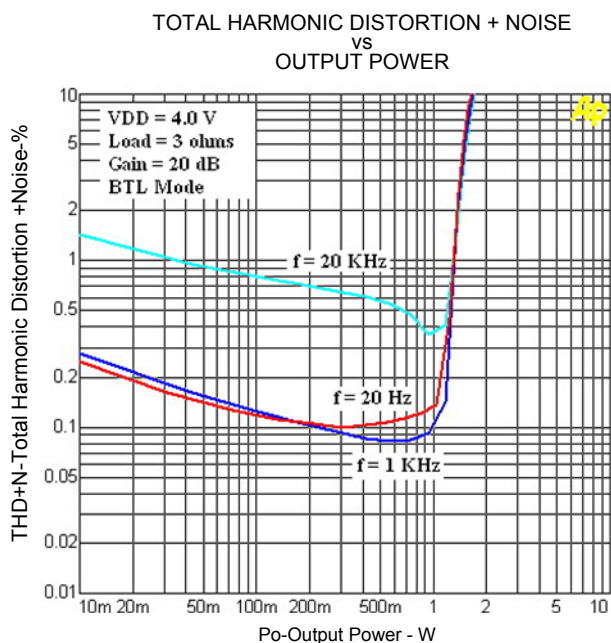


Figure-18

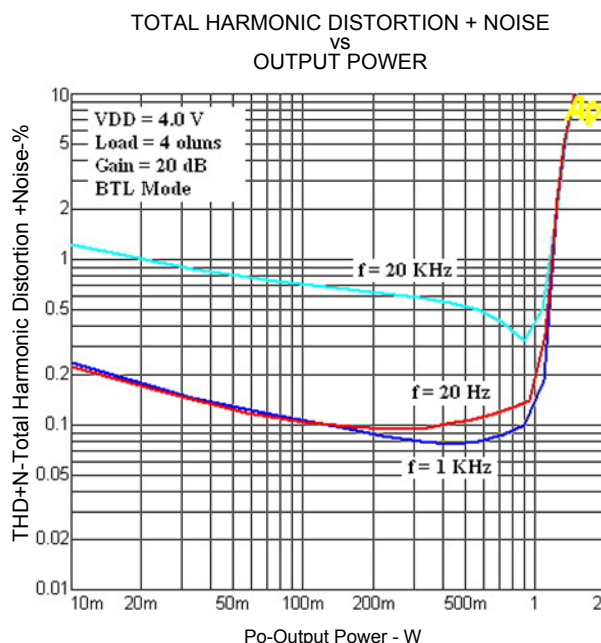


Figure-19

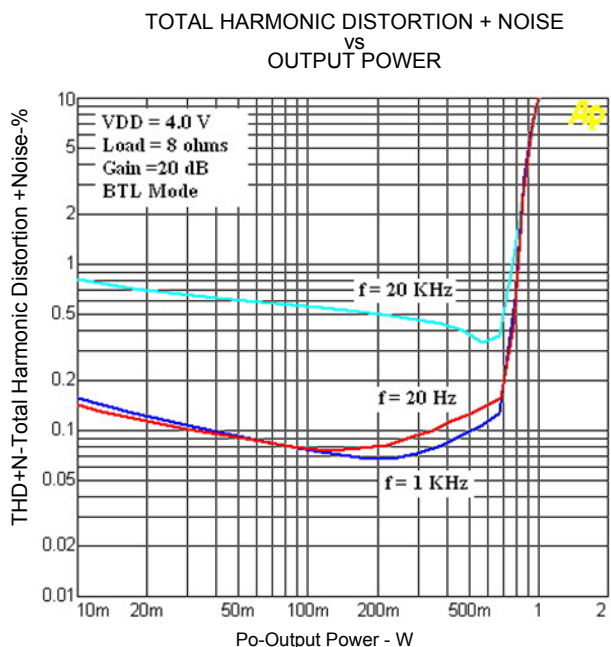


Figure-20

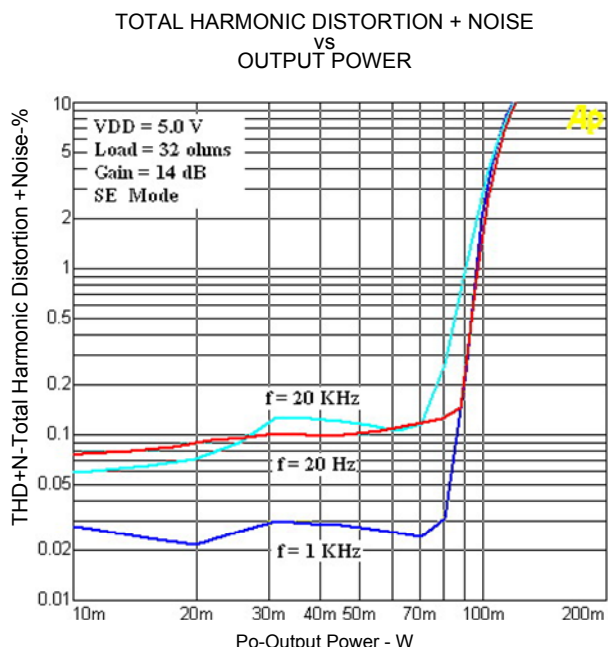


Figure-21



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

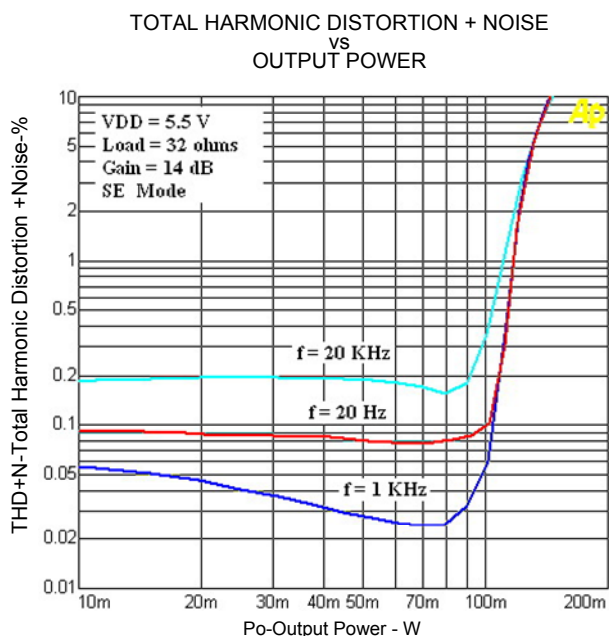


Figure-22

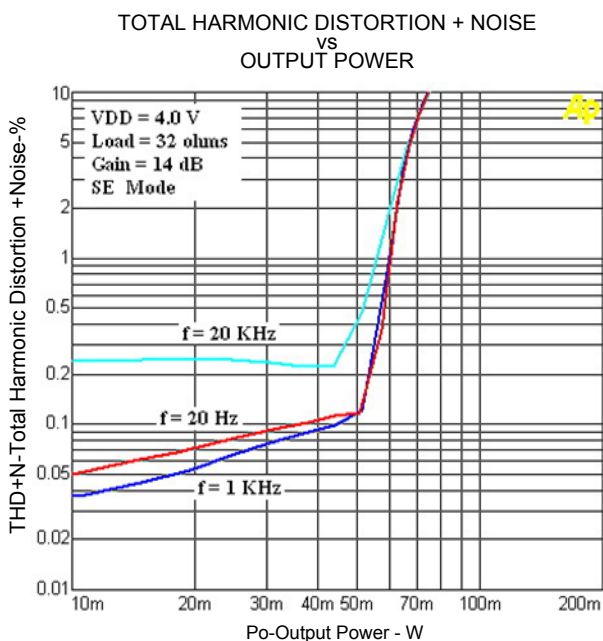


Figure-23

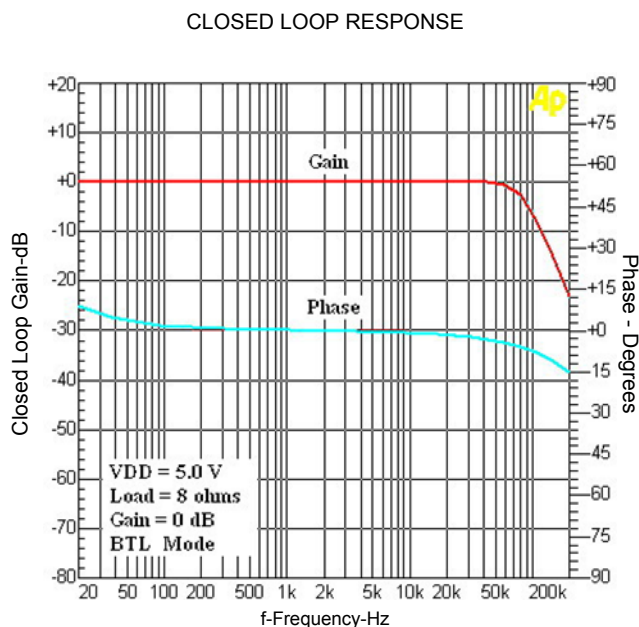


Figure-24

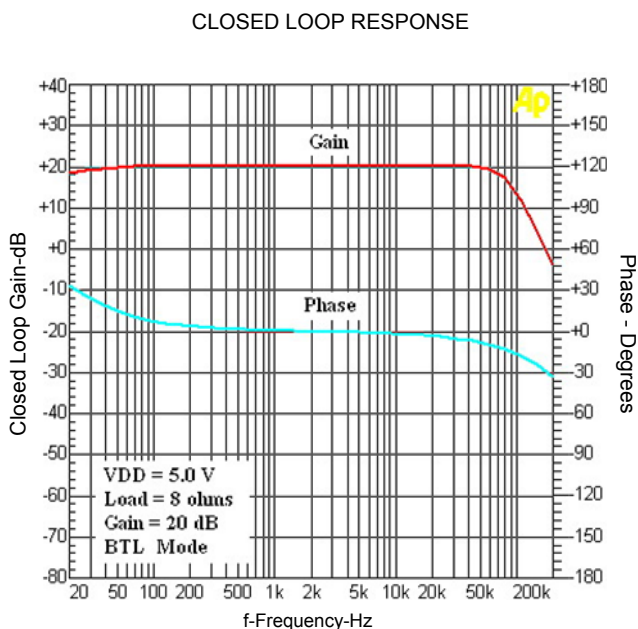


Figure-25



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

CROSSTALK
VS
FREQUENCY

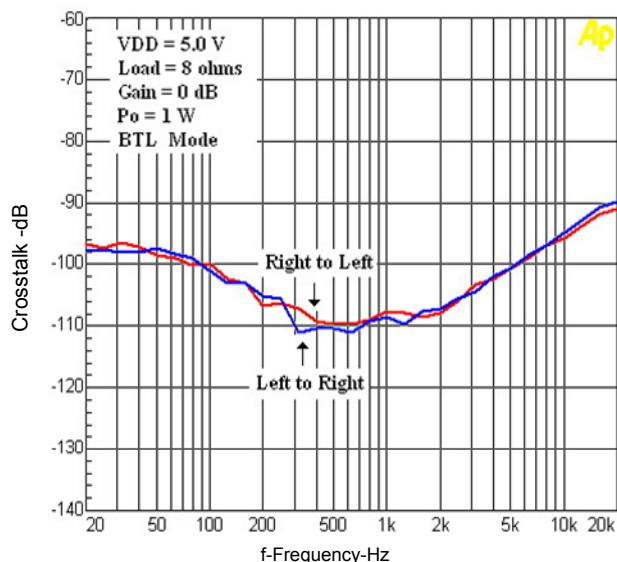


Figure-26

CROSSTALK
VS
FREQUENCY

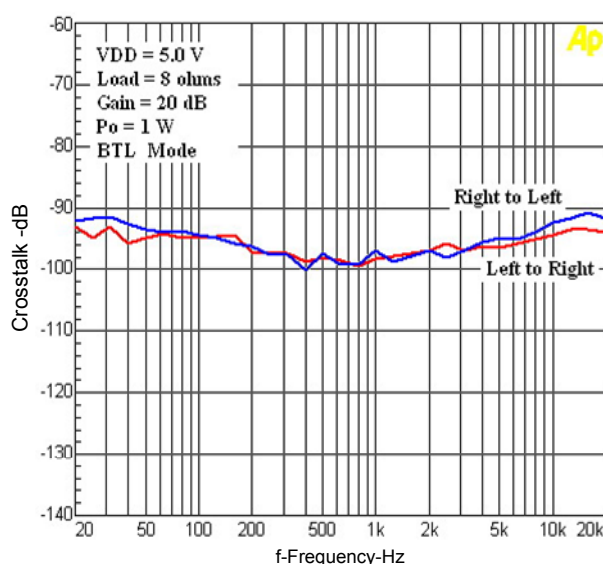


Figure-27

POWER SUPPLY REJECTION RATIO
VS
FREQUENCY

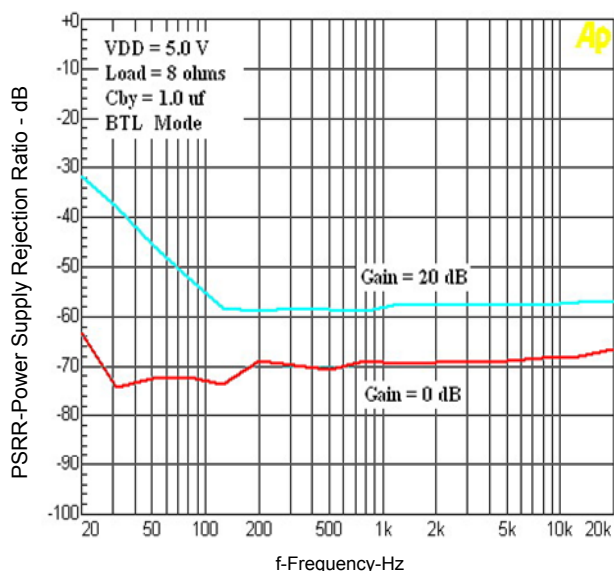


Figure-28

POWER SUPPLY REJECTION RATIO
VS
FREQUENCY

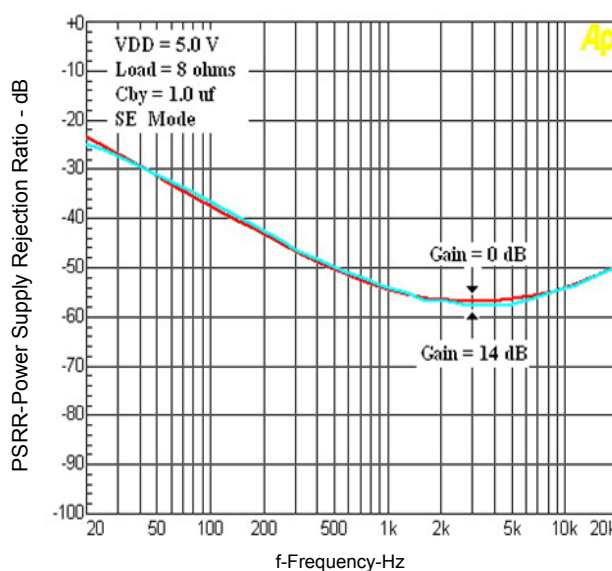


Figure-29



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

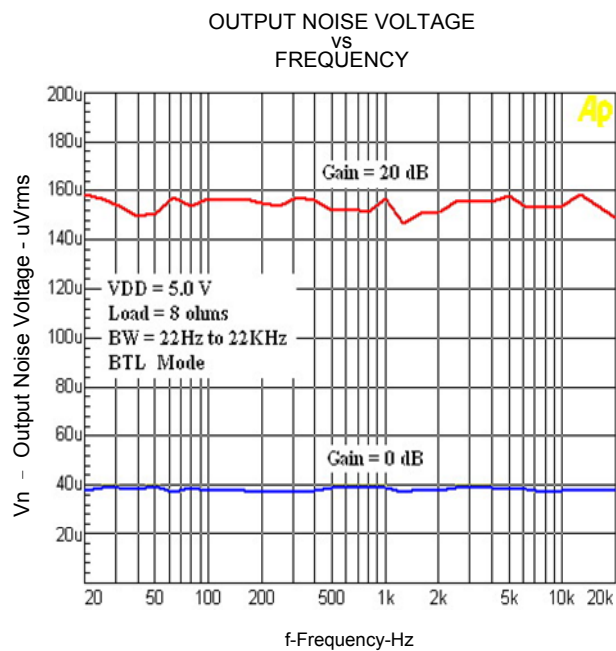


Figure-30

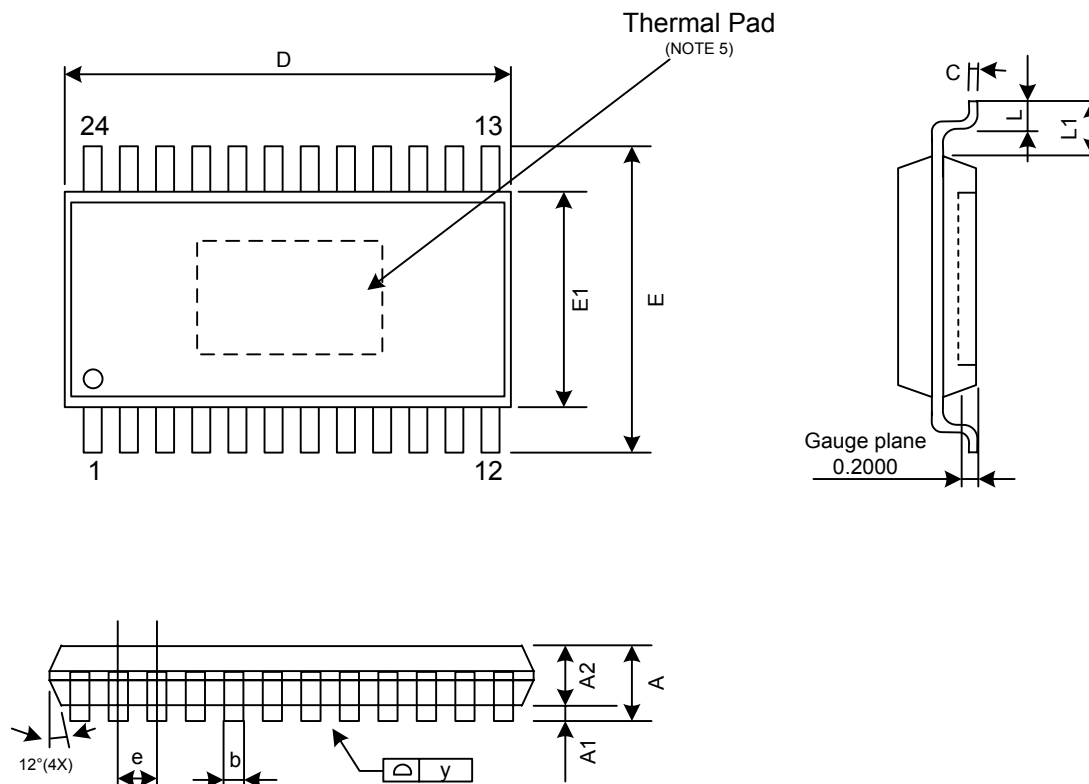


3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

PACKAGE OUTLINE

Unit : mm

SM7511 24 PIN TSSOP (150mil)



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.15
A1	0.00	—	0.10
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	—	0.65	—
L	0.45	0.60	0.75
y	—	—	0.10
θ	0°	—	8°
L1	0.90	1.00	1.10

NOTES:

1. PACKAGE BODY SIZE EXCLUDE MOLD FLASH PROTRUSION OR GATE BURRS.
2. TOLERANCE $\pm 0.1\text{mm}$ UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1mm
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
5. DIE PAD EXPOSURE SIZE IS ACCORDING TO LEAD FRAME DESIGN
6. FOLLOWED FROM JEDEC MO-153



3W STEREO AUDIO POWER AMPLIFIER WITH ADVANCED DC VOLUME CONTROL

Ordering Information

Package	Marking	Part Number (Tape and Reel)
TSSOP-24	SM7511	SM7511

Lead Free Information

Package	Marking	Lead Free Part Number
TSSOP-24	SM7511L	SM7511L

Green Information

Package	Marking	Green Part Number
TSSOP-24	SM7511G	SM7511G