REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add a new case outline to 1.2.2. Technical changes to 1.3 and 1.4. Technical changes to table I. Clarification made on figure 3 and figure 3. Add vendor CAGE code 01295. Editorial changes throughout.	91-08-29	D. M. Cool
B	Changes in accordance with 5962-R042-94.	93-11-18	M. L. Poelking
C	Add device type 03. Update boilerplate. Editorial changes throughout.	95-07-06	T. M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Tim H. Noh

CHECKED BY Tim H. Noh

APPROVED BY D. M. Cool

DRAWING APPROVAL DATE 89-08-16

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, SIGNAL PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-88619
A	67268	

SHEET 1 OF 25

DESC FORM 193
JUL 94

5962-E182-95

9004708 0010237 363

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-88619	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per (1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C25	Digital signal processor, 40 MHz
02	320C25-50	Digital signal processor, 50 MHz
03	320C26B	Digital signal processor, 40 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-P68	68	pin grid array package
Y	CQCC1-N68	68	leadless chip carrier package
Z	CQCC2-J68	68	J-leaded chip carrier package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) 1/	-0.3 V dc to 7 V dc
Output voltage range (V_O)	-0.3 V dc to 7 V dc
Input voltage range (V_I)	-0.3 V dc to 7 V dc
Continuous total power dissipation (P_D)	1.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC}):	
Device type 01 and 03	4.5 V dc mininum to 5.5 V dc maximum
Device type 02	4.75 V dc mininum to 5.25 V dc maximum
Supply voltage (V_{SS})	0 V dc
High level output currrent (I_{OH})	300 µA
Low level output current (I_{OL})	2 mA
High level input voltage (V_{IH}):	
D15-0	2.20 V dc minimum
FSX device types 01	2.30 V dc minimum
FSX device types 02, 03	2.20 V dc minimum
CLKR/CLKX	3.50 V dc minimum

1/ Voltage values for maximum ratings are with respect to V_{SS}.

1.4 Recommended operating conditions - Continued.

Device types 01 and 03	3.50 V dc minimum
Device type 02	4.00 V dc minimum
All others	3.00 V dc minimum
Low level input voltage (V_{IL}):	
D15-0/FSX/CLKIN/CLKX/CLKR	0.8 V dc maximum
All others	0.7 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Intergrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The fuctional block diagram shall be as specified on figure 2.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V dc, I_{OH} = 300 µA	$V_{IN} = V_{IL}$ max, V_{IH} min	1,2,3	01 03	2.4		V
		V_{CC} = 4.75 V dc, I_{OH} = 300 µA			02			
Low level output voltage	V_{OL}	V_{CC} = 4.5 V dc, I_{OL} = 2 mA	$V_{IN} = V_{IL}$ max, V_{IH} min	1,2,3	01 03		0.6	V
		V_{CC} = 4.75 V dc, I_{OL} = 2 mA			02			
Three-state current	I_Z	V_{CC} = 5.5 V dc	V_{IN} = 0 V	1,2,3	01 03		-20	µA
			$V_{IN} = V_{CC}$				20	
		V_{CC} = 5.25 V dc	$V_{IN} = V_{CC}$		02		20	
			V_{IN} = 0 V				-20	
Input current (X2/CLKIN)	I_I	$V_I = V_{CC}$	V_{CC} = 5.5 V	1,2,3	01		20	µA
			V_{CC} = 5.25 V		02		20	
			V_{CC} = 5.5 V		03		10	
		$V_I = V_{SS}$	V_{CC} = 5.5 V	1, 2, 3	01		-20	
			V_{CC} =5.25 V		02		-20	
			V_{CC} = 5.5 V		03		-10	
Input current (All others)		$V_I = V_{CC}$	V_{CC} = 5.5 V	1, 2, 3	01		10	
			V_{CC} = 5.25 V		02		10	
			V_{CC} = 5.5 V		03		10	
		$V_I = V_{SS}$	V_{CC} = 5.5 V	1, 2, 3	01		-10	
			V_{CC} = 5.25 V		02		-10	
			V_{CC} 5.5 V		03		-10	
Supply current — Normal	I_{CC}	V_{CC} = 5.5 V dc, f_x = 40 MHz		1,2,3	01 03		185	mA
Supply current — Idle/$\overline{\text{Hold}}$							100	
Supply current — Normal		V_{CC} = 5.25 V dc, f_x = 50 MHz			02		185	mA
Supply current — Idle/$\overline{\text{Hold}}$							100	
Input capacitance	C_{IN}	See 4.3.1c V_{IN} = 100 mV T_C = +25°C Freq = 1 MHz V_{CC} = 0.0 V		4	All		15	pF
Output capacitance	C_{OUT}			4	All		20	pF
Bidirectional capacitance	$C_{I/O}$			4	All		20	pF
Functional tests		See 4.3.1d, V_{CC} = min, max		7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Internal clock option							
Input clock frequency	f_X	See figure 3 1/ 2/ 4/	9,10,11	01 03	6.7	40	MHz
				02	6.7	50	
External clock option							
CLKOUT1/CLKOUT2 cycle time	$t_{c(C)}$	See figure 3 3/ 4/	9,10,11	01 03	100	600	ns
				02	80	600	
CLKIN high to CLKOUT1, CLKOUT2, STRB high/low	$t_{d(CIH-C)}$		9,10,11	01	5	30	ns
				02	5	28	
				03	5	32	
CLKOUT1/CLKOUT2 $\overline{STRB}$ fall time 2/	$t_{f(C)}$		9,10,11	01,03		5	ns
				02		5	
CLKOUT1/CLKOUT2 $\overline{STRB}$ rise time 2/	$t_{r(C)}$		9,10,11	01,03		5	ns
				02		3	
CLKOUT1/CLKOUT2 low pulse duration	$t_{w(CL)}$		9,10,11	01,03	2Q-8	2Q+8	ns
				02	2Q-7	2Q+5	
CLKOUT1/CLKOUT2 high pulse duration	$t_{w(CH)}$		9,10,11	01,03	2Q-8	2Q+8	ns
				02	2Q-5	2Q+7	
CLKOUT1(high or low) to CLKOUT2(high or low) high	$t_{d(C1-C2)}$		9,10,11	01,03	Q-6	Q+6	ns
				02	Q-6	Q+3	
CLKIN cycle time	$t_{c(CI)}$		9,10,11	01,03	25	150	ns
				02	20	150	
CLKIN low pulse duration 5/	$t_{w(CIL)}$	See figure 3 3/ 4/ $t_{c(CI)}$ = 25 ns	9,10,11	01,03	10	15	ns
				02	8		
CLKIN high pulse duration 5/	$t_{w(CIH)}$		9,10,11	01,03	10	15	ns
				02	8		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
External clock option - Continued.							
$\overline{SNYC}$ setup time before CLKIN low	$t_{su(S)}$	See figure 3 3/ 4/	9,10,11	01,03	5	Q-5	ns
				02	4	Q-4	
$\overline{SYNC}$ hold time from CLKIN low	$t_{h(S)}$		9,10,11	01,03	8		ns
				02	4		
Memory and peripheral interface timing							
$\overline{STRB}$ from CLKOUT1 (if $\overline{STRB}$ is present)	$t_{d(C1-S)}$	See figure 3 3/ 4/	9,10,11	01,03	Q-6	Q+6	ns
				02	Q-5	Q+3	
CLKOUT2 to $\overline{STRB}$ (if $\overline{STRB}$ is present)	$t_{d(C2-S)}$		9,10,11	01,03	-6	6	ns
				02	-2	5	
Address setup time before $\overline{STRB}$ low 6/	$t_{su(A)}$		9,10,11	01,03	Q-12		ns
				02	Q-13		
Address hold time after $\overline{STRB}$ high 6/	$t_{h(A)}$		9,10,11	01,03	Q-8		ns
				02	Q-4		
$\overline{STRB}$ low pulse duration (no wait states) 7/	$t_{w(SL)}$		9,10,11	01,03	2Q-5	2Q+5	ns
				02	2Q-5	2Q+5	
$\overline{STRB}$ high pulse duration (between consecutive 7/ cycles)	$t_{w(SH)}$		9,10,11	01,03	2Q-5	2Q+5	ns
				02	2Q-5	2Q+5	
Data write setup time before $\overline{STRB}$ high (no wait states)	$t_{su(D)W}$		9,10,11	01,03	2Q-20		ns
				02	2Q-17		
Data write hold time from $\overline{STRB}$ high	$t_{h(D)W}$		9,10,11	01,03	Q-10		ns
				02	Q-5		
Data bus starts being driven after $\overline{STRB}$ low (write cycle)	$t_{en(D)}$ 1/		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Memory and peripheral interface timing - Continued.							
Data bus three state after STRB high (write cycle)	$t_{dis(D)}$ 27/	See figure 3 3/ 4/	9,10,11	All		Q+15	ns
MSC valid from CLKOUT1	$t_{d(MSC)}$ 17/		9,10,11	01,03	-10	10	ns
				02	-5	10	
Read data access time from address time (read cycle) 6/ 8/	$t_{a(A)}$		9,10,11	01,03		3Q-40	ns
				02		3Q-31	
Data read setup time before STRB high	$t_{su(D)R}$		9,10,11	01,03	23		ns
				02	17		
Data read hold time from STRB high	$t_{h(D)R}$		9,10,11	All	0		ns
READY valid after STRB low (no wait states)	$t_{d(SL-R)}$		9,10,11	01,02		Q-20	ns
				03		Q-22	
READY valid after CLKOUT2 high	$t_{d(C2H-R)}$ 27/		9,10,11	01		Q-20	ns
				02		Q-21	
				03		Q-22	
READY hold time after STRB low (no wait states)	$t_{h(SL-R)}$		9,10,11	01,03	Q+3		ns
				02	Q-1		
READY hold after CLKOUT2 high	$t_{h(C2H-R)}$ 17/		9,10,11	01,03	Q+3		ns
				02	Q-1		
READY valid after MSC valid	$t_{d(M-R)}$ 2/		9,10,11	All		2Q-25	ns
READY hold time after MSC valid	$t_{h(M-R)}$ 1/		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limit Min	Limit Max	Unit
$\overline{RS}$, $\overline{INT}$, $\overline{BIO}$, and XF timing 9/							
CLKOUT1 low to reset state entered	$t_{d(RS)}$ 2/	See figure 3 3/ 4/	9,10,11	All		22	ns
CLKOUT1 to $\overline{IACK}$ valid	$t_{d(IACK)}$ 1/		9,10,11	01,03	-8	8	ns
				02	-5	7	
XF valid before falling edge of STRB	$t_{d(XF)}$		9,10,11	01,03	Q-12		ns
				02	Q-10		
$\overline{INT}/\overline{BIO}/\overline{RS}$ setup before CLKOUT1 high	$t_{su(IN)}$		9,10,11	01,03	32		ns
				02	25		
$\overline{INT}/\overline{BIO}/\overline{RS}$ hold after CLKOUT1 high	$t_{h(IN)}$		9,10,11	All	0		ns
$\overline{INT}/\overline{BIO}$ low pulse duration	$t_{w(IN)}$		9,10,11	All	$t_c(C)$		ns
$\overline{RS}$ low pulse duration	$t_{w(RS)}$		9,10,11	All	3 tc(C)		ns
$\overline{HOLD}$ timing							
$\overline{HOLDA}$ low after CLKOUT1 low	$t_{d(C1L-AL)}$ 1/	See figure 3 3/ 4/	9,10,11	01,03	0	10	ns
				02	1	11	
Address three-state after CLKOUT1 low (HOLD mode)	$t_{dis(C1L-A)}$ 2/ 6/		9,10,11	All		20	ns
$\overline{HOLD}$ high to $\overline{HOLDA}$ high	$t_{d(HH-AH)}$		9,10,11	01,03		25	ns
				02		19	
Address driven before CLKOUT1 low (HOLD mode)	$t_{en(A-C1L)}$ 2/ 6/		9,10,11	01		9	ns
				02,03		8	
$\overline{HOLD}$ valid after CLKOUT2 high 10/	$t_{d(C2H-H)}$		9,10,11	01,03		Q-24	ns
				02		Q-19	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

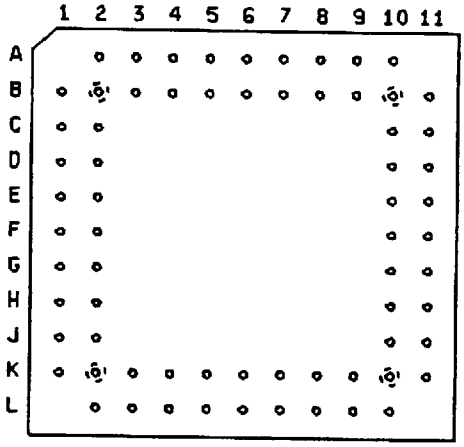
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Serial port timing							
DX valid after CLKX rising edge 11/	$t_{d(CH-DX)}$	See figure 3 3/ 4/	9,10,11	01,03		80	ns
				02		75	
DX valid after FSX falling edge (TXM = 0) 11/	$t_{d(FL-DX)}$		9,10,11	01,03		45	ns
				02		40	
FSX valid after CLKX rising edge (TXM = 1)	$t_{d(CH-FS)}$		9,10,11	01,03		45	ns
				02		40	
Serial port frequency	f_{sx}		9,10,11	01,03	1.25	5000	kHz
				02	1.25	6250	
Serial port clock (CLKX/CLKR) cycle time	$t_{c(SCK)}$		9,10,11	01,03	200		ns
				02	160		
Serial port clock (CLKX/CLKR) cycle time	$t_{c(SCK)}$		9,10,11	All		800	µs
Serial port clock (CLKX/CLKR) low pulse duration 12/	$t_{w(SCK)}$		9,10,11	01,03	80		ns
				02	64		
Serial port clock (CLKX/CLKR) high pulse duration 12/	$t_{w(SCK)}$		9,10,11	01,03	80		ns
				02	64		
FSX/FSR setup time before CLKX/CLKR falling edge (TXM = 0)	$t_{su(FS)}$		9,10,11	01,03	18		ns
				02	5		
FSX/FSR hold time after CLKX/ CLKR falling edge (TXM = 0)	$t_{h(FS)}$		9,10,11	01,03	20		ns
				02	10		
DR setup time before CLKR falling edge	$t_{su(DR)}$		9,10,11	01,03	10		ns
				02	5		
DR hold time after CLKR falling edge	$t_{h(DR)}$		9,10,11	01,03	20		ns
				02	10		

See footnotes at end of table.

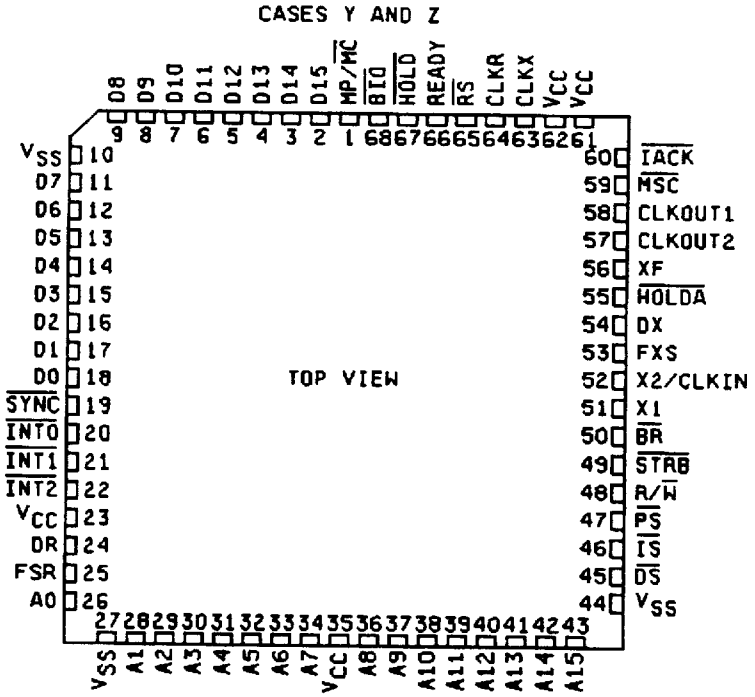
TABLE I. Electrical performance characteristics - Continued.

1/ This minimum value was determined from characterization data and is guaranteed to the value herein, if not tested.
2/ This maximum value was determined from characterization data and is guaranteed to the value herein, if not tested.
3/ Q = $1/4t_{c(C)}$, $V_{CC} = V_{CCmin}$, V_{CCmax}.
4/ Device types 01 and 03 V_{CC} = 4.5 V and 5.5 V. Device type 02 V_{CC} = 4.75 V and 5.25 V.
5/ Rise and fall times, assuming 40% to 60% duty cycle, are incorporated within this document. CLKIN rise and fall times must be less than 5 ns.
6/ A15-A0, PS, DS, IS, STRB, R/W and BR timings are all included in timings referenced as "address", where applicable.
7/ Delays between CLKOUT1/CLKOUT2 edges and STRB edges track each other, resulting in $t_{w(SL)}$ and $t_{w(SH)}$ being 2Q with no wait states.
8/ Read data access time is defined as $t_{a(A)} = t_{su(A)} + t_{w(SL)} - t_{su(D)R} + t_{r(C)}$.
9/ RS, INT, and BIO are asynchronous inputs and can occur at any time during a clock cycle. However, if the specified setup time is met, the exact sequence shown in the timing diagrams will occur. INT/BIO fall time must be less than 8 ns.
10/ HOLD is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur, otherwise a delay of one CLKOUT2 cycle will occur.
11/ The last occurrence of FSX falling and CLKX rising.
12/ The duty cycle of the serial port clock must be within 40 to 60 percent. Serial port clock (CLKX/CLKR) rise and fall times must be less than 25 ns.

CASE X

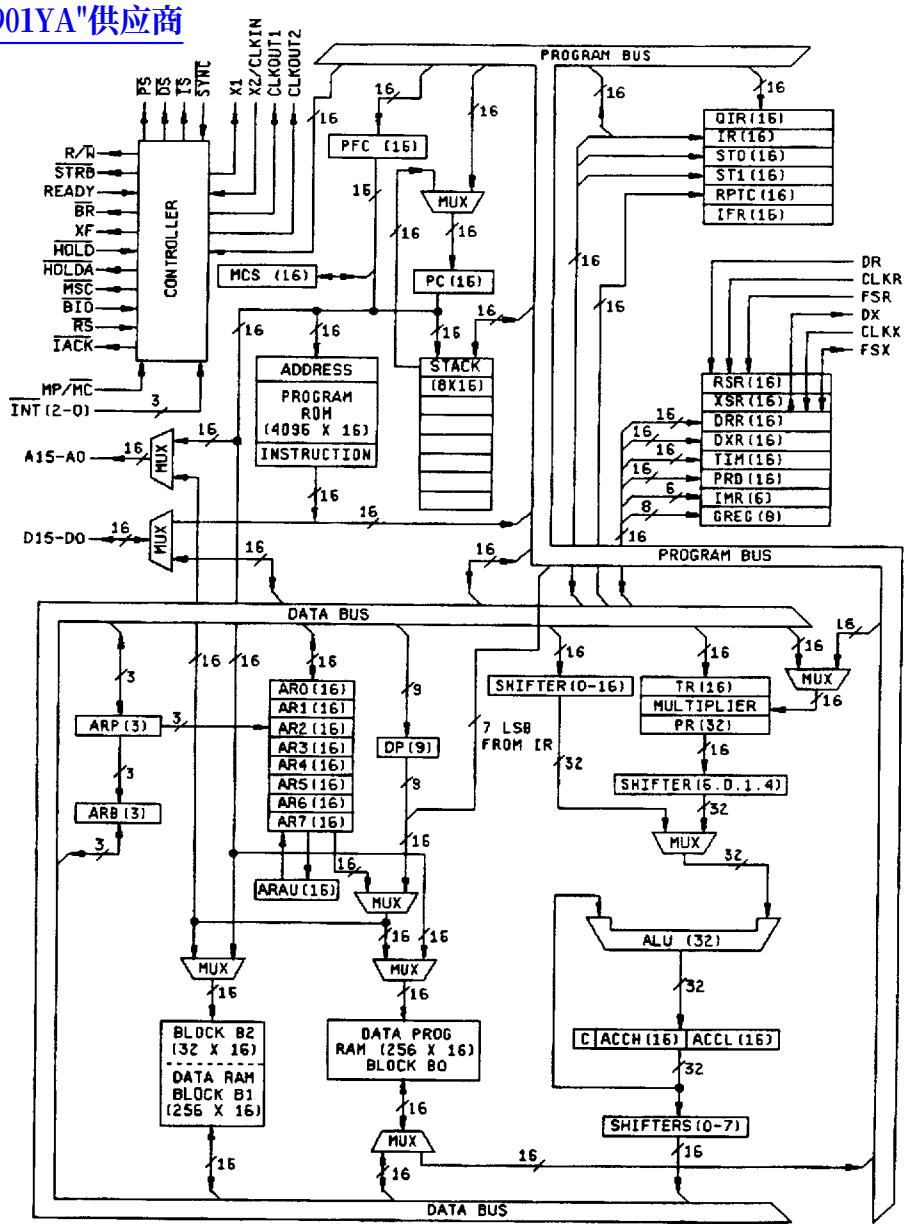


CASES Y AND Z



Function	pin	Function	pin	Function	pin	Function	pin	Function	pin	Function	pin
A0	K1	A12	K8	D2	E1	D14	A5	$\overline{INT2}$	H1	V_{CC}	H2
A1	K2	A13	L9	D3	D2	D15	B6	$\overline{IS}$	J11	V_{CC}	L6
A2	L3	A14	K9	D4	D1	$\overline{DR}$	J1	MP/$\overline{MC}$	A6	V_{SS}	B1
A3	K3	$\overline{A15}$	L10	D5	C2	DS	K10	$\overline{MSC}$	C10	V_{SS}	K11
A4	L4	$\overline{BIO}$	B7	D6	C1	DX	E11	PS	J10	V_{SS}	L2
A5	K4	BR	G11	D7	B2	FSR	J2	$\overline{READY}$	B8	XF	D11
A6	L5	CLKOUT1	C11	D8	A2	$\overline{FSX}$	F10	$\overline{RS}$	A8	X1	G10
A7	K5	CLKOUT2	D10	D9	B3	$\overline{HOLD}$	A7	R/$\overline{W}$	H11	X2/CLKIN	F11
A8	K6	CLKR	B9	D10	A3	$\overline{HOLDA}$	E10	$\overline{STRB}$	H10		
A9	L7	CLKX	A9	D11	B4	$\overline{IACK}$	B11	SYNC	F2		
A10	K7	D0	F1	D12	A4	$\overline{INTO}$	G1	V_{CC}	A10		
A11	L8	D1	E2	D13	B5	$\overline{INT1}$	G2	V_{CC}	B10		

FIGURE 1. Terminal connections.



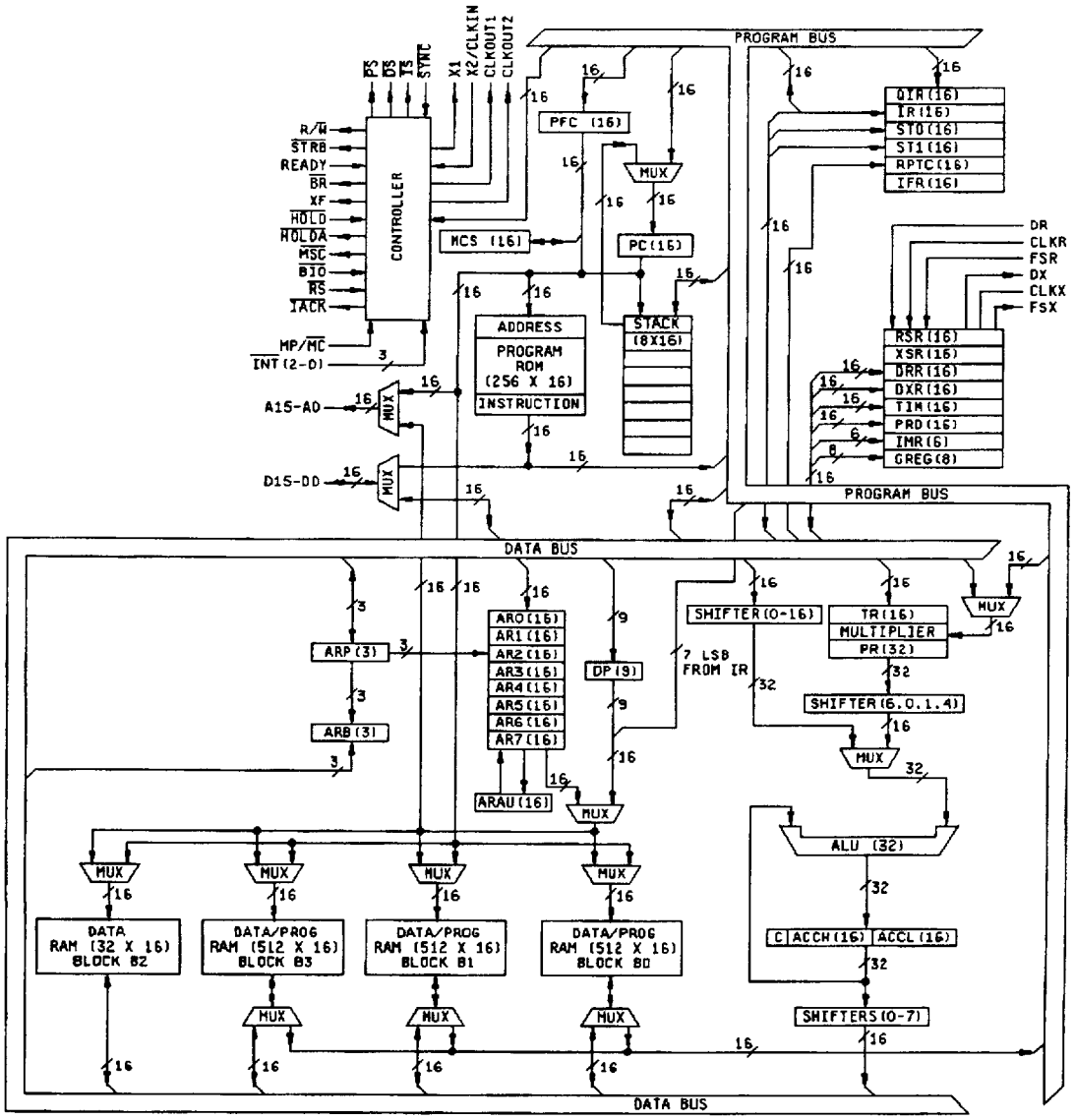
Device types 01 and 02.

FIGURE 2. Functional block diagram.

LEGEND

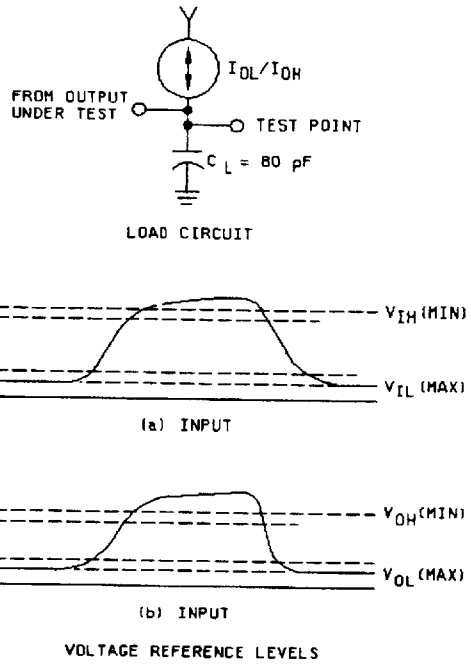
ACCH	= Accumulator high	IFR	= Interrupt flag register	PC	= Program counter
ACCL	= Accumualtor low	IMR	= Interrupt mask register	PFC	= Prefetch counter
ALU	= Arithmetic logic unit counter	IR	= Instruction register	RPTC	= Repeat instruction
ARAU	= Auxlliary register arithmetic unit	MCS	= Microcall stack	GREG	= Global memory allocation register
ARB	= Auxlliary register buffer	QIR	= Queue instruction register	RSR	= Serial port receive pointer shift register
ARP	= Auxlliary register pointer	PR	= Product register	XSR	= Serial port transmit shift register
DP	= Data memory page pointer	PRD	= Period register for timer	ARO AR7	= Auxillary registers
DRR	= Serial port data receive register	TIM	= Timer	ST0 ST1	= Status registers
DXR	= Serial port data transmit register	TR	= Temporary register	C	= Carry bit

FIGURE 2. Functional block diagram - Continued.



Device type 03.

FIGURE 2. Functional block diagram. - continued



Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.2 V with the exception of CLKOUT1, CLKOUT2 and STRB timing that are referenced from a falling edge low voltage of 1.1 V and a rising edge low voltage of 2.2 V.

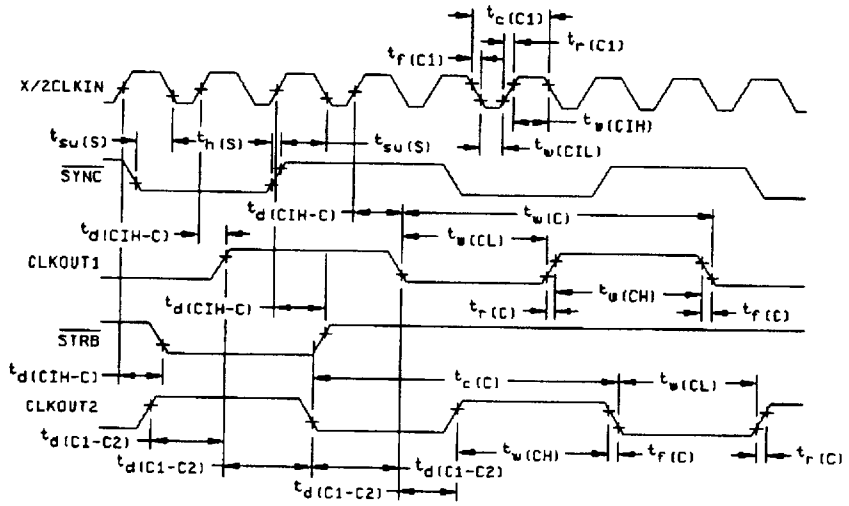


FIGURE 3. Switching test circuit and waveforms.

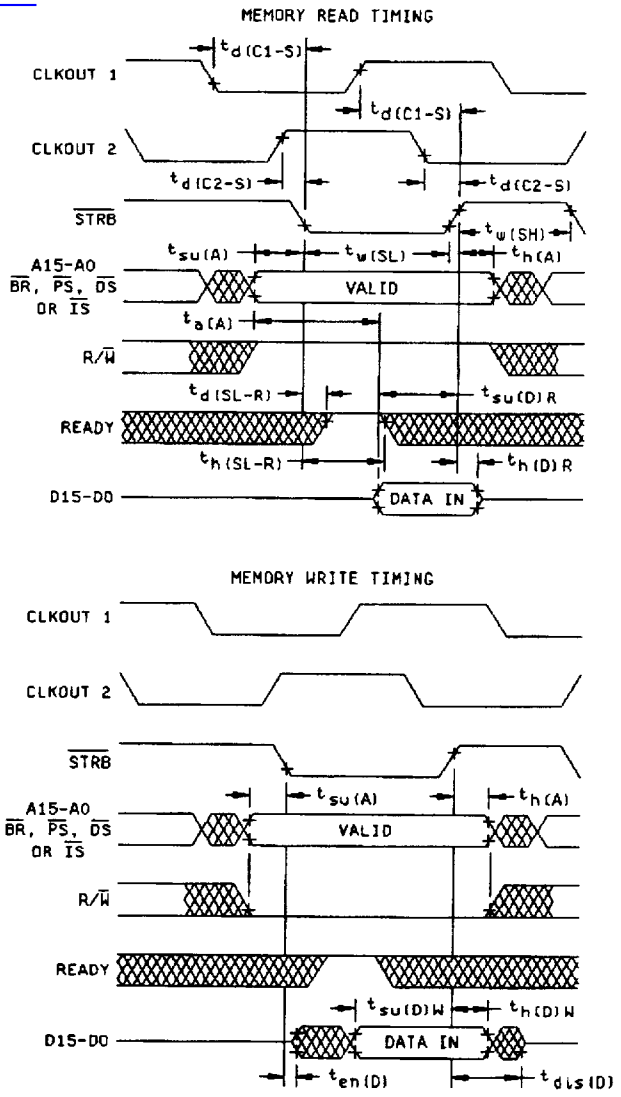


FIGURE 3. Switching test circuit and waveforms - Continued.

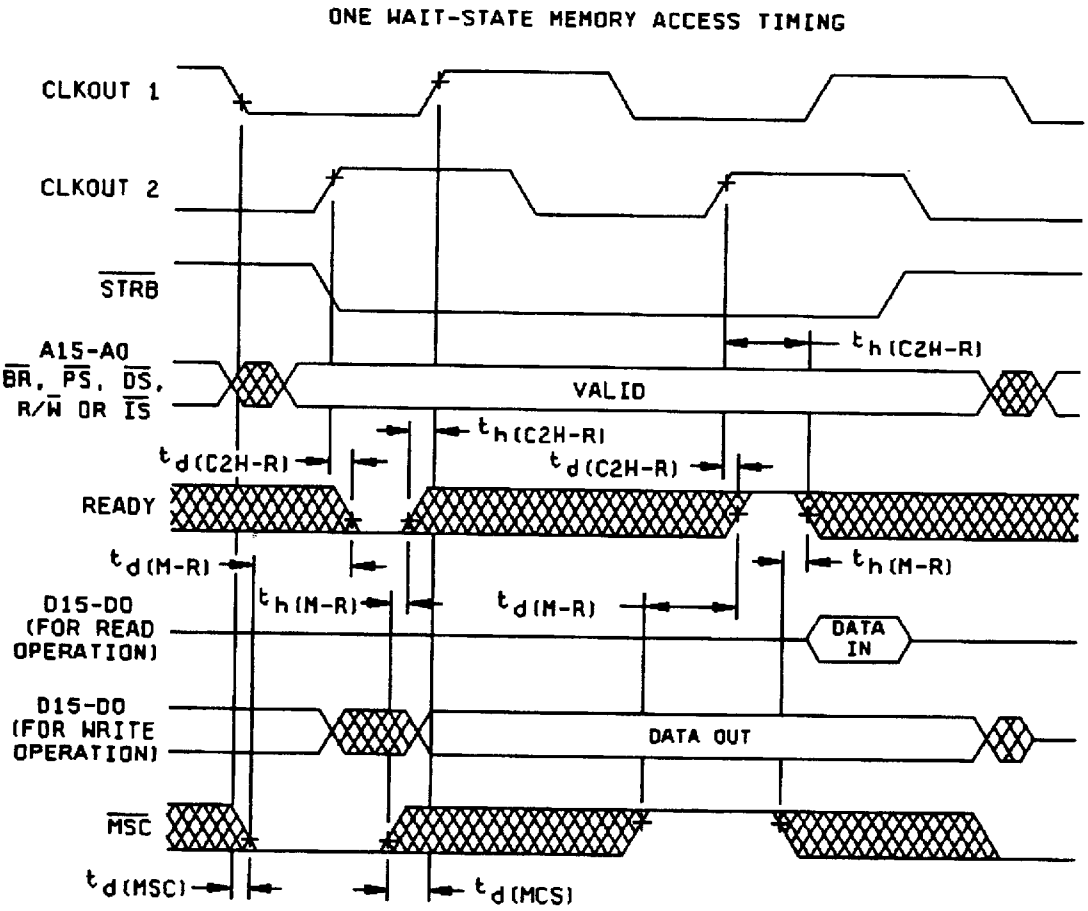
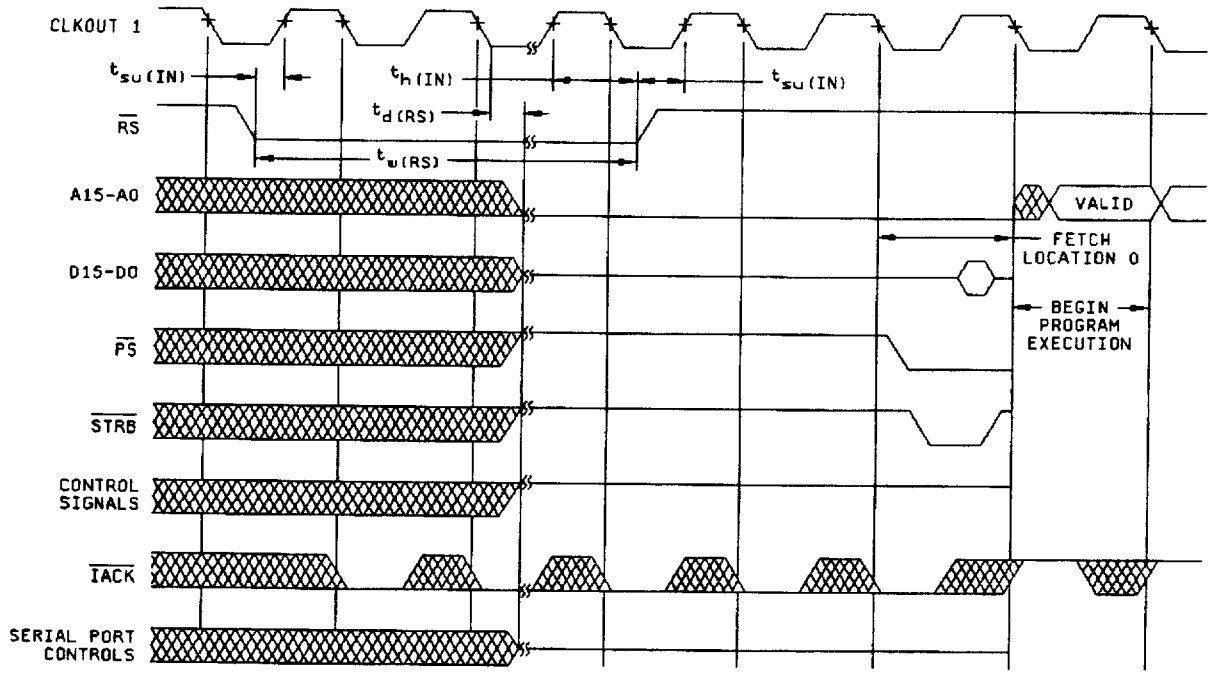


FIGURE 3. Switching test circuit and waveforms - Continued.

RESET TIMING



CONTROL SIGNALS ARE $\overline{DS}$, $\overline{IS}$, R/$\overline{W}$, AND XF.
SERIAL PORT CONTROLS ARE DX AND FSX.

INTERRUPT TIMING

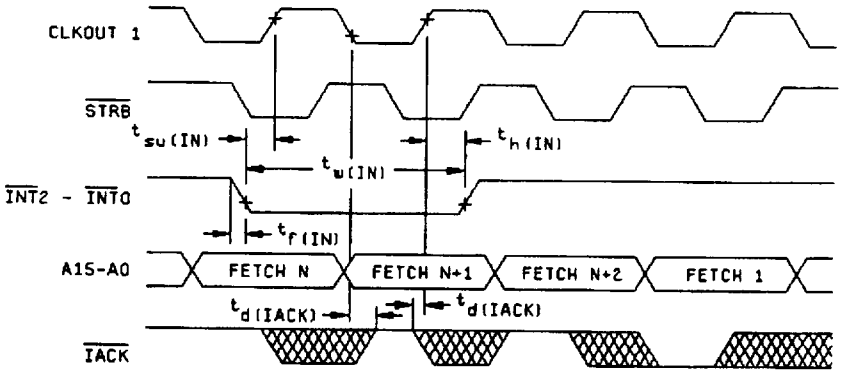


FIGURE 3. Switching test circuit and waveforms - Continued.

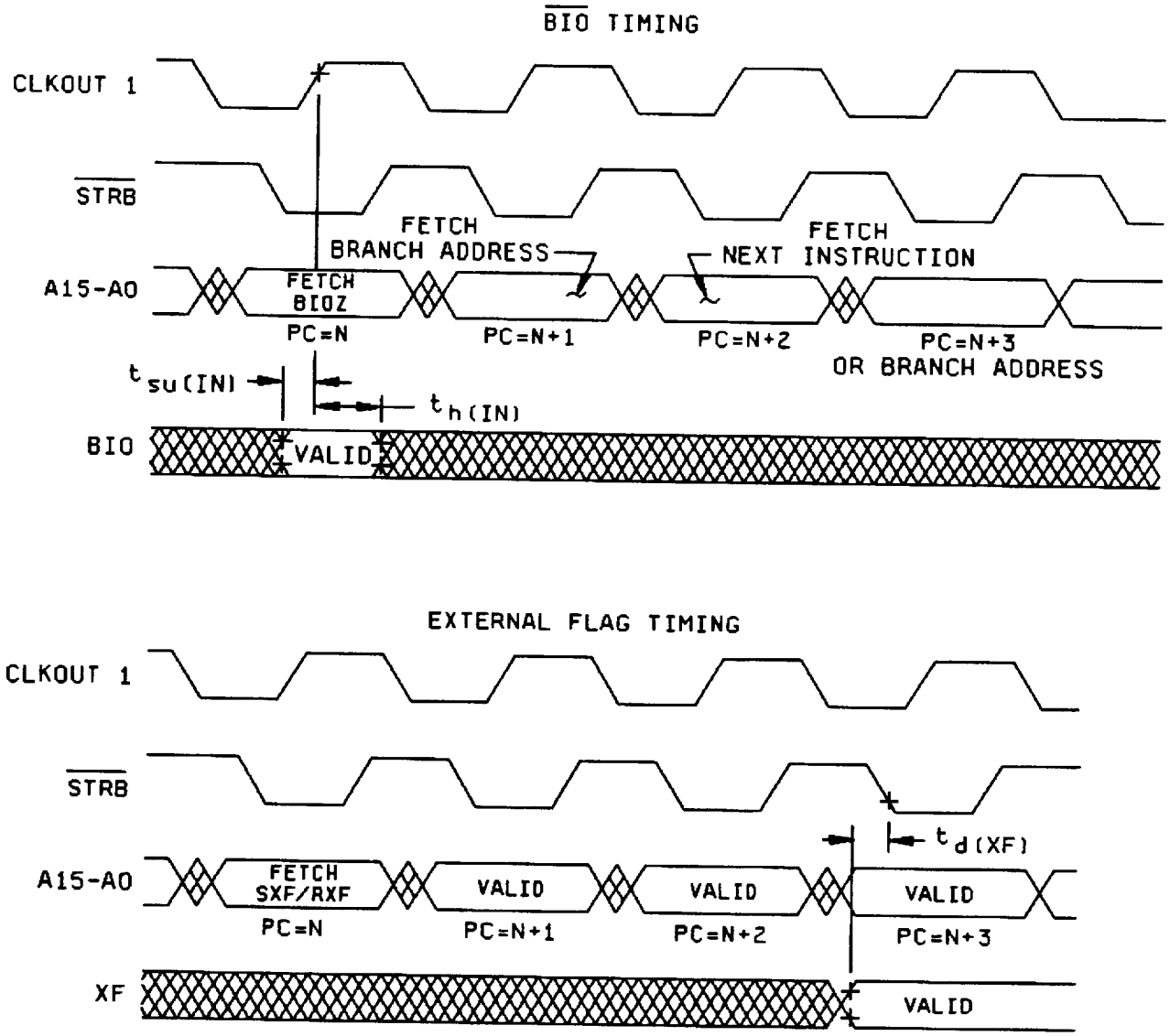
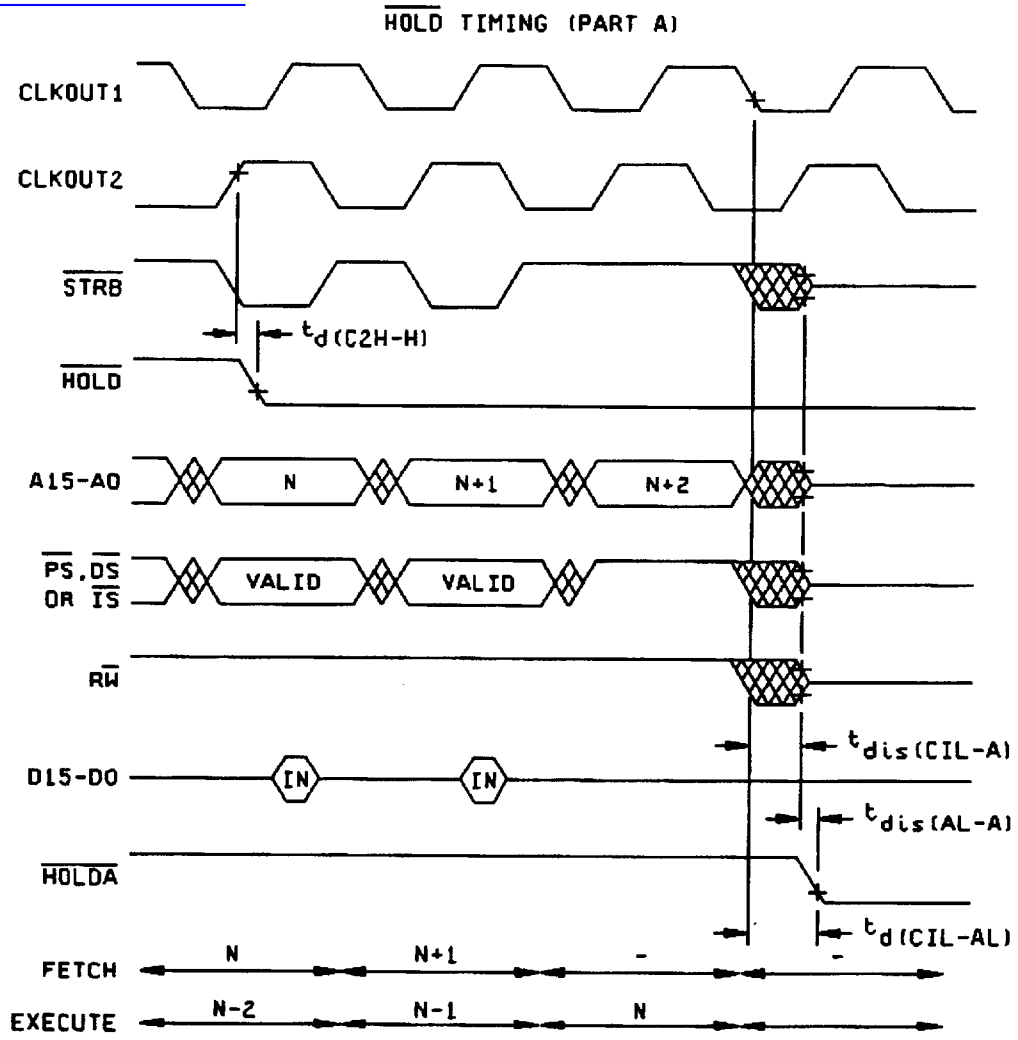


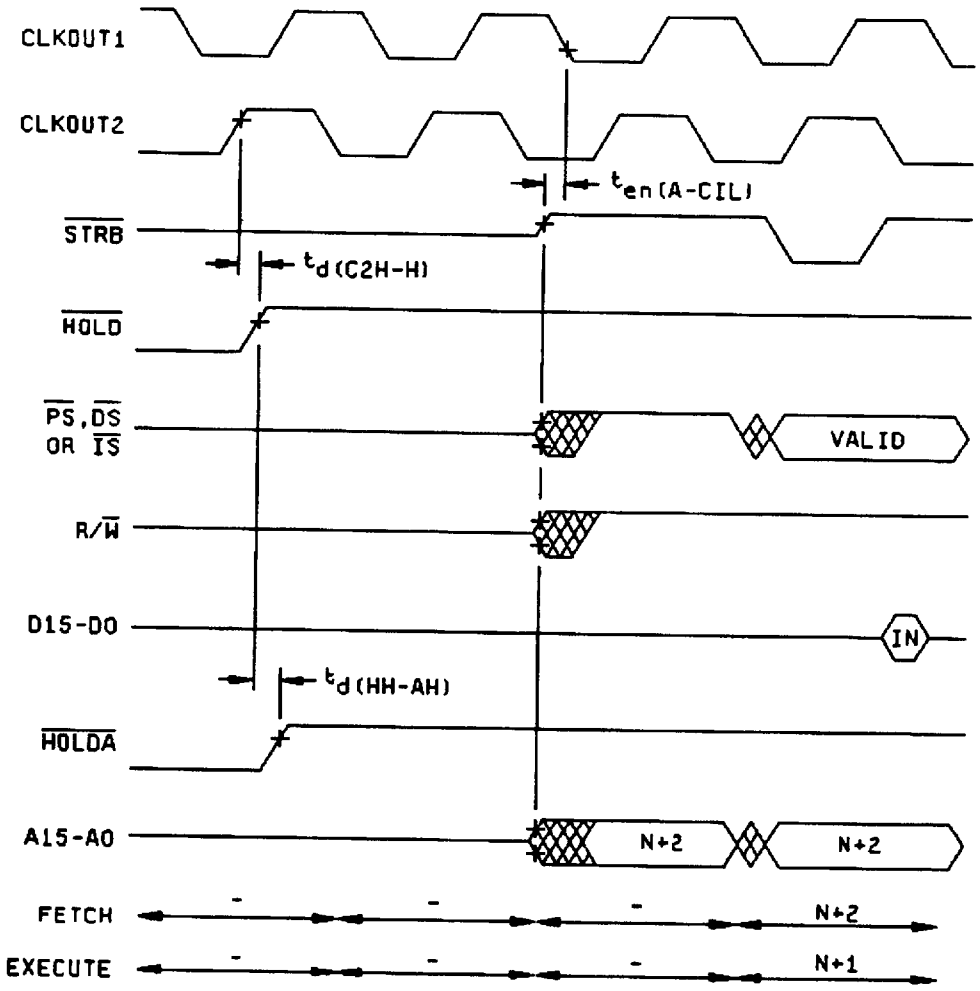
FIGURE 3. Switching test circuit and waveforms - Continued.



NOTE: HOLD is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

FIGURE 3. Switching test circuit and waveforms - Continued.

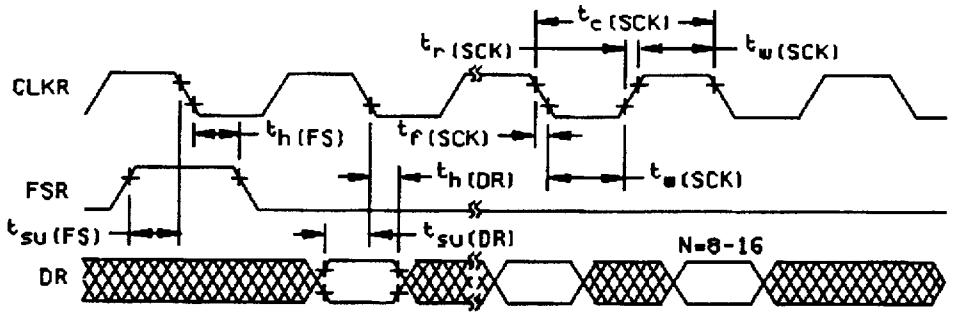
$\overline{\text{HOLD}}$ TIMING (PART B)



NOTE: $\overline{\text{HOLD}}$ is an asynchronous input and can occur at any time during a clock cycle. If the specified timing is met, the exact sequence shown will occur; otherwise, a delay of one CLKOUT2 cycle will occur.

FIGURE 3. Switching test circuit and waveforms - Continued.

SERIAL PORT RECEIVE TIMING



SERIAL PORT TRANSMIT TIMING

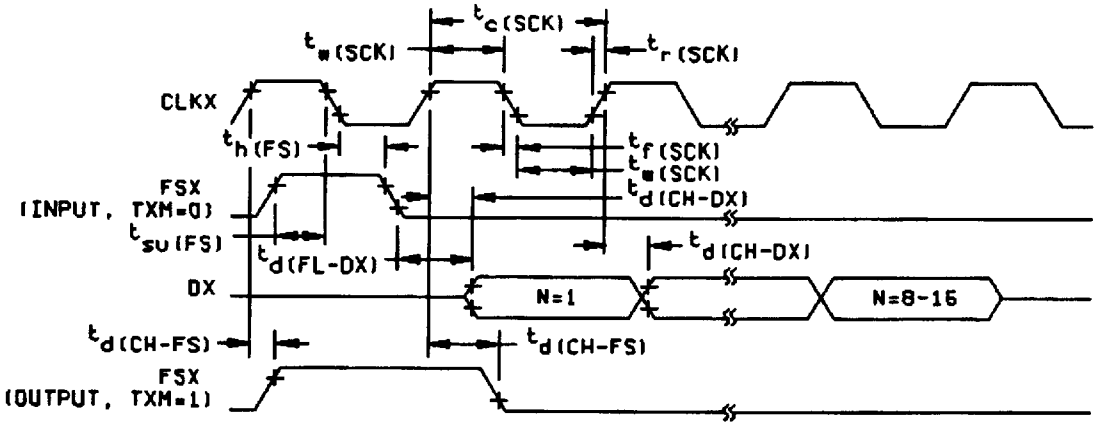


FIGURE 3. Switching test circuit and waveforms - Continued.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	*1,2,3,7,8,9,10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,8A,10

* PDA applies to subgroups 1 and 7.

c. Subgroup 4 (C_{IN}, C_{OUT}, and $C_{I/O}$) shall be measured for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

d. Subgroups 7 and 8 shall verify the instruction set. The instruction set forms a part of the vendors test tape and shall be maintained and available at the approved source of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5765 or telephone (513) 296-8525.

6.6 Approved source of supply. An approved source of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.