

# LP3958

## Lighting Management Unit with High Voltage Boost Converter

### General Description

LP3958 is a Lighting Management Unit for portable applications. It is used to drive display backlight and keypad LEDs. The device can drive 5 separately connected strings of LEDs with high voltage boost converter.

The keypad LED driver allows driving LEDs from high voltage boost converter or separate supply voltage. The MAIN and SUB outputs are high resolution current mode drivers. Keypad LED outputs can be used in switch mode and current mode. External PWM control can be used for any selected outputs.

The device is controlled through 2-wire low voltage I<sup>2</sup>C compatible interface that reduces the number of required connections.

LP3958 is offered in a tiny 25-bump micro-SMD package.

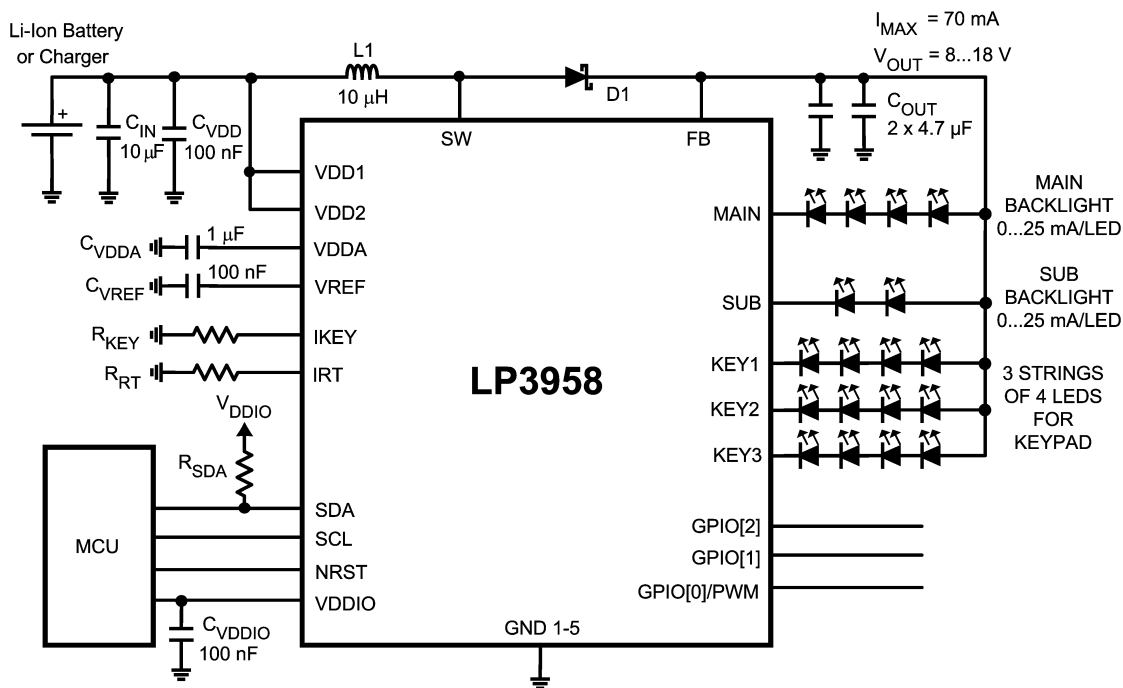
### Features

- High efficiency boost converter with programmable output voltage
- 2 individual drivers for serial display backlight LEDs
- 3 drivers for serial keypad LEDs
- Automatic dimming controller
- Stand alone serial keypad LEDs controller
- 3 general purpose IO pins
- 25-bump micro SMD Package: (2.54mm x 2.54mm x 0.6mm)

### Applications

- Cellular Phones and PDAs
- MP3 Players
- Digital Cameras

### Typical Application

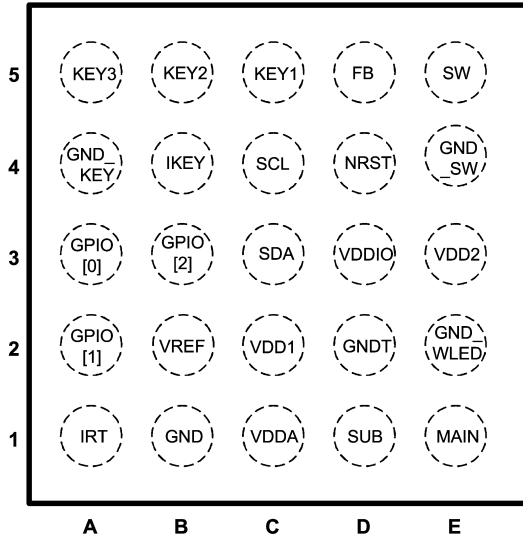


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# Connection Diagrams and Package Mark Information

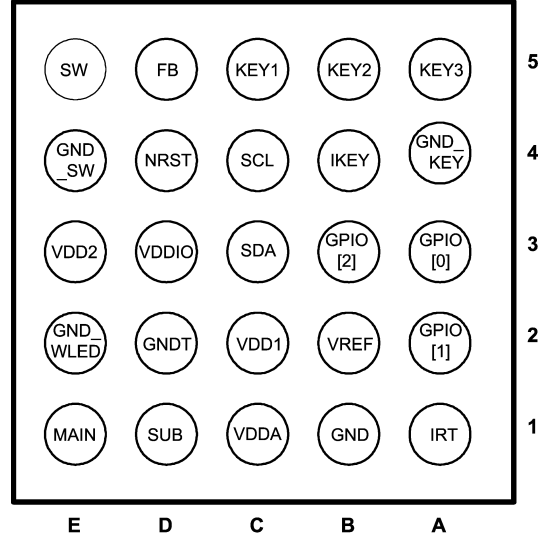
## CONNECTION DIAGRAMS

25-Bump Thin Micro SMD Package, Large Bump  
NS Package Number TLA25CCA



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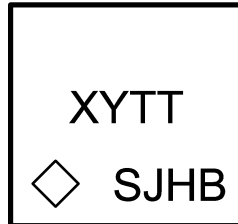
Top View



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Bottom View

## PACKAGE MARK



XY = 2 Digit Date Code

TT = Die Traceability

SJHB = Product Identification

◇ = Pin 1A

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## ORDERING INFORMATION

Order Number	Package Marking	Supplied As	Spec/Flow
LP3958TL	SJHB	TNR 250	NoPb
LP3958TLX	SJHB	TNR 3000	NoPb

## Connection Diagrams and Package Mark Information (Continued)

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### PIN DESCRIPTIONS

Pin #	Name	Type	Description
5E	SW	Output	Boost Converter Power Switch
5D	FB	Input	Boost Converter Feedback
5C	KEY1	Output	Keypad LED Output 1 (Current Sink)
5B	KEY2	Output	Keypad LED Output 2 (Current Sink)
5A	KEY3	Output	Keypad LED Output 3 (Current Sink)
4E	GND_SW	Ground	Power Switch Ground
4D	NRST	Input	External Reset, Active Low
4C	SCL	Logic Input	Clock Input for I <sup>2</sup> C Compatible Interface
4B	IKEY	Input	External Keypad LED Maximum Current Set Resistor
4A	GND_KEY	Ground	Ground for KEY LED Currents
3E	VDD2	Power	Supply Voltage 3.0...5.5 V
3D	VDDIO	Power	Supply Voltage for Digital Input/Output Buffers and Drivers
3C	SDA	Logic Input/Output	Data Input/Output for I <sup>2</sup> C Compatible Interface
3B	GPIO[2]	Logic Input/Output	General Purpose Logic Input/Output
3A	GPIO[0] / PWM	Logic Input/Output	General Purpose Logic Input/Output / External PWM Input
2E	GND_WLED	Ground	Ground for White LED Currents (MAIN and SUB Outputs)
2D	GNDT	Ground	Ground
2C	VDD1	Power	Supply Voltage 3.0...5.5 V
2B	VREF	Output	Reference Voltage (1.23V)
2A	GPIO[1]	Logic Input/Output	General Purpose Logic Input/Output
1E	MAIN	Output	MAIN Display White LED Current Output (Current Sink)
1D	SUB	Output	SUB Display White LED Current Output (Current Sink)
1C	VDDA	Output	Internal LDO Output (2.80V)
1B	GND	Ground	Ground for Core Circuitry
1A	IRT	Input	Oscillator Frequency Set Resistor

## Absolute Maximum Ratings (Notes 1, 2)

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**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

V (SW, FB, MAIN, SUB, KEY1, KEY2, KEY3)	-0.3V to +20V
$V_{DD1}$ , $V_{DD2}$ , $V_{DDIO}$ , $V_{DDA}$	-0.3V to +6.0V
Voltage on $I_{KEY}$ , $I_{RT}$ , $V_{REF}$	-0.3V to $V_{DD1}+0.3V$ with 6.0V max
Voltage on Logic Pins	-0.3V to $V_{DDIO}+0.3V$ with 6.0V max
$I(V_{REF})$	10 $\mu$ A
$I(KY1, KY2, KY3)$	100mA
Continuous Power Dissipation (Note 3)	Internally Limited
Junction Temperature ( $T_{J-MAX}$ )	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Soldering) (Note 4)	260°C
ESD Rating (Note 5)	
Human Body Model:	2kV
Machine Model:	200V

## Operating Ratings (Notes 1, 2)

V (SW, FB, MAIN, SUB)	0 to +19V
$V_{DD1,2}$	3.0 to 5.5V
$V_{DDIO}$	1.65V to $V_{DD1}$
Recommended Load Current (KEY1, KEY2, KEY3) CC Mode	0mA to 15mA/driver
Recommended Total Boost Converter Load Current	0mA to 70mA
Junction Temperature ( $T_J$ ) Range	-30°C to +125°C
Ambient Temperature ( $T_A$ ) Range (Note 6)	-30°C to +85°C

## Thermal Properties

Junction-to-Ambient Thermal Resistance( $\theta_{JA}$ ), TLA25 Package (Note 7)	60 - 100°C/W
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## Electrical Characteristics (Notes 2, 8)

Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T<sub>A</sub> < +85°C). Unless otherwise noted, specifications apply to the LP3958 Block Diagram with: V<sub>DD1,2</sub> = 3.0 ... 5.5V, C<sub>VDD</sub> = C<sub>VDDIO</sub> = 100nF, C<sub>OUT</sub> = 2 x 4.7μF, C<sub>IN</sub> = 10μF, C<sub>VDDA</sub> = 1μF, C<sub>VREF</sub> = 100nF, L1 = 10μH, R<sub>KEY</sub> = 8.2kΩ and R<sub>RT</sub> = 82kΩ (Note 9).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I <sub>VDD</sub>	Standby supply current (V <sub>DD1</sub> , V <sub>DD2</sub> )	NSTBY = L Register 0DH=08H (Note 10)		1.7	<b>7</b>	μA
	No-boost supply current (V <sub>DD1</sub> , V <sub>DD2</sub> )	NSTBY = H, EN_BOOST = L		300	<b>800</b>	μA
	No-load supply current (V <sub>DD1</sub> , V <sub>DD2</sub> )	NSTBY = H, EN_BOOST = H Autoload OFF		750	<b>1300</b>	μA
V <sub>DDA</sub>	Output voltage of internal LDO	I <sub>VDDA</sub> = 1mA		2.80		V
			<b>-3</b>		<b>+3</b>	%
V <sub>REF</sub>	Reference voltage (Note 11)			1.23		V

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** All voltages are with respect to the potential at the GND pins.

**Note 3:** Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub>=150°C (typ.) and disengages at T<sub>J</sub>=130°C (typ.).

**Note 4:** For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package

**Note 5:** The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

**Note 6:** In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A-MAX</sub>) is dependent on the maximum operating junction temperature (T<sub>J-MAX-OP</sub> = 125°C), the maximum power dissipation of the device in the application (P<sub>D-MAX</sub>), and the junction-to ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A-MAX</sub> = T<sub>J-MAX-OP</sub> - (θ<sub>JA</sub> × P<sub>D-MAX</sub>).

**Note 7:** Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

**Note 8:** Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

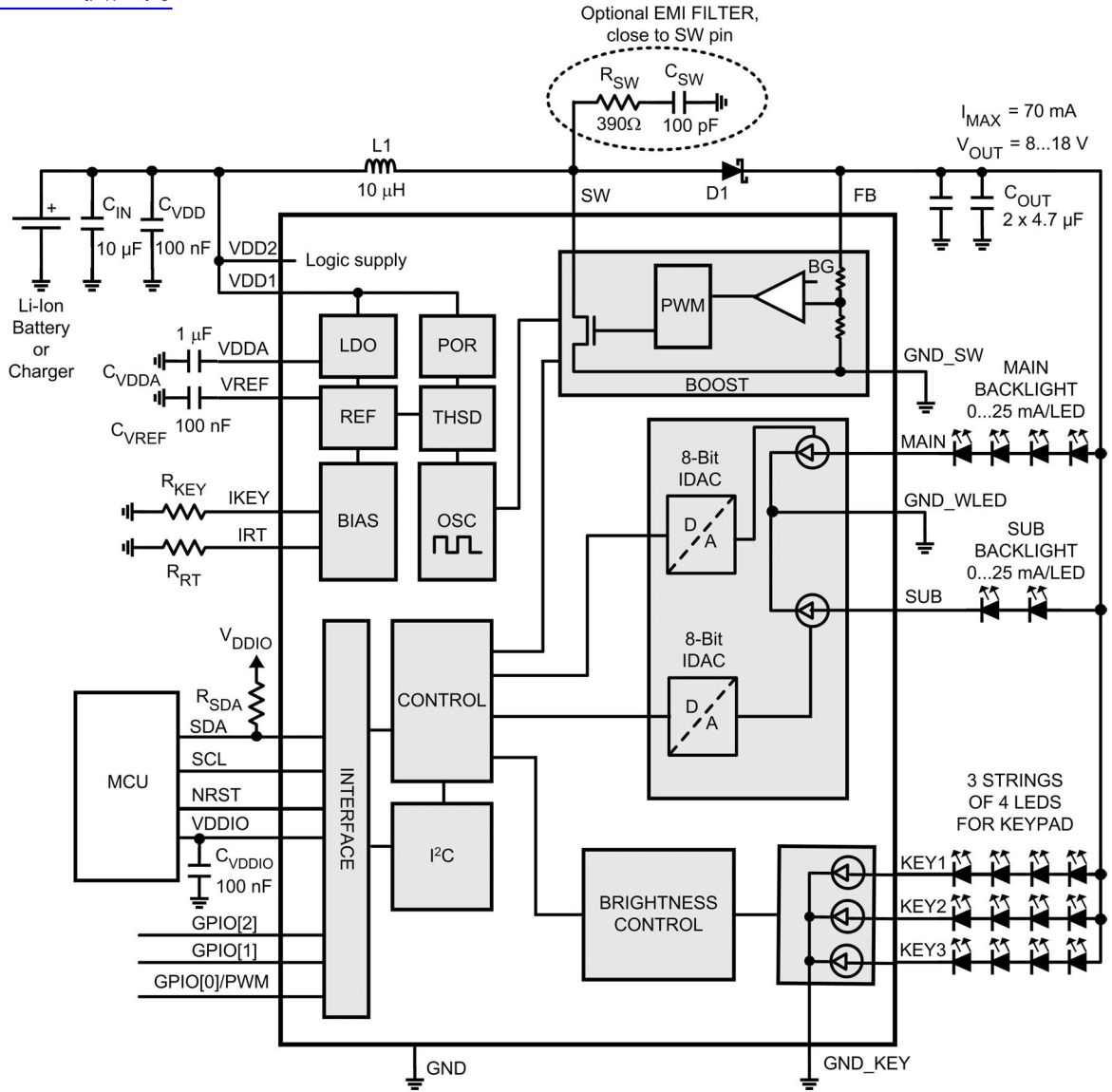
**Note 9:** Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

**Note 10:** Boost output voltage set to 8V (08H in register 0DH) to prevent any unnecessary current consumption.

**Note 11:** No external loading allowed for V<sub>REF</sub> pin.

# Block Diagram

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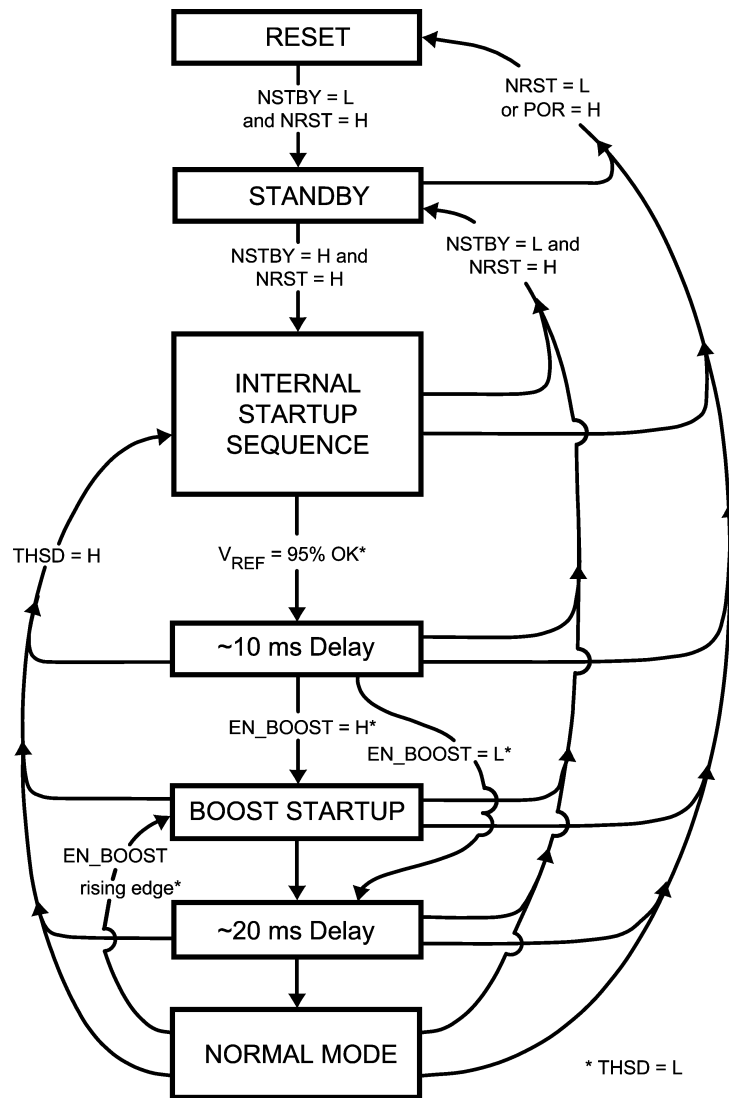


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# Modes of Operation

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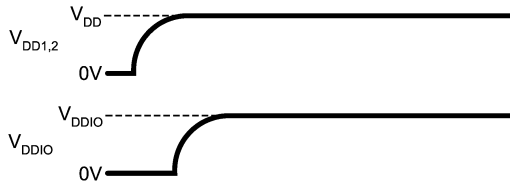
- RESET:** In the RESET mode all the internal registers are reset to the default values. Reset is entered always if input NRST is LOW or internal Power On Reset is active. Power On Reset (POR) will activate during the chip startup or when the supply voltages  $V_{DD1}$  and  $V_{DD2}$  fall below 1.5V. Once  $V_{DD1}$  and  $V_{DD2}$  rises above 1.5V, POR will inactivate and the chip will continue to the STANDBY mode. NSTBY control bit is low after POR by default.
- STANDBY:** The STANDBY mode is entered if the register bit NSTBY is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after start up.
- STARTUP:** When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks ( $V_{REF}$ , Bias, Oscillator etc.). To ensure the correct oscillator initialization, a 10ms delay is generated by the internal state-machine. If the chip temperature rises too high, the Thermal Shutdown (THSD) disables the chip operation and STARTUP mode is entered until no thermal shutdown event is present.
- BOOST STARTUP:** Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in low current PWM mode during the 20ms delay generated by the state-machine. All LED outputs are off during the 20ms delay to ensure smooth startup. The Boost startup is entered from Internal Startup Sequence if EN\_BOOST is HIGH or from Normal mode when EN\_BOOST is written HIGH.
- NORMAL:** During NORMAL mode the user controls the chip using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write.



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## Power-Up Sequence

When powering up the device,  $V_{DD1}$  and  $V_{DD2}$  should be greater than  $V_{DDIO}$  to prevent any damage to the device.



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## Magnetic Boost DC/DC Converter

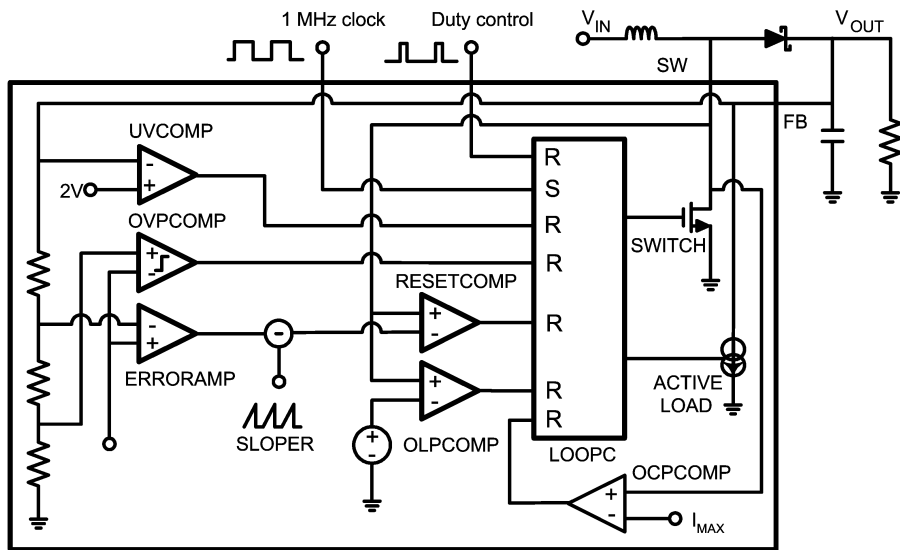
The LP3958 Boost DC/DC Converter generates an 8...18V supply voltage for the LEDs from single Li-Ion battery (3V...4.5V). The output voltage is controlled with an 8-bit register in 10 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. Switching frequency is 1MHz, when timing resistor  $R_T$  is 82k $\Omega$ . Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and KEY timings.

EMI filter ( $R_{SW}$  and  $C_{SW}$ ) on the SW pin can be used to suppress EMI caused by fast switching. These components should be as near as possible to the SW pin to ensure reliable operation. The LP3958 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is

fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. Active load can be disabled with the EN\_AUTOLOAD bit. Disabling active load will increase slightly the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped when there is no load to minimise the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop. The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
  - Keeps the output below breakdown voltage.
  - Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
  - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.



Boost Converter Topology

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# Magnetic Boost DC/DC Converter (Continued)

## MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{LOAD}$	Maximum Continuous Load Current	$3.0V = V_{IN}$ $V_{OUT} = 18V$			70	mA
$V_{OUT}$	Output Voltage Accuracy (FB Pin)	$3.0V \leq V_{IN} \leq 5.5V$ $V_{OUT} = 18V$	-3.5		+3.5	%
$RDS_{ON}$	Switch ON Resistance	$I_{SW} = 0.5A$		0.15	0.3	$\Omega$
$f_{PWM}$	PWM Mode Switching Frequency	$RT = 82 k\Omega$		1.0		MHz
	Frequency Accuracy	$RT = 82 k\Omega$	-7 -9		+7 +9	%
$t_{PULSE}$	Switch Pulse Minimum Width	no load		45		ns
$t_{STARTUP}$	Startup Time	Boost startup from STANDBY to $V_{OUT} = 18V$ , no load		15		ms
$I_{MAX}$	SW Pin Current Limit			800	1150	mA

### BOOST STANDBY MODE

User can set the Boost Converter to STANDBY mode by writing the register bit EN\_BOOST low. When EN\_BOOST is written high, the converter starts for 20ms in low current PWM mode and then goes to normal PWM mode. All LED outputs are off during the 20ms delay to ensure smooth startup.

### BOOST OUTPUT VOLTAGE CONTROL

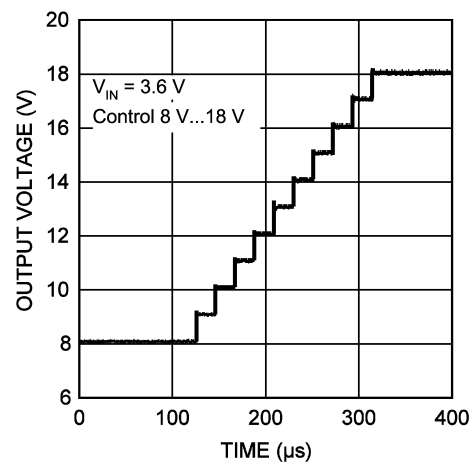
User can control the boost output voltage by Boost Output 8-bit register.

Boost Output [7:0] Register 0DH		Boost Output Voltage (typical)
Bin	Dec	
0000 1000	8	8.0V
0000 1001	9	9.0V
0000 1010	10	10.0V
0000 1011	11	11.0V
0000 1100	12	12.0V
0000 1101	13	13.0V
0000 1110	14	14.0V
0000 1111	15	15.0V
0001 0000	16	16.0V
0001 0001	17	17.0V
0001 0010	18	18.0V

If register value is lower than 8, then value of 8 is used internally.

If register value is higher than 18, then value of 18 is used internally.

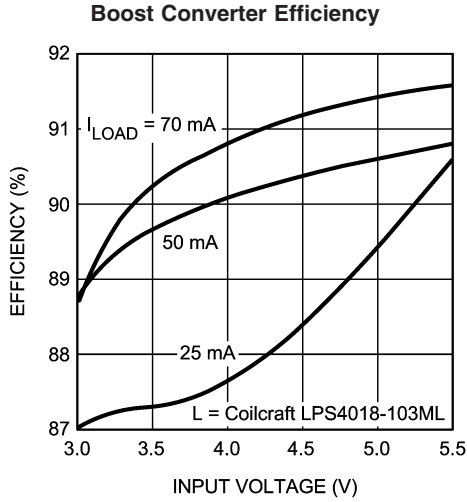
Boost Output Voltage Control



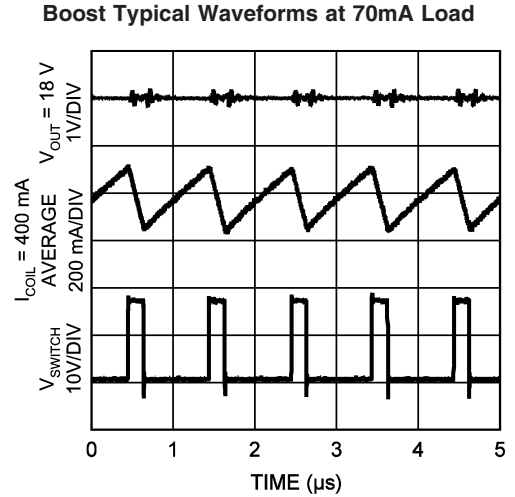
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# Boost Converter Typical Performance Characteristics

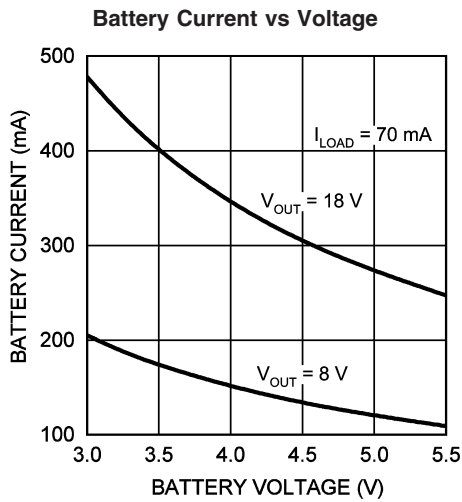
$V_{IN} = 3.0V$ ,  $V_{OUT} = 18V$  if not otherwise stated



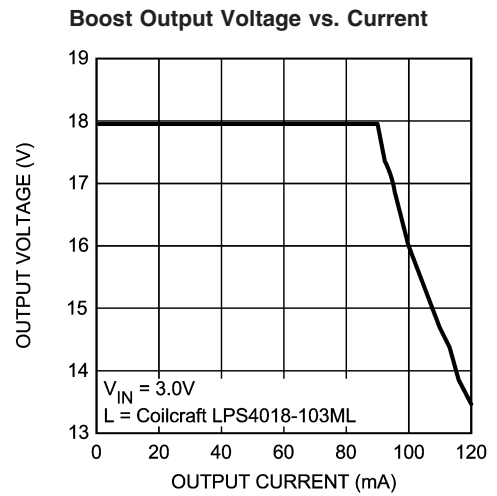
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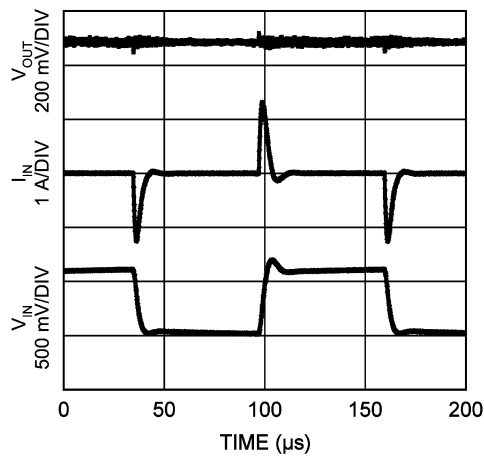


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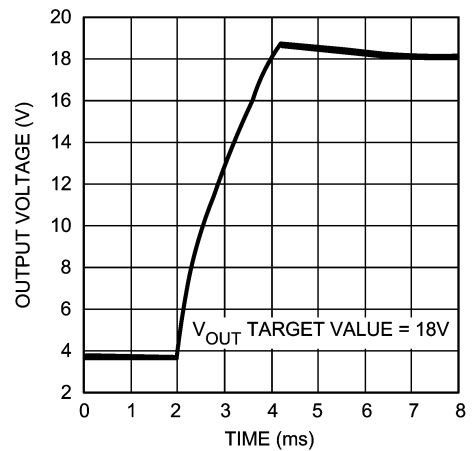
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### Boost Line Regulation 3.0V - 3.6V, no load



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### Boost Turn On Time with No Load

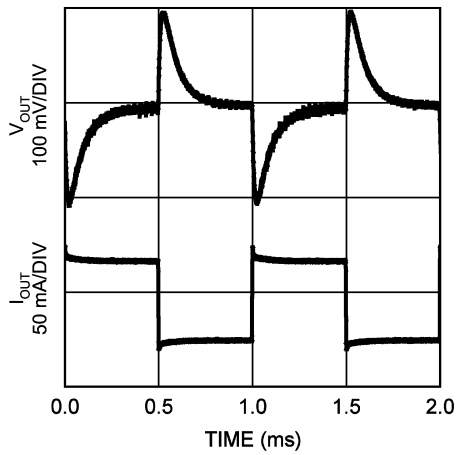


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# Boost Converter Typical Performance Characteristics (Continued)

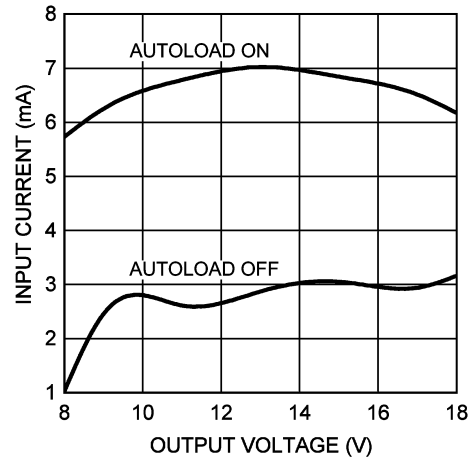
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**Boost Load Transient Response 25mA – 70mA**



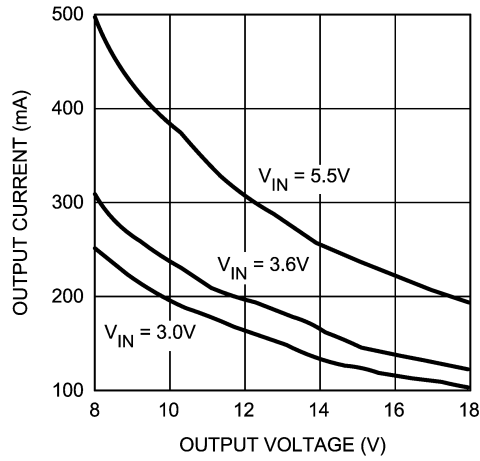
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**Autoload Effect on Input Current, No Load**



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**Boost Maximum Current vs. Output Voltage**



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## Functionality of Keypad LED Outputs (KEY1, KEY2, KEY3)

LP3958 has three individual keypad LED output pins. Output pins can be used in switch mode or constant current mode. Output mode can be selected with the control register (address 00H) bit CC\_SW. If the bit is set high, then keypad LED outputs are in switch mode, otherwise in constant current mode. These modes are described later in separate chapters.

Keypad LED output control can be done in three ways:

1. Defining the expected balance and brightness in Keypad register (address 01H)
2. Direct setting each LED ON/OFF via Keypad control register (address 00H)
3. External PWM control

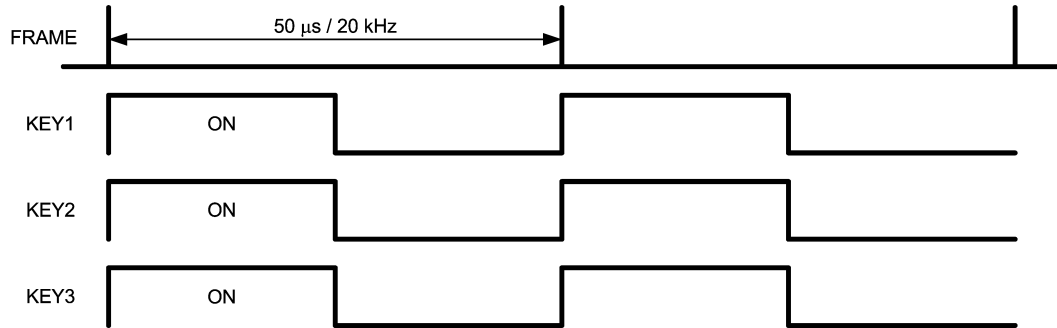
### BRIGHTNESS CONTROL WITH KEYPAD REGISTER

If the keypad LED output is used by defining the balance and brightness in the Keypad register, then one needs to set EN\_KEYP bit high and KEYP\_PWM bit high in the Control register (address 00H). K1SW, K2SW and K3SW are used to enable each LED output, enabled when written high. CC\_SW defines the LED output mode. A single register is used for defining the balance and brightness for keypad LED output:

KEYPAD REGISTER (01H)		
Name	Bit	Description
BALANCE[2:0]	6:4	Balance of KEY1, KEY2 and KEY3 outputs
BRIGHT[2:0]	3:1	Brightness control
OVL	0	Overlapping mode selection: 0 = non-overlapping mode 1 = overlapping mode

### OVERLAPPING MODE

The brightness is controlled using PWM duty cycle based control method as the following figure shows.



Overlapping Mode

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Since KEY outputs are on simultaneously, the maximum load peak current is:

$$I_{MAX} = I(K1)_{MAX} + I(K2)_{MAX} + I(K3)_{MAX}$$

### NON-OVERLAPPING MODE

The timing diagram shows the splitted KEY1, KEY2 and KEY3 and brightness control effect to splitted parts. Full brightness is used in the diagram. If for example 1/2 brightness is used, the frame is still 50μs, but all LED outputs' ON time is 50% shorter and at the last 25μs all LED outputs are OFF.

Brightness control is logarithmic and is programmed as follows:

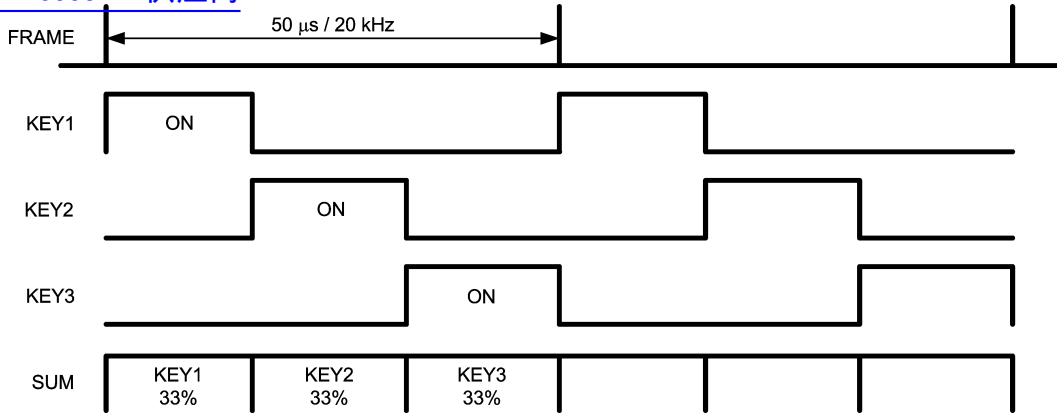
Bright[2:0]	Brightness [%]	Ratio to max brightness
000	0	0
001	1.56	1/64
010	3.12	1/32
011	6.25	1/16
100	12.5	1/8
101	25	1/4
110	50	1/2
111	100	1/1

The LED balance can be selected as follows. This is valid only in non-overlapping mode.

Balance [2:0]	KEY1 active [%]	KEY2 active [%]	KEY3 active [%]
000	100	0	0
001	0	100	0
010	0	0	100
011	50	50	0
100	0	50	50
101	50	0	50
110	33	33	33
111	50	25	25

## Functionality of Keypad LED Outputs (KEY1, KEY2, KEY3) (Continued)

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Non-overlapping Mode

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The non-overlapping mode has 8-programmed balance ratios. Since the KEY1, KEY2 and KEY3 are split in to non-overlapping slots the output current through the keypad LED can be calculated by following equation:

$$I_{AVG} = (C_{KEY1} \times I_{KEY1} + C_{KEY2} \times I_{KEY2} + C_{KEY3} \times I_{KEY3}) \times B$$

where

C = Balance [%] (see table of balance control earlier)

B = Brightness [%] (see table of Brightness Control)

### LED ON/OFF CONTROL WITH KEYPAD CONTROL REGISTER

Each LED output can be set ON by writing the corresponding bit high in the control register. K1SW controls KEY1, K2SW controls KEY2 and K3SW controls KEY3 output. Note that EN\_KEYP bit must be high and KEYP\_PWM bit low. In this mode, the KEYPAD register does not have any effect. CC\_SW bit in control register defines the LED output mode.

#### Switch Mode / Constant Current Mode

Each keypad LED output can be set to act as a switch or a constant current sink. Selection of mode is done with the CC\_SW bit in the Control Register. If bit is set high, then the switch mode is selected. Default is switch mode.

#### 1. SWITCH MODE

In switch mode, the keypad LED outputs are low ohmic switches to ground. Resistance is typically 3.5Ω. **External ballast resistors must be used to limit the current through the LED.**

#### 2. CONSTANT CURRENT MODE

In constant current mode, the maximum output current is defined with a single external resistor ( $R_{KEY}$ ) and the maximum current control register (address 02H).

KEYPAD MAX CURRENT REGISTER (02H)		
Name	Bit	Description
IK1[1:0]	5:4	KEY1 maximum current
IK2[1:0]	3:2	KEY2 maximum current
IK3[1:0]	1:0	KEY3 maximum current

Maximum current for each LED output is adjusted with the Keypad max current register in following way:

IK1[1:0], IK2[1:0], IK3[1:0]	Maximum current / output
00	$0.25 \times I_{MAX}$
01	$0.50 \times I_{MAX}$
10	$0.75 \times I_{MAX}$
11	$1.00 \times I_{MAX}$

External ballast resistors are not needed in this mode. The maximum current for all keypad LED drivers is set with  $R_{KEY}$ . The equation for calculating the maximum current is:

$$I_{MAX} = 100 \times 1.23V / (R_{KEY} + 50 \Omega)$$

where

$I_{MAX}$  = maximum KEY current in any KEY output (during constant current mode)

1.23V = reference voltage

100 = internal current mirror multiplier

$R_{KEY}$  = resistor value in Ohms

50 Ω = Internal resistor in the  $I_{KEY}$  input

Table with example resistance values and corresponding output currents:

KEY resistor $R_{KEY}$ (kΩ)	Maximum current / output $I_{MAX}$ (mA)
8.2	14.9
9.1	13.4
10	12.2
12	10.2
15	8.2
18	6.8
24	5.1

Note that the LED output requires a minimum saturation voltage in order to act as a true constant current sink. The saturation voltage minimum is typically 100mV. If the LED output voltage drops below 100mV, then the current will decrease significantly.

## Functionality of Keypad LED Outputs (KEY1, KEY2, KEY3) (Continued)

### External PWM Control

The GPIO[0]/PWM pin can be used to control the KEY output. PWM function for the pin is selected by writing EN\_PWM\_PIN high in GPIO control register (address 06H). Note, that EN\_KEYP bit must be set high. Each LED output can be enabled with K1SW, K2SW and K3SW bits. EN\_EXT\_K1\_PWM, EN\_EXT\_K2\_PWM and EN\_EXT\_K3\_PWM bits are used to select, which LED outputs are controlled with the external PWM input. Note that

polarity of external PWM control is active high i.e. when high, then LED output is enabled. If KEYP\_PWM is set low, then each selected LED output is controlled directly with external PWM input. If KEYP\_PWM is set high, then internal PWM control is modulated by the external PWM input. In latter case, internal PWM control is passed to LED when external PWM input is high.

### Keypad LEDs Driver Performance Characteristics

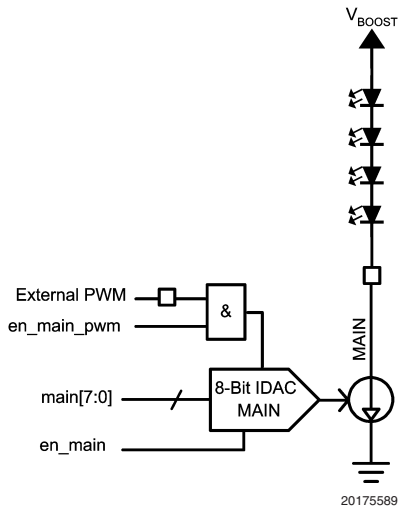
Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	KEY1, KEY2, KEY3 pin leakage current				1	$\mu A$
$I_{MAX(KEY)}$	Maximum recommended sink current	CC mode			15	mA
		SW mode			60	mA
	Accuracy @ 15mA	CC mode		5		%
	Current mirror ratio	CC mode		1:100		
	KEY current matching error	$I_{KEY}$ set to 15mA, CC mode		3		%
$R_{SW}$	Switch resistance	SW mode		3.5		$\Omega$
$f_{KEY}$	KEY internal PMW switching frequency	Accuracy same as internal clock frequency accuracy		20		kHz
$V_{SAT}$	Saturation voltage (current drop 10%)	$I_{KEY}$ set to 15mA		100	500	mV

**Note:** KEY current should be limited as follows:  
**constant current mode** – limited by external  $R_{KEY}$  resistor  
**switch mode** – limited by external ballast resistors

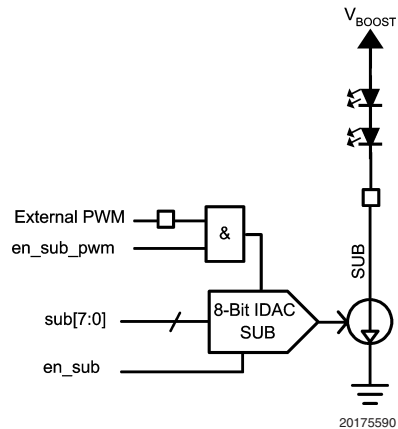
# Backlight Drivers

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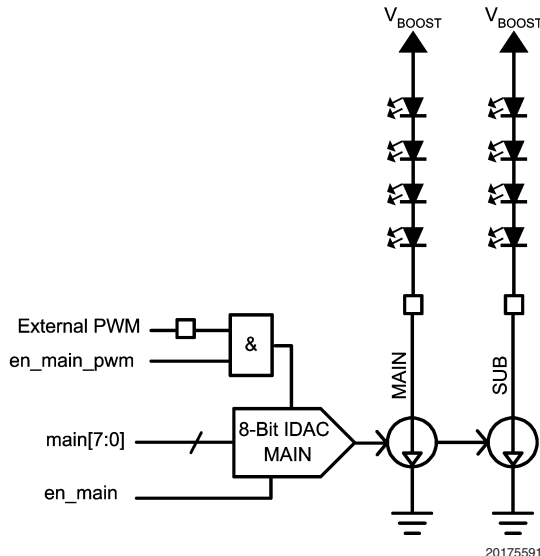
LP3958 has 2 independent backlight drivers. Both drivers are regulated constant current sinks. LED current for both LED strings are controlled by the 8-bit current mode DACs with 0.1 mA step. MAIN and SUB LEDs can be also controlled with one DAC (MAIN) for better matching allowing the use of larger displays having up to 8 white LEDs by setting DISPL bit to 1.



20175589  
MAIN output for 4 LEDs (DISPL = 0)



20175590  
SUB output for 2 LEDs (DISPL = 0)



20175591  
MAIN and SUB outputs for 8 LEDs (DISPL = 1)

## PWM CONTROL

External PWM control is enabled by writing 1 to EN\_MAIN\_PWM and/or EN\_SUB\_PWM bits in register address 2BH. GPIO[0] pin is used as external PWM input when EN\_PWM\_PIN is set high. PWM input is active high, i.e. LED is activated when in high state.

## Backlight Drivers (Continued)

### FADE IN / FADE OUT

LP3958 has an automatic fade in and out for main and sub backlight. The fade function is enabled with EN\_FADE bit. The slope of the fade curve is set by the SLOPE bit. Fade control for main and sub display is set by FADE\_SEL bit.

Recommended fading sequence:

1. ASSUMPTION: Current WLED value in register
2. Set SLOPE
3. Set FADE\_SEL
4. Set EN\_FADE = 1
5. Set target WLED value
6. Fading will be done either within 0.65s or 1.3s based on SLOPE selection

Fading times apply to full scale change i.e. from 0 to 100% or vice versa. If the current change does not correspond to full scale change, the time will be respectively shorter. See WLED Dimming diagrams for typical fade times.

WLED CONTROL REGISTER (03H)		
Name	Bit	Description
SLOPE	5	FADE execution time: 0 = 1.3s (full scale) 1 = 0.65s (full scale)
FADE_SEL	4	FADE selection: 0 = FADE controls MAIN 1 = FADE controls SUB
EN_FADE	3	FADE enable 0 = FADE disabled 1 = FADE enabled
DISPL	2	Display mode: 0 = MAIN and SUB individual control 1 = MAIN and SUB controlled with MAIN DAC
EN_MAIN	1	MAIN enable: 0 = disable 1 = enable
EN_SUB	0	SUB enable: 0 = disable 1 = enable

**Note:** if DISPL=1 and FADE\_SEL=0 then FADE effects MAIN and SUB

Adjustment is made with 04H (main current) and with 05H (sub current) registers:

MAIN CURRENT [7:0] SUB CURRENT [7:0]	Driver current, mA (typical)
0000 0000	0
0000 0001	0.1
0000 0010	0.2
0000 0011	0.3
...	...
...	...
1111 1101	25.3
1111 1110	25.4
1111 1111	25.5

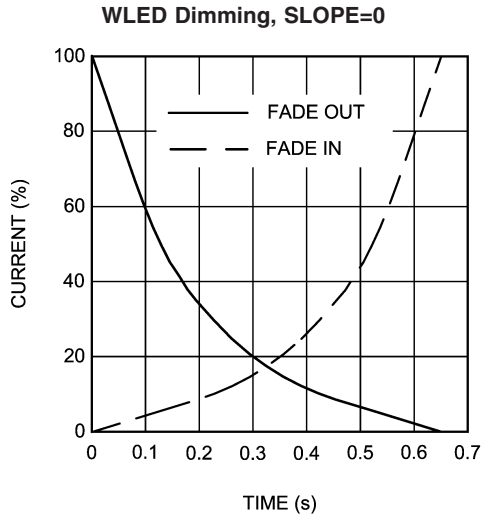


# Backlight Driver Electrical Characteristics

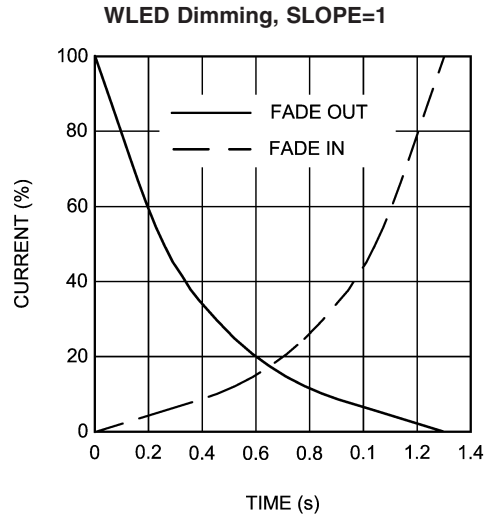
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Symbol	Parameter	Conditions	Min	Typical	Max	Units
$I_{MAX}$	Maximum Sink Current			25.5	<b>30</b>	mA
$I_{LEAKAGE}$	Leakage Current	$V_{SUB, MAIN} = 18V$		0.03	<b>1</b>	$\mu A$
$I_{MAIN}$ $I_{SUB}$	MAIN Current tolerance SUB Current tolerance	$I_{MAIN}$ and $I_{SUB}$ set to 12.8mA (80H)	<b>11.1</b>	12.8	<b>14.1</b>	mA
$Match_{MAIN-SUB}$	Sink Current Matching Error	$I_{SINK} = 12.8mA$ , DISPL=1		0.2		%
$Match_{MAIN-SUB}$	Sink Current Matching Error	$I_{SINK} = 12.8mA$ , DISPL=0		5		%
$V_{SAT}$	95% Saturation Voltage	$I_{SINK} = 25mA$		400	600 <b>800</b>	mV

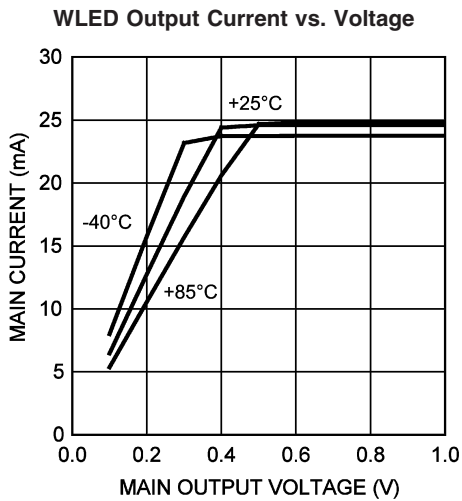
Note: Matching is the maximum difference from the average.



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## General Purpose I/O Functionality

LP3958 has three general purpose I/O pins: GPIO[0]/PWM, GPIO[1] and GPIO[2]. GPIO[0]/PWM can also be used as a PWM input for the external LED PWM controlling. GPIO bi-directional drivers are operating from the  $V_{DDIO}$  supply domain.

Registers for GPIO are as follows:

GPIO CONTROL (06H)		
Name	Bit	Description
EN_PWM_PIN	4	Enable PWM pin 0 = disable 1 = enable
OEN[2:0]	2:0	GPIO pin direction 0 = input 1 = output

## Logic Interface Characteristics

( $V_{DDIO} = 1.65V \dots V_{DD1,2}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LOGIC INPUT SCL, SDA, GPIO[0:2]</b>						
$V_{IL}$	Input Low Level				$0.2 \times V_{DDIO}$	V
$V_{IH}$	Input High Level		$0.8 \times V_{DDIO}$			V
$I_I$	Logic Input Current		-1.0		1.0	$\mu A$
$f_{SCL}$	Clock Frequency				400	kHz
<b>LOGIC INPUT NRST</b>						
$V_{IL}$	Input Low Level				0.5	V
$V_{IH}$	Input High Level		1.2			V
$I_I$	Input Current		-1.0		1.0	$\mu A$
$t_{NRST}$	Reset Pulse Width		10			$\mu s$
<b>LOGIC OUTPUT SDA</b>						
$V_{OL}$	Output Low Level	$I_{SDA} = 3mA$		0.3	0.5	V
$V_{OH}$	Output High Level	$I_{SDA} = -3mA$	$V_{DDIO} - 0.5$	$V_{DDIO} - 0.3$		
$I_L$	Output Leakage Current	$V_{SDA} = 2.8V$			1.0	$\mu A$
<b>LOGIC OUTPUT GPIO[0:2]</b>						
$V_{OL}$	Output Low Level	$I_{GPIO} = 3mA$		0.3	0.5	V
$V_{OH}$	Output High Level	$I_{GPIO} = -3mA$	$V_{DDIO} - 0.5$	$V_{DDIO} - 0.3$		V
$I_L$	Output Leakage Current	$V_{GPIO} = 2.8V$			1.0	$\mu A$

### GPIO DATA (07H)

Name	Bit	Description
DATA[2:0]	2:0	Data bits

GPIO control register is used to set the direction of each GPIO pin. For example, by setting OEN0 bit high the GPIO[0]/PWM pin acts as a logic output pin with data defined DATA0 in GPIO data register. Note, that the EN\_PWM\_PIN bit overrides OEN0 state by forcing GPIO[0]/PWM to act as PWM input. GPIO[1] and GPIO[2] pins can be selected to be inputs or outputs, defined by OEN1 and OEN2 bit status. PWM functionality is valid only for GPIO[0]/PWM pin. GPIO data register contains the data of GPIO pins. When output direction is selected to GPIO pin, then GPIO data register defines the output pin state. When GPIO data register is read, it contains the state of the pin despite of the pin direction.

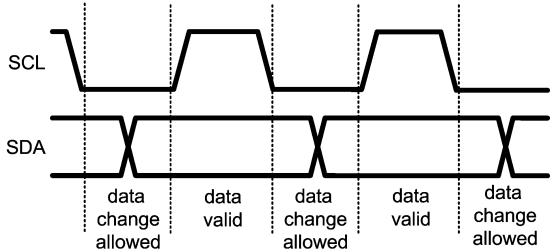
# I<sup>2</sup>C Compatible Interface

## I<sup>2</sup>C SIGNALS [查询"LP3958TL"供应商](#)

The SCL pin is used for the I<sup>2</sup>C clock and the SDA pin is used for bidirectional data transfer. Both these signals need a pull-up resistor according to I<sup>2</sup>C specification.

### I<sup>2</sup>C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

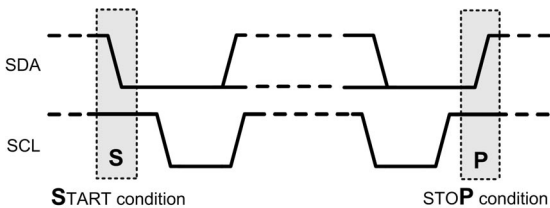


I<sup>2</sup>C Signals: Data Validity

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### I<sup>2</sup>C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I<sup>2</sup>C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I<sup>2</sup>C master always generates START and STOP bits. The I<sup>2</sup>C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I<sup>2</sup>C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



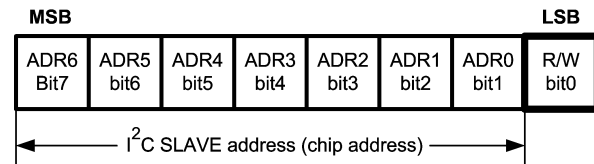
I<sup>2</sup>C Start and Stop Conditions

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### TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9<sup>th</sup> clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I<sup>2</sup>C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3958 address is 59H (101 1001b). For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. This means that the first byte is B2H for WRITE and B3H for READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.



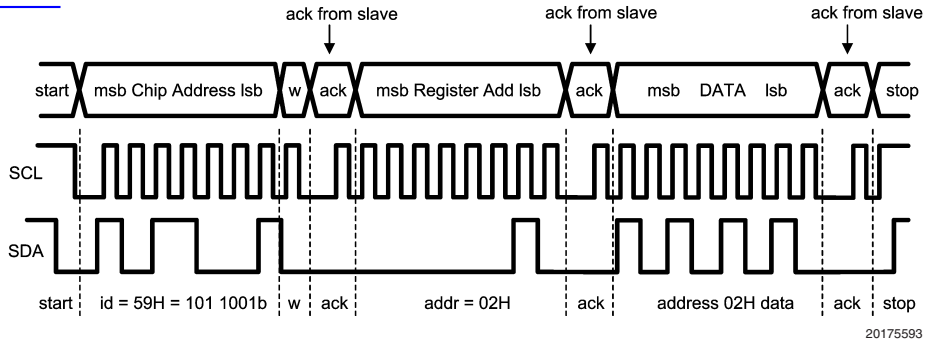
I<sup>2</sup>C Chip Address

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Register changes take an effect at the SCL rising edge during the last ACK from slave.

# I<sup>2</sup>C Compatible Interface (Continued)

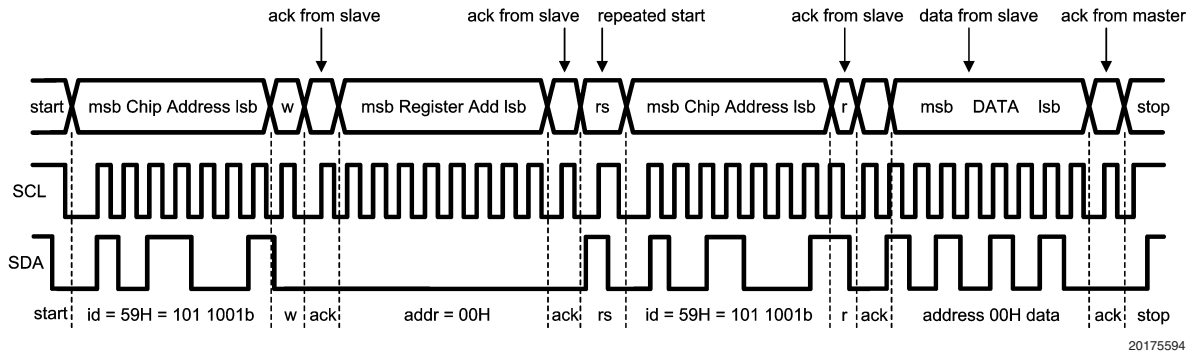
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w = write (SDA = "0")  
 r = read (SDA = "1")  
 ack = acknowledge (SDA pulled down by either master or slave)  
 rs = repeated start  
 id = 7-bit chip address, 59H (101 1001b) for LP3958.

## I<sup>2</sup>C Write Cycle

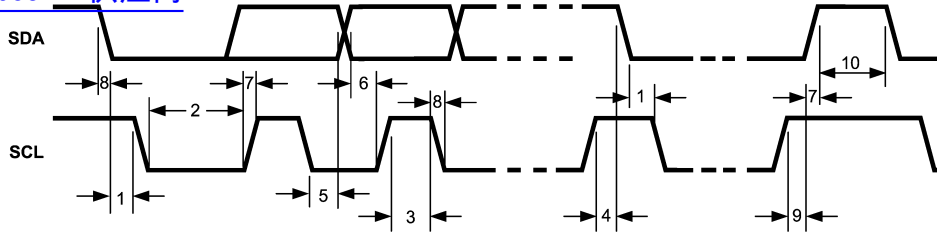
When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.



## I<sup>2</sup>C Read Cycle

I<sup>2</sup>C Compatible Interface (Continued)

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I<sup>2</sup>C Timing Diagram

I<sup>2</sup>C TIMING PARAMETERS ( $V_{DD1,2} = 3.0$  to  $4.5V$ ,  $V_{DDIO} = 1.8V$  to  $V_{DD1,2}$ )

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		$\mu s$
2	Clock Low Time	1.3		$\mu s$
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LP3958)	300	900	ns
5	Data Hold Time (Input direction, delay generated by Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		$\mu s$
$C_b$	Capacitive Load for Each Bus Line	10	200	pF

NOTE: Data guaranteed by design

## Recommended External Components

### OUTPUT CAPACITOR, $C_{OUT}$

The output capacitor  $C_{OUT}$  directly affects the magnitude of the output ripple voltage. In general, the higher the value of  $C_{OUT}$ , the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower  $V_{OUT}$  ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower  $V_{OUT}$  ripple magnitude than the tantalums of the same value. However, the  $dv/dt$  of the  $V_{OUT}$  ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 25V or greater is recommended. Examples of suitable capacitors are: TDK C3216X5R1E475K, Panasonic ECJ3YB1E475K, ECJMFB1E475K and ECJ4YB1E475K.

**Some ceramic capacitors, especially those in small packages, exhibit a strong capacitance reduction with the increased applied voltage (DC bias effect). The capacitance value can fall below half of the nominal capacitance. Too low output capacitance can make the boost converter unstable. Output capacitors DC bias effect should be better than -50% at 18V.**

### INPUT CAPACITOR, $C_{IN}$

The input capacitor  $C_{IN}$  directly affects the magnitude of the input ripple voltage and to a lesser degree the  $V_{OUT}$  ripple. A higher value  $C_{IN}$  will give a lower  $V_{IN}$  ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

### OUTPUT DIODE, $D_1$

A schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current (800mA) to ensure reliable operation.

Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown voltage of the schottky diode significantly larger (~30V) than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer. Example of suitable diode is: Central Semiconductor CMMSH1-40.

### EMI FILTER COMPONENTS $C_{SW}$ , $R_{SW}$

EMI filter ( $R_{SW}$  and  $C_{SW}$ ) on the SW pin can be used to suppress EMI caused by fast switching. These components should be as near as possible to the SW pin to ensure reliable operation. 50V or greater voltage rating is recommended for capacitor.

### INDUCTOR, $L_1$

A 10uH shielded inductor is suggested for LP3958 boost converter. The inductor should have a saturation current rating higher than the rms current it will experience during circuit operation (600mA). Less than 300mΩ ESR is suggested for high efficiency and sufficient output current. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Examples of suitable inductors are: TDK VLF4012AT-100MR79, VLF4018BT-100MR90, VLF5014AT-100MR92, Coilcraft LPS4018-103ML.

### LIST OF RECOMMENDED EXTERNAL COMPONENTS

Symbol	Symbol explanation	Value	Unit	Type
$C_{VDD}$	C between VDD1,2 and GND	100	nF	Ceramic, X7R / X5R
$C_{VDDIO}$	C between VDDIO and GND	100	nF	Ceramic, X7R / X5R
$C_{VDDA}$	C between VDDA and GND	1	μF	Ceramic, X7R / X5R
$C_{OUT}$	C between FB and GND	2 x 4.7 or 1 x 10	μF	Ceramic, X7R / X5R, tolerance +/-10%
	Maximum DC bias effect @ 18V	-50	%	
$C_{IN}$	C between battery voltage and GND	10	μF	Ceramic, X7R / X5R
$L_1$	L between SW and $V_{BAT}$	10	μH	Shielded inductor, low ESR
	Saturation current	600	mA	
$C_{VREF}$	C between $V_{REF}$ and GND	100	nF	Ceramic, X7R / X5R
$R_{KEY}$	R between $I_{KEY}$ and GND	8.2	kΩ	±1%
$R_{RT}$	R between $I_{RT}$ and GND	82	kΩ	±1%
$D_1$	Rectifying diode ( $V_f$ @ maxload)	0.3-0.5	V	Schottky diode
	Reverse voltage	30	V	
	Repetitive peak current	800	mA	
$C_{SW}$	C in EMI filter	100	pF	Ceramic, X7R / X5R, 50V
$R_{SW}$	R in EMI filter	390	Ω	±1%
LEDs				User Defined

Note: See Application Note AN-1436 "Design and Programming Examples for Lighting Management Unit LP3958" for more information on how to design with LP3958

LP3958 Control Register Names and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00	Control Register	KEYP_PWM 0	EN_KEYP 0	CC_SW 1		K1SW 0	K2SW 0	K3SW 0	
01	Keypad			BALANCE[2:0] 0			BRIGHT[2:0] 0		OVL 0
02	Keypad Max Current			IK1[1:0] 0	IK2[1:0] 0	IK3[1:0] 0			
03	WLED Control			SLOPE 0	FADE_SEL 0	EN_FADE 0	DISPL 0	EN_MAIN 0	EN_SUB 0
04	MAIN Current					MAIN[7:0] 0			
05	SUB Current					SUB[7:0] 0			
06	GPIO Control				EN_PWM_PIN 0			OEN[2:0] 0	
07	GPIO Data							DATA[2:0] 0	
0B	Enables		NSTBY 0	EN_BOOST 0			EN_AUTOLOAD 1		
0D	Boost Output					BOOST[7:0] 1			
2B	PWM Enable				EN_EXT_K1_PWM 0	EN_EXT_K2_PWM 0	EN_EXT_K3_PWM 0	EN_MAIN_PWM 0	EN_SUB_PWM 0

## LP3958 Register Bit Explanations

Each register is shown with a key indicating the accessibility of the each individual bit, and the initial condition:

### Register Bit Accessibility and Initial Condition

Key	Bit Accessibility
RW	Read/write
R	Read only
-0,-1	Condition after POR

### CONTROL REGISTER (00H) – KEYPAD LEDS CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>KEYP_PWM</b>	<b>EN_KEYP</b>	<b>CC_SW</b>		<b>K1SW</b>	<b>K2SW</b>	<b>K3SW</b>	
RW - 0	RW - 0	RW - 1	R - 0	RW - 0	RW - 0	RW - 0	R - 0

<b>KEYP_PWM</b>	Bit 7	0 - Internal KEYPAD PWM control disabled 1 - Internal KEYPAD PWM control enabled
<b>EN_KEYP</b>	Bit 6	0 - KEYPAD outputs disabled 1 - KEYPAD outputs enabled
<b>CC_SW</b>	Bit 5	0 - Constant current sink mode 1 - Switch mode
<b>K1SW</b>	Bit 3	0 - KEYPAD1 disabled 1 - KEYPAD1 enabled
<b>K2SW</b>	Bit 2	0 - KEYPAD2 disabled 1 - KEYPAD2 enabled
<b>K3SW</b>	Bit 1	0 - KEYPAD3 disabled 1 - KEYPAD3 enabled

### KEYPAD (01H) – KEYPAD BALANCE AND BRIGHTNESS CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
	<b>BALANCE[2:0]</b>			<b>BRIGHT[2:0]</b>			<b>OVL</b>
R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>BALANCE[2:0]</b>	Bits 6-4	PWM balance for KEYPAD outputs
<b>BRIGHT[2:0]</b>	Bits 3-1	PWM brightness control for KEYPAD outputs
<b>OVL</b>	Bit 0	0 - Overlapping mode disabled 1 - Overlapping mode enabled



## LP3958 Register Bit Explanations (Continued)

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### KEYPAD MAX CURRENT (02H) – MAXIMUM KEYPAD CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		<b>IK1[1:0]</b>		<b>IK2[1:0]</b>		<b>IK3[1:0]</b>	
R - 0	R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

Maximum current for KEY1,2,3 driver	
IK1,2,3[1:0]	Maximum output current
00	$0.25 \times I_{MAX}$
01	$0.50 \times I_{MAX}$
10	$0.75 \times I_{MAX}$
11	$1.00 \times I_{MAX}$

### WLED CONTROL (03H) – WLED CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
		<b>SLOPE</b>	<b>FADE_SEL</b>	<b>EN_FADE</b>	<b>DISPL</b>	<b>EN_MAIN</b>	<b>EN_SUB</b>
R - 0	R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>SLOPE</b>	Bit 5	0 – fade execution time 0.65 sec (full scale) 1 – fade execution time 1.3 sec (full scale)
<b>FADE_SEL</b>	Bit 4	0 – fade control for MAIN 1 – fade control for SUB
<b>EN_FADE</b>	Bit 3	0 – automatic fade disabled 1 – automatic fade enabled
<b>DISPL</b>	Bit 2	0 - MAIN and SUB individual control 1 - MAIN and SUB controlled with MAIN DAC
<b>EN_MAIN</b>	Bit 1	0 – MAIN output disabled 1 – MAIN output enabled
<b>EN_SUB</b>	Bit 0	0 – SUB output disabled 1 – SUB output enabled

# LP3958 Register Bit Explanations (Continued)

## MAIN CURRENT (04H) – MAIN CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>MAIN[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

## SUB CURRENT (05H) – SUB CURRENT CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>SUB[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

MAIN, SUB current adjustment	
MAIN[7:0], SUB[7:0]	Typical driver current (mA)
0000 0000	0
0000 0001	0.1
0000 0010	0.2
0000 0011	0.3
0000 0100	0.4
...	...
1111 1101	25.3
1111 1110	25.4
1111 1111	25.5

## GPIO CONTROL (06H) – GPIO CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
			<b>EN_PWM_PIN</b>		<b>OEN[2:0]</b>		
R - 0	R - 0	R - 0	RW - 0	R - 0	RW - 0	RW - 0	RW - 0

<b>EN_PWM_PIN</b>	Bit 4	0 – External PWM pin disabled 1 – External PWM pin enabled
<b>OEN[2:0]</b>	Bits 2-0	0 – GPIO pin set as a input 1 – GPIO pin set as a output

## GPIO DATA (07H) – GPIO DATA REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
					<b>DATA[2:0]</b>		
R - 0	R - 0	R - 0	R - 0	R - 0	RW - 0	RW - 0	RW - 0

<b>DATA[2:0]</b>	Bits 2-0	GPIO data register bits
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## LP3958 Register Bit Explanations (Continued)

### ENABLES (0BH) – ENABLES REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
	<b>NSTBY</b>	<b>EN_BOOST</b>			<b>EN_AUTOLOAD</b>		
R - 0	RW - 0	RW - 0	R - 0	R - 0	RW - 1	R - 0	R - 0

<b>NSTBY</b>	Bit 6	0 – LP3958 standby mode 1 – LP3958 active mode
<b>EN_BOOST</b>	Bit 5	0 – Boost converter disabled 1 – Boost converter enabled
<b>EN_AUTOLOAD</b>	Bit 2	0 – Boost active load disabled 1 – Boost active load enabled

### BOOST OUTPUT (0DH) – BOOST OUTPUT VOLTAGE CONTROL REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
<b>BOOST[7:0]</b>							
RW - 0	RW - 0	RW - 0	RW - 0	RW - 1	RW - 0	RW - 0	RW - 0

<b>BOOST output voltage adjustment</b>	
<b>BOOST[7:0]</b>	<b>Typical boost output voltage (V)</b>
0000 1000	8.00
0000 1001	9.00
0000 1010	10.00
0000 1011	11.00
0000 1100	12.00
0000 1101	13.00
0000 1110	14.00
0000 1111	15.00
0001 0000	16.00
0001 0001	17.00
0001 0010	18.00

### PWM ENABLE (2BH) – EXTERNAL PWM CONTROL REGISTER

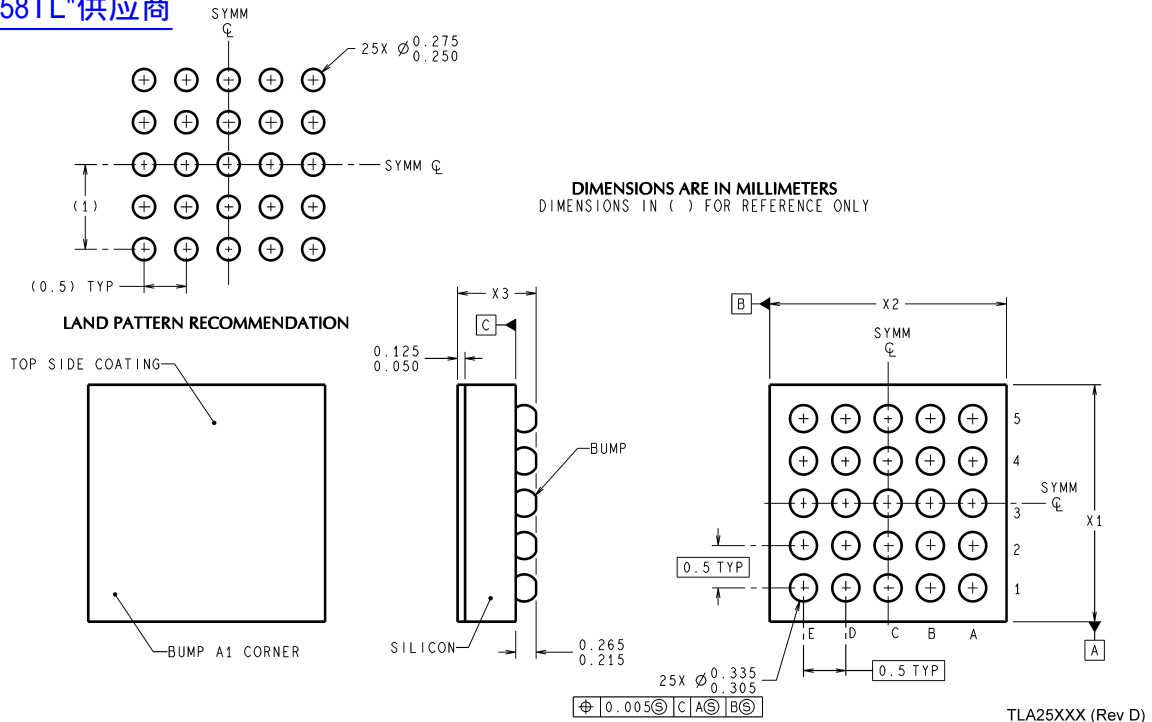
D7	D6	D5	D4	D3	D2	D1	D0
			<b>EN_EXT_K1_PWM</b>	<b>EN_EXT_K2_PWM</b>	<b>EN_EXT_K3_PWM</b>	<b>EN_MAIN_PWM</b>	<b>EN_SUB_PWM</b>
R - 0	R - 0	R - 0	RW - 0	RW - 0	RW - 0	RW - 0	RW - 0

<b>EN_EXT_K1_PWM</b>	Bit 4	0 – External PWM control for KEY1 disabled 1 – External PWM control for KEY1 enabled
<b>EN_EXT_K2_PWM</b>	Bit 3	0 – External PWM control for KEY2 disabled 1 – External PWM control for KEY2 enabled
<b>EN_EXT_K3_PWM</b>	Bit 2	0 – External PWM control for KEY3 disabled 1 – External PWM control for KEY3 enabled
<b>EN_EXT_MAIN_PWM</b>	Bit 1	0 – External PWM control for MAIN disabled 1 – External PWM control for MAIN enabled
<b>EN_EXT_SUB_PWM</b>	Bit 0	0 – External PWM control for SUB disabled 1 – External PWM control for SUB enabled

## Physical Dimensions

inches (millimeters) unless otherwise noted

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The dimension for X1, X2 and X3 are as given:

- X1=2.543mm ± 0.03mm
- X2=2.543mm ± 0.03mm
- X3=0.60mm ± 0.075mm

**25-bump micro SMD Package, 2.54 x 2.54 x 0.6mm, 0.5mm pitch**  
**NS Package Number TLA25CCA**

See Application note AN-1112 for PCB design and assembly instructions.

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