



September 2000
Revised August 2001

74VCX32244

Low Voltage 32-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

General Description

The VCX32244 contains thirty-two non-inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for 8-bit, 16-bit or full 32-bit operation.

The 74VCX32244 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74VCX32244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- t_{PD}
 - 2.5 ns max for 3.0V to 3.6V V_{CC}
 - 3.0 ns max for 2.3V to 2.7V V_{CC}
 - 6.0 ns max for 1.65V to 1.95V V_{CC}
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive (I_{OH}/I_{OL})
 - ± 24 mA @ 3.0V V_{CC}
 - ± 18 mA @ 2.3V V_{CC}
 - ± 6 mA @ 1.8V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 300 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Packages in plastic Fine-Pitch Ball Grid Array (FBGA)

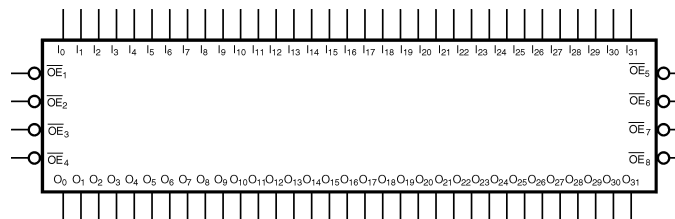
Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX32244GX (Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]

Note 2: BGA package available in Tape and Reel only.

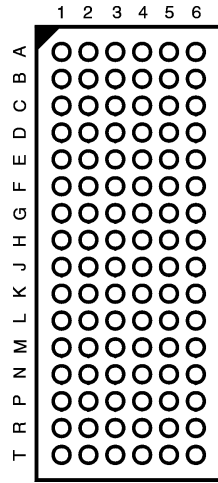
Logic Symbol



74VCX32244 Low Voltage 32-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

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Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
I_0-I_{31}	Inputs
O_0-O_{31}	Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	\overline{OE}_1	\overline{OE}_2	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC}	V_{CC}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC}	V_{CC}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	\overline{OE}_4	\overline{OE}_3	I_{15}	I_{14}
J	O_{17}	O_{16}	\overline{OE}_5	\overline{OE}_6	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC}	V_{CC}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC}	V_{CC}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	\overline{OE}_8	\overline{OE}_7	I_{31}	I_{30}

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	O_8-O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$O_{12}-O_{15}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_5	$I_{16}-I_{19}$	$O_{16}-O_{19}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_6	$I_{20}-I_{23}$	$O_{20}-O_{23}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_7	$I_{24}-I_{27}$	$O_{24}-O_{27}$
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
\overline{OE}_8	$I_{28}-I_{31}$	$O_{28}-O_{31}$
L	L	L
L	H	H
H	X	Z

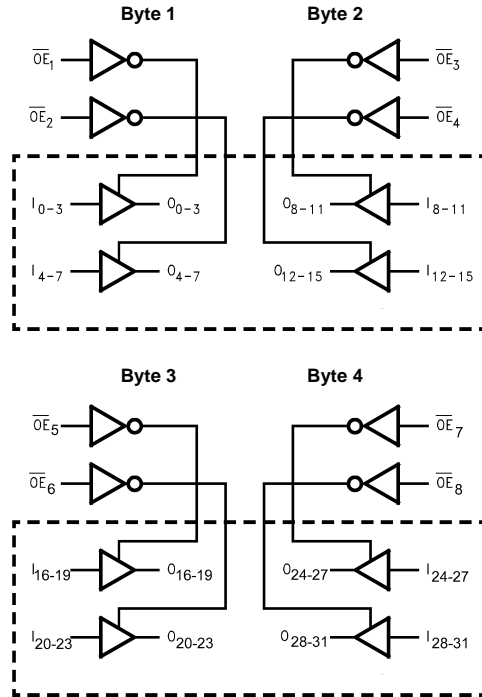
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs may not float)
 Z = High Impedance

Functional Description

The 74VCX32244 contains thirty-two non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 32-bit operation. The 3-STATE out-

puts are controlled by an Output Enable (\overline{OE}_n) input. When \overline{OE}_n is LOW, the outputs are in the 2-state mode. When \overline{OE}_n is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagrams



Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings(Note 3)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	-0.5V to +4.6V
Outputs Active (Note 4)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	± 50 mA
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	± 100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 5)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to 3.6V	± 24 mA
$V_{CC} = 2.3V$ to 2.7V	± 18 mA
$V_{CC} = 1.65V$ to 2.3V	± 6 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 3: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 4: I_O Absolute Maximum Rating must be observed.

Note 5: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < V_{CC} ≤ 3.6V)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12$ mA	2.7	2.2		V
		$I_{OH} = -18$ mA	3.0	2.4		V
		$I_{OH} = -24$ mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 12$ mA	2.7		0.4	V
		$I_{OL} = 18$ mA	3.0		0.4	V
		$I_{OL} = 24$ mA	3.0		0.55	V
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	2.7-3.6		± 5.0	μA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	2.7-3.6		± 10	μA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		40	μA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 6)	2.7-3.6		± 40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	μA

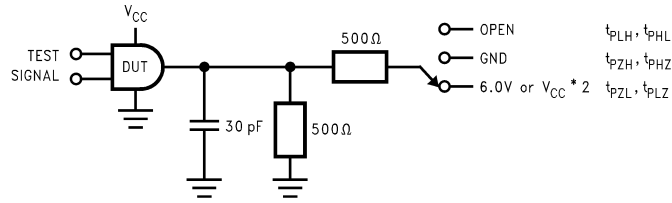
Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V ≤ V_{CC} ≤ 2.7V)						
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		2.3–2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = –100 μA	2.3–2.7	V _{CC} – 0.2		V
		I _{OH} = –6 mA	2.3	2.0		V
		I _{OH} = –12 mA	2.3	1.8		V
		I _{OH} = –18 mA	2.3	1.7		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3–2.7		0.2	V
		I _{OL} = 12 mA	2.3		0.4	V
		I _{OL} = 18 mA	2.3		0.6	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	2.3–2.7		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	2.3–2.7		±10	μA
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3–2.7		40	μA
		V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 7)	2.3–2.7		±40	μA
Note 7: Outputs disabled or 3-STATE only.						
DC Electrical Characteristics (1.65V ≤ V_{CC} < 2.3V)						
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65–2.3	0.65 × V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65–2.3		0.35 × V _{CC}	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = –100 μA	1.65–2.3	V _{CC} – 0.2		V
		I _{OH} = –6 mA	1.65	1.25		V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	1.65–2.3		0.2	V
		I _{OL} = 6 mA	1.65		0.3	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	1.65–2.3		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V V _I = V _{IH} or V _{IL}	1.65–2.3		±10	μA
I _{OFF}	Power-OFF Leakage Current	0 ≤ (V _I , V _O) ≤ 3.6V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.65–2.3		40	μA
		V _{CC} ≤ (V _I , V _O) ≤ 3.6V (Note 8)	1.65–2.3		±40	μA
Note 8: Outputs disabled or 3-STATE only.						

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AC Electrical Characteristics (Note 9)								
Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30\text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		
		Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	0.8	2.5	1.0	3.0	1.5	6.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	0.8	3.5	1.0	4.1	1.5	8.2	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	0.8	3.5	1.0	3.8	1.5	6.8	ns
Note 9: For $C_L = 50\text{ pF}$, add approximately 300 ps to the AC maximum specification.								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25^{\circ}\text{C}$	Units			
				Typical				
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	0.25	V			
			2.5	0.6				
			3.3	0.8				
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	-0.25	V			
			2.5	-0.6				
			3.3	-0.8				
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	$C_L = 30\text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0\text{V}$	1.8	1.5	V			
			2.5	1.9				
			3.3	2.2				
Capacitance								
Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units				
			Typical					
C_{IN}	Input Capacitance	$V_{CC} = 1.8, 2.5\text{V or } 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	6	pF				
C_{OUT}	Output Capacitance	$V_I = 0\text{V or } V_{CC}, V_{CC} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	7	pF				
C_{PD}	Power Dissipation Capacitance	$V_I = 0\text{V or } V_{CC}, f = 10\text{ MHz}, V_{CC} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	20	pF				

AC Loading and Waveforms



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} * 2$ at $V_{CC} = 2.5 \pm 0.2V; 1.8V \pm 0.15V$
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit

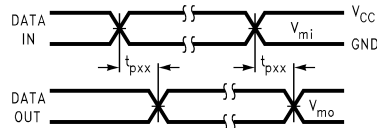


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

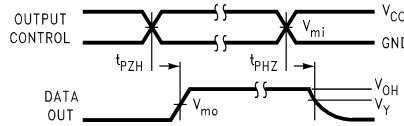


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

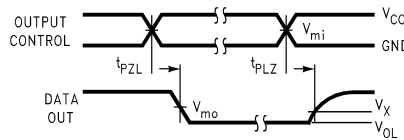


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

74VCX32244 Low Voltage 32-Bit Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs

Physical Dimensions inches (millimeters) unless otherwise noted

Top View

Bottom View

SEATING PLANE

NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A**

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