CIRRUS LOGIC®

CS8405A

96 kHz Digital Audio Interface Transmitter

Features

- Complete EIAJ CP1201, IEC-60958, AES3, S/PDIF-compatible Transmitter
- +5.0 V Digital Supply (VD+)
- +3.3 V or 5.0 V Digital Interface (VL+)
- On-chip channel status and user bit buffer memories allow block-sized updates.
- Flexible 3-wire Serial Digital Audio Input Port
- Up to 96 kHz Frame Rate
- Microcontroller Write Access to Channel Status and User Bit Data
- On-chip Differential Line Driver
- Generates CRC Codes and Parity Bits
- Standalone Mode Allows use Without a Microcontroller

General Description

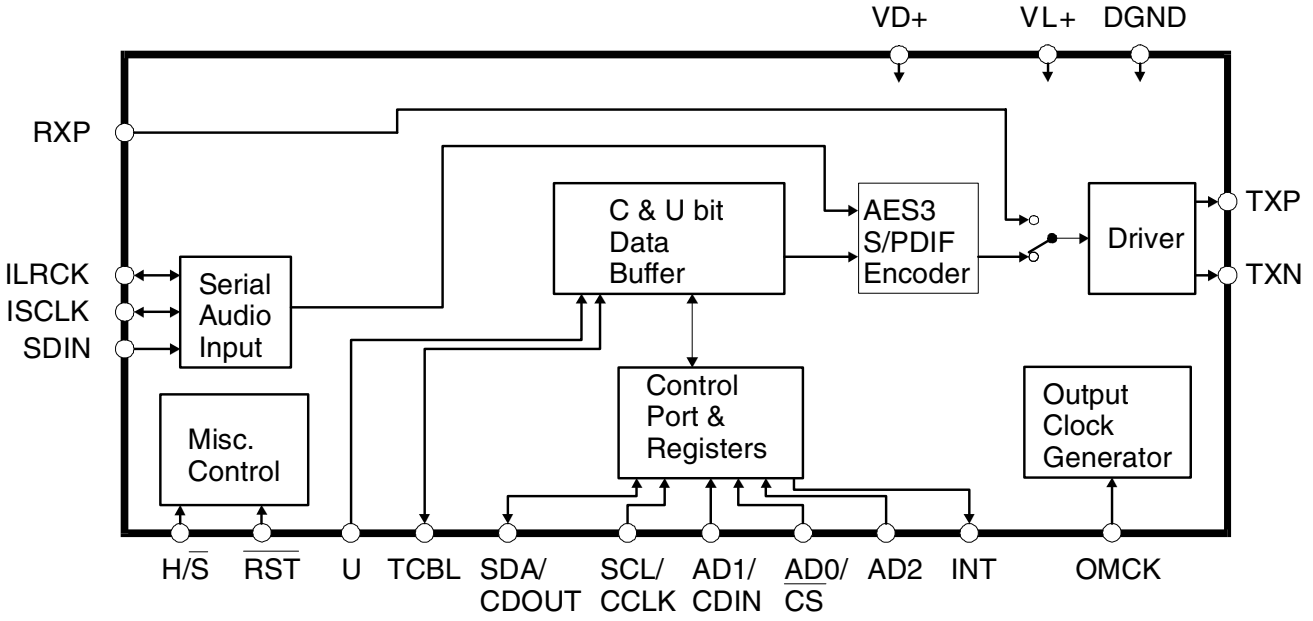
The CS8405A is a monolithic CMOS device which encodes and transmits audio data according to the AES3, IEC60958, S/PDIF, or EIAJ CP1201. The CS8405A accepts audio and digital data, which is then multiplexed, encoded, and driven onto a cable.

The audio data is input through a configurable, 3-wire input port. The channel status and user bit data are input through an SPI or I²C microcontroller port, and may be assembled in block-sized buffers. For systems with no microcontroller, a standalone mode allows direct access to channel status and user bit data pins.

Target applications include A/V Receivers, CD-R, DVD receivers, digital mixing consoles, effects processors, set-top boxes, and computer or automotive audio systems.

ORDERING INFORMATION

CS8405A-CS	28-pin SOIC	-10 to +70°C
CS8405A-CZ	28-pin TSSOP	-10 to +70°C
CS8405A-CZZ, Lead Free	28-pin TSSOP	-10 to +70°C
CS8405A-IS	28-pin SOIC	-40 to +85°C
CS8405A-IZ	28-pin TSSOP	-40 to +85°C
CDB8415A	Evaluation Board	



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1. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (DGND = 0 V, all voltages with respect to 0 V)

Parameter		Symbol	Min	Typ	Max	Units
Power Supply Voltage	(Note 1)	VD+ VL+	4.5 2.85	5.0 3.3 or 5.0	5.5 5.5	V V
Ambient Operating Temperature:	'-CS' & '-CZ' '-IS' & '-IZ'	T_A	-10 -40	- -	+70 +85	°C

Notes: 1. I²C protocol is supported only in VL+ = 5.0 V mode.

ABSOLUTE MAXIMUM RATINGS (DGND = 0 V; all voltages with respect to 0 V. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameter		Symbol	Min	Max	Units
Power Supply Voltage		VD+,VL+	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 2)	I_{in}	-	±10	mA
Input Voltage		V_{in}	-0.3	(VL+) + 0.3	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 2. Transient currents of up to 100 mA will not cause SCR latch-up.

DC ELECTRICAL CHARACTERISTICS (DGND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Typ	Max	Units
Power-down Mode (Note 3)						
Supply Current in power down	VD+		-	20	-	µA
	VL+ = 3.3 V		-	60	-	µA
	VL+ = 5.0 V		-	60	-	µA
Normal Operation (Note 4)						
Supply Current at 48 kHz frame rate	VD+		-	6.3	-	mA
	VL+ = 3.3 V		-	30.1	-	mA
	VL+ = 5.0 V		-	46.5	-	mA
Supply Current at 96 kHz frame rate	VD+		-	6.6	-	mA
	VL+ = 3.3 V		-	44.8	-	mA
	VL+ = 5.0 V		-	76.6	-	mA

Notes: 3. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

4. Normal operation is defined as $\overline{RST}$ = HI.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	±1	±10	µA

DIGITAL INTERFACE SPECIFICATIONS (DGND = 0 V; all voltages with respect to 0 V.)

Parameters		Symbol	Min	Max	Units
High-Level Output Voltage (I_{OH} = -3.2 mA), except TXP/TXN		V_{OH}	(VL+) - 1.0	-	V
Low-Level Output Voltage (I_{OL} = 3.2 mA), except TXP/TXN		V_{OL}	-	0.4	V
High-Level Output Voltage, TXP, TXN	(23 mA at VL+ = 5.0 V)		(VL+) - 0.7	-	V
	(15.2 mA at VL+ = 3.3 V)		(VL+) - 0.7	-	V
Low-Level Output Voltage, TXP, TXN	(23 mA at VL+ = 5.0 V)		-	0.7	V
	(15.2 mA at VL+ = 3.3 V)		-	0.7	V
High-Level Input Voltage		V_{IH}	2.0	(VL+) + 0.3	V
Low-Level Input Voltage	(Note 5)	V_{IL}	-0.3	0.4/0.8	V

Notes: 5. At 5.0 V mode, V_{IL} = 0.8 V (Max), at 3.3 V mode, V_{IL} =0.4 V (Max).

TRANSMITTER CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
TXP Output Resistance	VL+ = 5.0 V	R_{TXP}	-	26	-	Ω
	VL+ = 3.3 V		-	40	-	Ω
TXN Output Resistance	VL+ = 5.0 V	R_{TXN}	-	26	-	Ω
	VL+ = 3.3 V		-	40	-	Ω

SWITCHING CHARACTERISTICS

(Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{RST}$ pin Low Pulse Width		200	-	-	µs
OMCK Frequency for OMCK = 512 * Fso		4.1	-	55.3	MHz
OMCK Low and High Width for OMCK = 512 * Fso		7.2	-	-	ns
OMCK Frequency for OMCK = 384 * Fso		3.1	-	41.5	MHz
OMCK Low and High Width for OMCK = 384 * Fso		10.8	-	-	ns
OMCK Frequency for OMCK = 256 * Fso		2.0	-	27.7	MHz
OMCK Low and High Width for OMCK = 256 * Fso		14.4	-	-	ns
Frame Rate		8.0	-	108.0	kHz
AES3 Transmitter Output Jitter		-	-	1	ns

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORTS

(Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
SDIN Setup Time Before ISCLK Active Edge	(Note 6)	t_{ds}	20	-	-	ns
SDIN Hold Time After ISCLK Active Edge	(Note 6)	t_{dh}	20	-	-	ns
Master Mode						
OMCK to ISCLK active edge delay	(Note 6)	t_{smd}	0	-	10	ns
OMCK to ILRCK delay	(Note 7)	t_{lmd}	0	-	10	ns
ISCLK and ILRCK Duty Cycle			-	50	-	%
Slave Mode						
ISCLK Period	(Note 8)	t_{sckw}	36	-	-	ns
ISCLK Input Low Width		t_{sckl}	14	-	-	ns
ISCLK Input High Width		t_{sckh}	14	-	-	ns
ISCLK Active Edge to ILRCK Edge	(Note 6,7,9)	t_{lrckd}	20	-	-	ns
ILRCK Edge Setup Before ISCLK Active Edge	(Note 6,7,10)	t_{lrcks}	20	-	-	ns

Notes:
6. The active edge of ISCLK is programmable.
7. The polarity of ILRCK is programmable.
8. No more than 128 SCLK per frame.
9. Prevents the previous ISCLK edge from being interpreted as the first one after ILRCK has changed.
10. This setup time ensures that this ISCLK edge is interpreted as the first one after ILRCK has changed

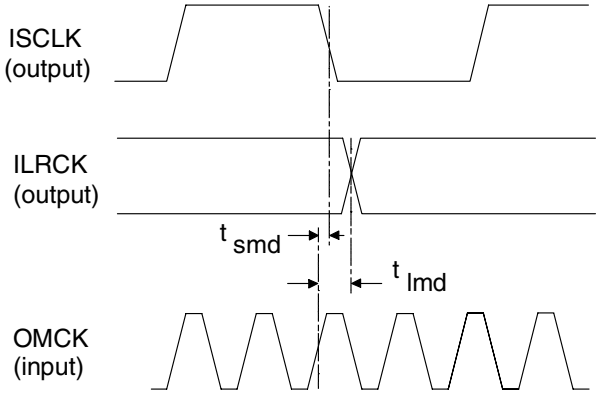


Figure 1. Audio Port Master Mode Timing

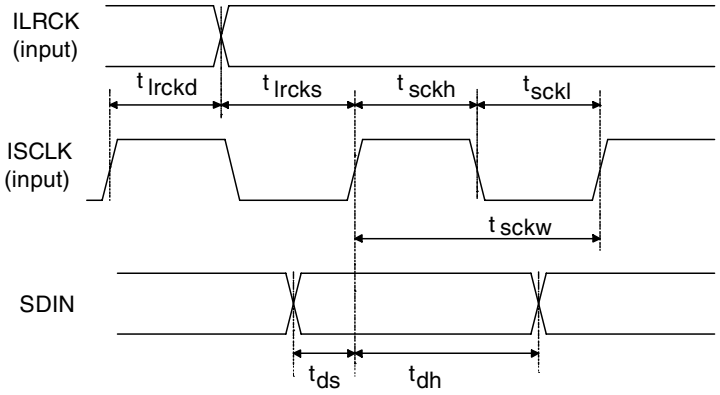


Figure 2. Audio Port Slave Mode and Data Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
CCLK Clock Frequency	(Note 11)	f_{sck}	0	-	6.0	MHz
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	-	µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	-	-	ns
CCLK Low Time		t_{scl}	66	-	-	ns
CCLK High Time		t_{sch}	66	-	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	-	ns
CCLK Rising to DATA Hold Time	(Note 12)	t_{dh}	15	-	-	ns
CCLK Falling to CDOUT Stable		t_{pd}	-	-	50	ns
Rise Time of CDOUT		t_{r1}	-	-	25	ns
Fall Time of CDOUT		t_{f1}	-	-	25	ns
Rise Time of CCLK and CDIN	(Note 13)	t_{r2}	-	-	100	ns
Fall Time of CCLK and CDIN	(Note 13)	t_{f2}	-	-	100	ns

Notes: 11. If Fs is lower than 46.875 kHz, the maximum CCLK frequency should be less than 128 Fs. This is dictated by the timing requirements necessary to access the Channel Status and User Bit buffer memory. Access to the control register file can be carried out at the full 6 MHz rate. The minimum allowable input sample rate is 8 kHz, so choosing CCLK to be less than or equal to 1.024 MHz should be safe for all possible conditions.

12. Data must be held for sufficient time to bridge the transition time of CCLK.

13. For f_{sck} < 1 MHz.

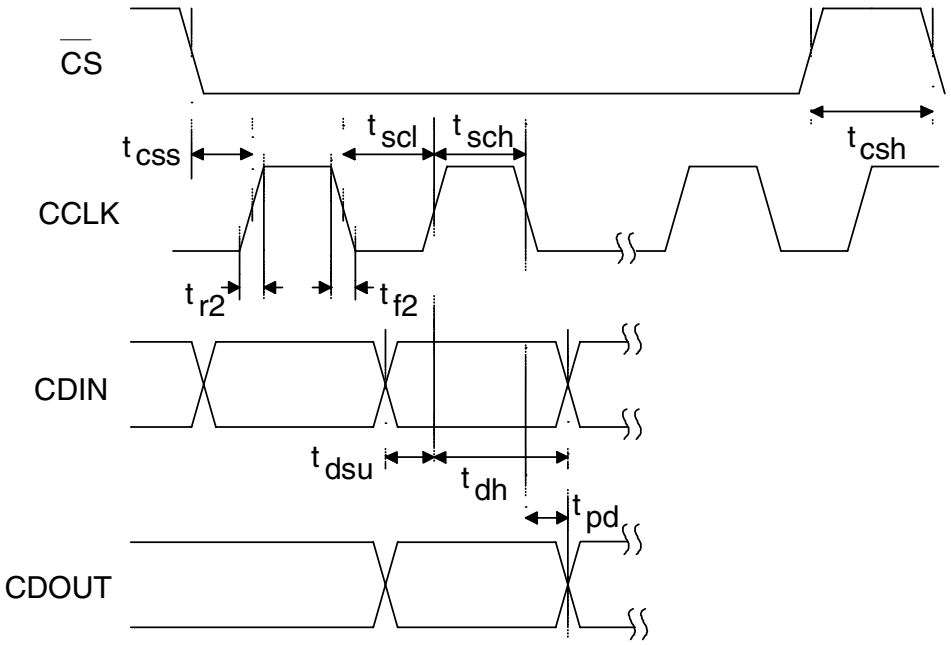


Figure 3. SPI Mode timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE

(Note 14, Inputs: Logic 0 = 0 V, Logic 1 = VL+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
SCL Clock Frequency	f_{scl}	-	-	100	kHz
Bus Free Time Between Transmissions	t_{buf}	4.7	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	-	µs
Clock Low Time	t_{low}	4.7	-	-	µs
Clock High Time	t_{high}	4.0	-	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	-	µs
SDA Hold Time from SCL Falling (Note 15)	t_{hdd}	0	-	-	µs
SDA Setup Time to SCL Rising	t_{sud}	250	-	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	-	25	ns
Fall Time of Both SDA and SCL Lines	t_f	-	-	25	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	-	µs

Notes: 14. I²C protocol is supported only in VL+ = 5.0 V mode.

15. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

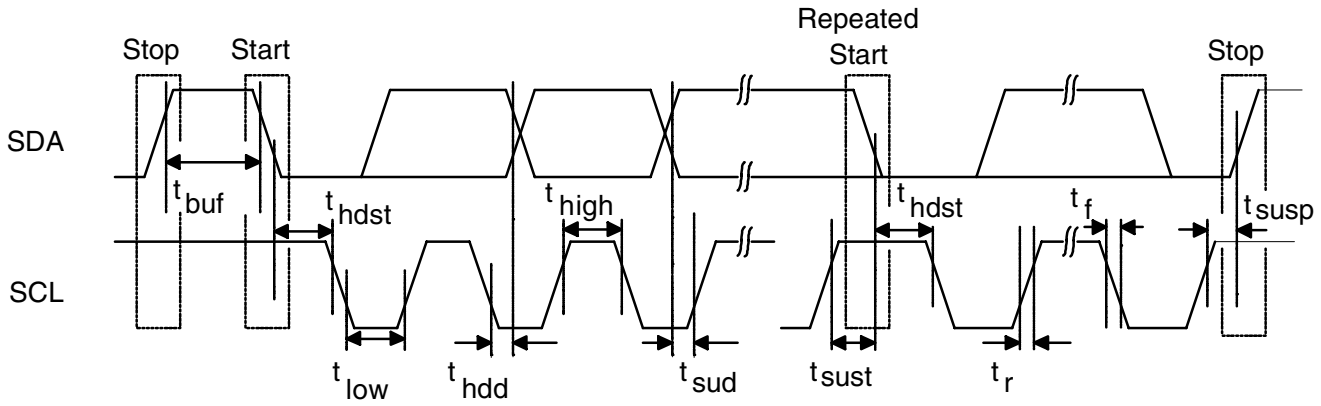


Figure 4. I²C Mode timing

2. TYPICAL CONNECTION DIAGRAM

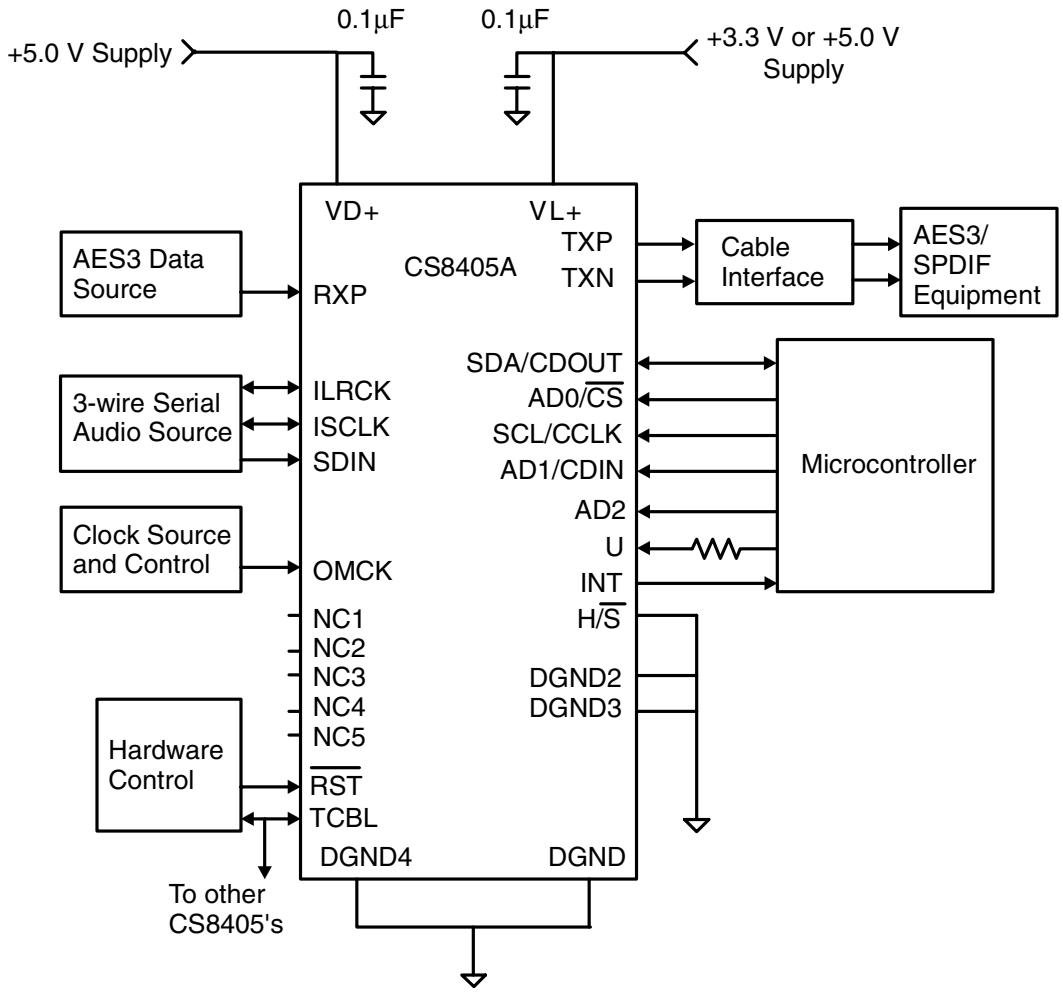


Figure 5. Recommended Connection Diagram for Software Mode

3. GENERAL DESCRIPTION

The CS8405A is a monolithic CMOS device which encodes and transmits audio data according to the AES3, IEC60958, S/PDIF, and EIAJ CP1201 interface standards. The CS8405A accepts audio, channel status and user data, which is then multiplexed, encoded, and driven onto a cable.

The audio data is input through a configurable, 3-wire input port. The channel status bits and user bit data are input through an SPI or I²C Mode microcontroller port and may be assembled in separate block sized buffers.

For systems with no microcontroller, a stand alone mode allows direct access to channel status and user data input pins.

Target applications include CD-R, DAT, DVD, MD and VTR equipment, mixing consoles, digital audio transmission equipment, high quality A/D converters, effects processors, set-top TV boxes, and computer audio systems.

Figure 5 shows the supply and external connections to the CS8405A when configured for operation with a microcontroller.

3.1 AES3 and S/PDIF Standards Documents

This data sheet assumes that the user is familiar with the AES3 and S/PDIF data formats. It is advisable to have current copies of the AES3 and IEC60958 specifications on hand for easy reference.

The latest AES3 standard is available from the Audio Engineering Society or ANSI at www.aes.org or www.ansi.org. Obtain the latest IEC60958 standard from ANSI or from the International Electrotechnical Commission at www.iec.ch. The latest EIAJ CP-1201 standard is available from the Japanese Electronics Bureau.

Crystal Application Note 22: *Overview of Digital Audio Interface Data Structures* contains a useful tutorial on digital audio specifications, but it should not be considered a substitute for the standards.

The paper *An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission*, by Clifton Sanchez, is an excellent tutorial on SCMS. It is available from the AES as preprint 3518.

4.THREE-WIRE SERIAL INPUT AUDIO PORT

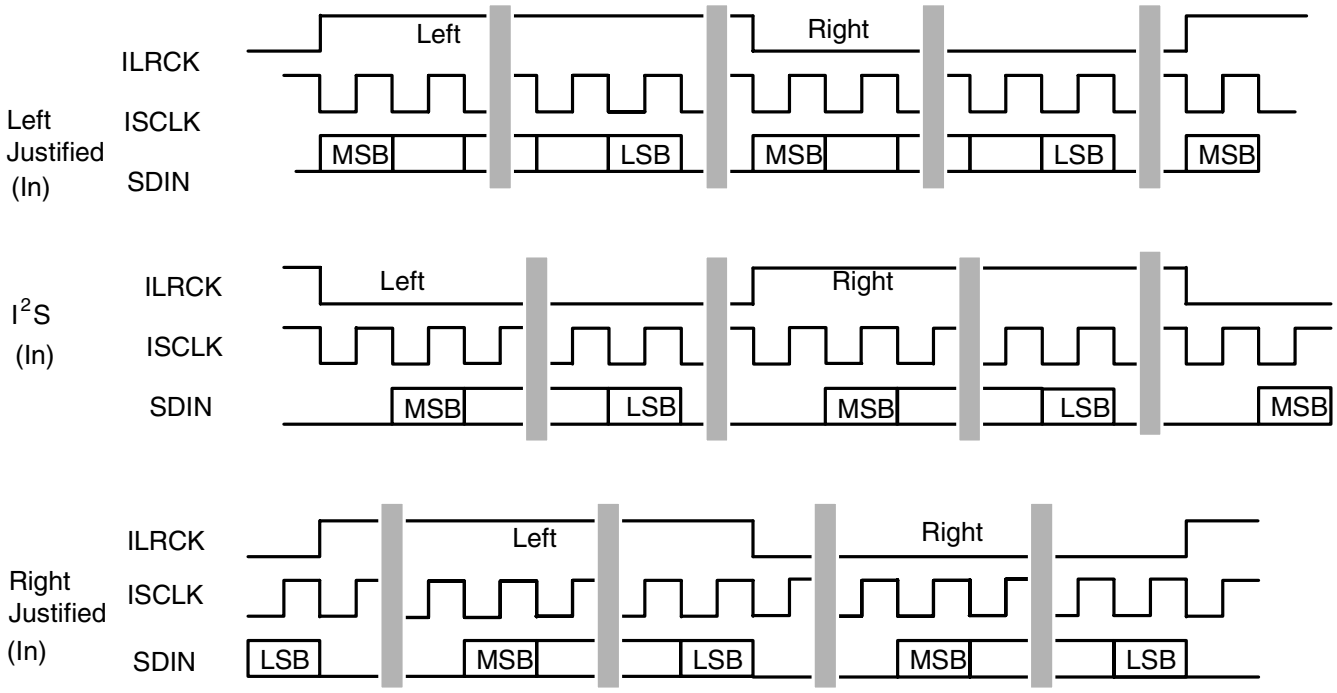
A 3-wire serial audio input port is provided. The interface format can be adjusted to suit the attached device through the control registers. The following parameters are adjustable:

- Master or slave
- Serial clock frequency
- Audio data resolution
- Left or right justification of the data relative to left/right clock
- Optional one-bit cell delay of the first data bit
- Polarity of the bit clock
- Polarity of the left/right clock. (By setting the appropriate control bits, many formats are possible).

Figure 6 shows a selection of common input formats with the corresponding control bit settings.

In master mode, the left/right clock and the serial bit clock are outputs, derived from the OMCK input pin master clock.

In slave mode, the left/right clock and the serial bit clock are inputs. The left/right clock must be synchronous to the OMCK master clock, but the serial bit clock can be asynchronous and discontinuous if required. The left/right clock should be continuous, but the duty cycle can be less than the specified typical value of 50% if enough serial clocks are present in each phase to clock all the data bits.



	SIMS*	SISF*	SIRES[1:0]*	SIJUST*	SIDEL*	SISPOL*	SILRPOL*
Left Justified	X	X	00+	0	0	0	0
I²S	X	X	00+	0	1	0	1
Right Justified	X	X	XX	1	0	0	0

X = don't care to match format, but does need to be set to the desired setting

+ I²S can accept an arbitrary number of bits, determined by the number of ISCLK cycles

* See Serial Input Port Data Format Register Bit Descriptions for an explanation of the meaning of each bit

Figure 6. Serial Audio Input Example Formats

5. AES3 TRANSMITTER

The CS8405A includes an AES3 digital audio transmitter. A comprehensive buffering scheme provides write access to the channel status and user data. This buffering scheme is described in "Appendix B: Channel Status and User Data Buffer Management" on page 35.

The AES3 transmitter encodes and transmits audio and digital data according to the AES3, IEC60958 (S/PDIF), and EIAJ CP-1201 interface standards. Audio and control data are multiplexed together and bi-phase mark encoded. The resulting bit stream is driven to an output connector either directly or through a transformer. The transmitter is clocked from the clock input pin, OM-K. If OMCK is asynchronous to the data source, an interrupt bit (TSLIP) is provided that will go high every time a data sample is dropped or repeated. Be aware that the pattern of slips does not have hysteresis and so the occurrence of the interrupt condition is not deterministic.

The channel status (C) and user (U) bits in the transmitted data stream are taken from storage areas within the CS8405A. The user can manually access the internal storage or configure the CS8405A to run in one of several automatic modes. "Appendix B: Channel Status and User Data Buffer Management" on page 35 provides detailed descriptions of each automatic mode and describes methods of manually accessing the storage areas. The transmitted user bit data can optionally be input through the U pin, under the control of a control port register bit. Figure 7 shows the timing requirements for inputting U data through the U pin.

5.1 Transmitted Frame and Channel Status Boundary Timing

The TCBL pin is used to control or indicate the start of transmitted channel status block boundaries and may be an input or an output.

In some applications, it may be necessary to control the precise timing of the transmitted AES3 frame boundaries. This may be achieved in two ways:

a) With TCBL set to input, driving TCBL high for >3 OMCK clocks will cause a frame start, as well as a new channel status block start.

b) If the serial audio input port is in slave mode and TCBL is set to output, the start of the A channel sub-frame will be aligned with the leading edge of ILRCK.

5.2 TXN and TXP Drivers

The line drivers are low skew, low impedance, differential outputs capable of driving cables directly. Both drivers are set to ground during reset ($\overline{RST}$ = low), when no AES3 transmit clock is provided, and optionally under the control of a register bit. The CS8405A also allows immediate muting of the AES3 transmitter audio data through a control register bit.

External components are used to terminate and isolate the external cable from the CS8405A. These components are detailed in "Appendix A: External AES3/SPDIF/IEC60958 Transmitter and Receiver Components" on page 34.

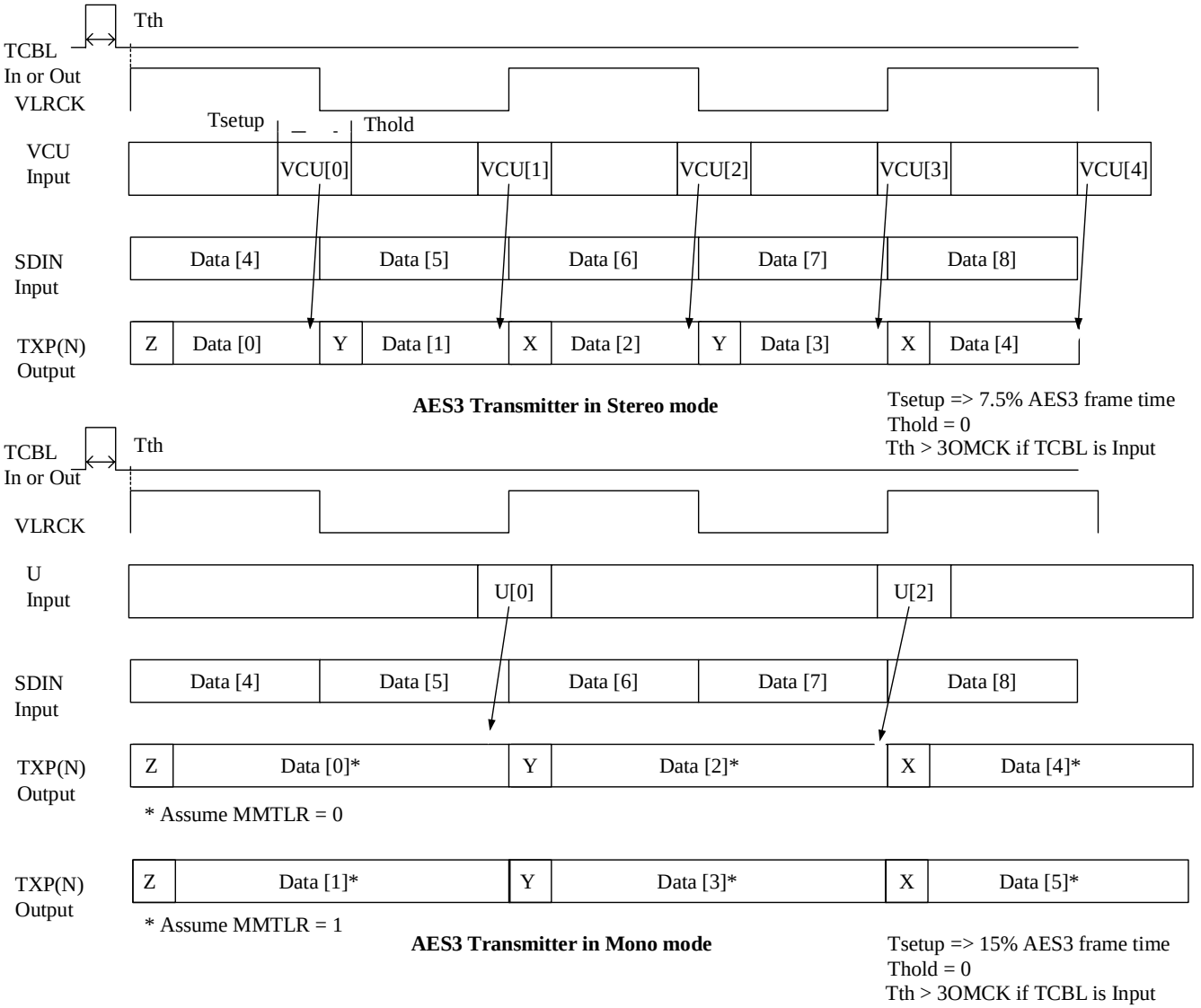
5.3 Mono Mode Operation

An AES3 stream may be used in more than one way to transmit 96 kHz sample rate data. One method is to double the frame rate of the current format. This results in a stereo signal with a sample rate of 96 kHz, carried over a single twisted pair cable. An alternate method is implemented using the two sub-frames in a 48 kHz frame rate AES3 signal to carry consecutive samples of a mono signal, resulting in a 96 kHz sample rate stream. This allows older equipment, whose AES3 transmitters and receivers are not rated for 96 kHz frame rate operation, to handle 96 kHz sample rate information. In this "mono mode", two AES3 cables are needed for stereo data transfer. The CS8405A offers mono mode operation. The CS8405A is set to mono mode by the MMT control bit.

In mono mode, the input port will run at the audio sample rate (Fs), while the AES3 transmitter frame rate will be at Fs/2. Consecutive left or right channel serial audio data samples may be selected for transmission on the A and B sub-frames, and the channel status block transmitted is also selectable.

Using mono mode is only necessary if the incoming audio sample rate is already at 96 kHz and contains both left and right audio data words. The "mono mode" AES3 output stream may also be achieved by keeping the CS8405A in normal

stereo mode, and placing consecutive audio samples in the left and right positions in an incoming 48 kHz word rate data stream.



VLRCK is a virtual word clock, which may not exist, and is used to illustrate the CUV timing.
VLRCK duty cycle is 50%.
In stereo mode, VLRCK frequency = AES3 frame rate. In mono mode, ALRCK frequency = 2xAES3 frame rate.
If the serial audio input port is on slave mode and TCBL is an output, then VLRCK=ILRCK if SILRPOL=0 and VLRCK= $\overline{\text{ILRCK}}$ if SILRPOL =1.
If the serial audio input port is in master mode and TCBL is an input, then VLRCK=ILRCK if SILRPOL=0 and VLRCK= $\overline{\text{ILRCK}}$ if SILRPOL =1.

Figure 7. AES3 Transmitter Timing for C, U, and V Pin Input Data

6. CONTROL PORT DESCRIPTION AND TIMING

The control port is used to access the registers, allowing the CS8405A to be configured for the desired operational modes and formats. In addition, Channel Status and User data may be read and written through the control port. The operation of the control port may be completely asynchronous with respect to the audio sample rate.

The control port has two modes: SPI and I²C, with the CS8405A acting as a slave device. SPI mode is selected if there is a high to low transition on the AD0/$\overline{CS}$ pin after the $\overline{RST}$ pin has been brought high. I²C mode is selected by connecting the AD0/$\overline{CS}$ pin to VL+ or DGND, thereby permanently selecting the desired AD0 bit address state.

6.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS8405A chip select signal, CCLK is the control port bit clock (input into the CS8405A from the microcontroller); CDIN is the input data line from the microcontroller; and CDOUT is the output data line to the microcontroller. Data is clocked in on the rising edge of CCLK and out on the falling edge.

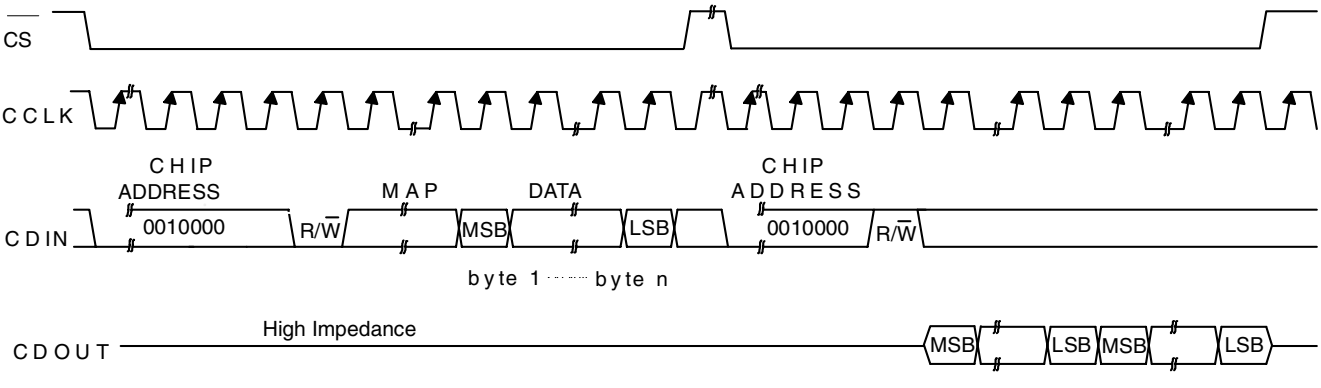
Figure 8 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which should be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data which will be placed into the register designated by the MAP. During writes, the CDOUT output stays in the Hi-Z state. It may be externally pulled high or low with a 47 kΩ resistor, if desired.

There is a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, the MAP will stay constant for successive read or writes. If INCR is set to a 1, then the MAP will auto increment after each byte is read or written, allowing block reads or writes of successive registers.

To read a register, the MAP has to be set to the correct address by executing a partial write cycle which finishes ($\overline{CS}$ high) immediately after the MAP byte. The MAP auto increment bit (INCR) may be set or not, as desired. To begin a read, bring $\overline{CS}$ low, send out the chip address and set the read/write bit (R/$\overline{W}$) high. The next falling edge of CCLK will clock out the MSB of the addressed register (CDOUT will leave the high impedance state). If the MAP auto increment bit is set to 1, the data for successive registers will appear consecutively.

6.2 I²C Mode

In I²C Mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 9. There is no $\overline{CS}$ pin. Each individual CS8405A is given a unique address. Pins AD0, AD1, and AD2 form the three least significant bits



MAP = Memory Address Pointer, 8 bits, MSB first

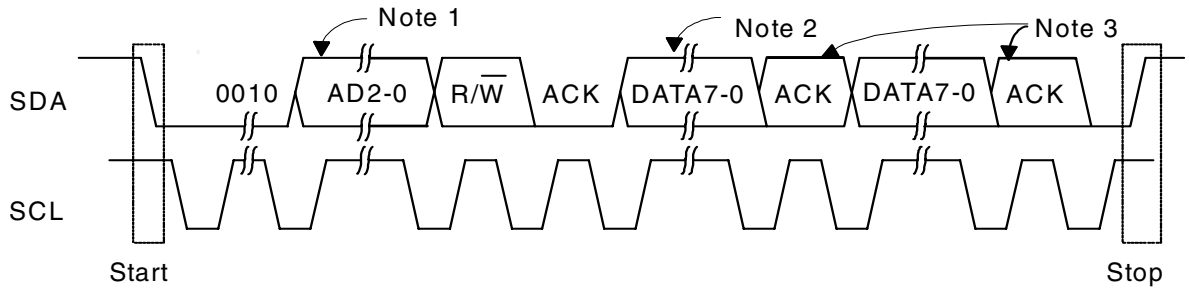
Figure 8. Control Port Timing in SPI Mode

of the chip address, and should be connected to VL+ or DGND as desired. The upper four bits of the seven-bit address field are fixed at 0010. To communicate with a CS8405A, the chip address field, which is the first byte sent to the CS8405A, should match 0010 followed by the settings of AD2, AD1, and AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit, ACK, which is output from the CS8405A after each input byte is read. The ACK bit is input to the CS8405A from the microcontroller after each transmitted byte. I²C mode is supported only with VL+ = 5.0 V.

6.3 Interrupts

The CS8405A has a comprehensive interrupt capability. The INT output pin is intended to drive the interrupt input pin on the host microcontroller. The INT pin may be set to be active low, active high or active low with no active pull-up transistor. This last mode is used for active low, wired-OR hook-ups, with multiple peripherals connected to the microcontroller interrupt input pin.

Many conditions can cause an interrupt, as listed in the interrupt status register descriptions. Each source may be masked off by a bit in the mask registers. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different set-ups are possible, depending on the needs of the equipment designer.



Notes:
1. AD2, AD1, and AD0 are determined by the state of the corresponding pins.
2. If operation is a write, this byte contains the Memory Address Pointer, MAP.
3. If operation is a read, the last bit of the read should be NACK (high).

Figure 9. Control Port Timing in I²C Mode

7. CONTROL PORT REGISTER SUMMARY

Addr (HEX)	Function	7	6	5	4	3	2	1	0
00	Reserved	0	0	0	0	0	0	0	0
01	Control 1	0	VSET	0	MUTEAES	0	INT1	INT0	TCBLD
02	Control 2	0	0	0	0	0	MMT	MMCST	MMTLR
03	Data Flow Control	0	TXOFF	AESBP	0	0	0	0	0
04	Clock Source Control	0	RUN	CLK1	CLK0	0	0	0	0
05	Serial Input Format	SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL
06	Reserved	0	0	0	0	0	0	0	0
07	Interrupt 1 Status	TSLIP	0	0	0	0	0	EFTC	0
08	Interrupt 2 Status	0	0	0	0	0	EFTU	0	0
09	Interrupt 1 Mask	TSLIPM	0	0	0	0	0	EFTCM	0
0A	Interrupt 1 Mode (MSB)	TSLIP1	0	0	0	0	0	EFTC1	0
0B	Interrupt 1 Mode (LSB)	TSLIP0	0	0	0	0	0	EFTC0	0
0C	Interrupt 2 Mask	0	0	0	0	0	EFTUM	0	0
0D	Interrupt 2 Mode (MSB)	0	0	0	0	0	EFTU1	0	0
0E	Interrupt 2 Mode (LSB)	0	0	0	0	0	EFTU0	0	0
0F-11	Reserved	0	0	0	0	0	0	0	0
12	CS Data Buffer Control	0	0	BSEL	0	0	EFTCI	CAM	0
13	U Data Buffer Control	0	0	0	UD	UBM1	UBM0	0	EFTUI
14-1F	Reserved	0	0	0	0	0	0	0	0
20-37	C or U Data Buffer								
7F	ID and Version	ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

Table 1. Control Register Map Summary

7.1 MEMORY ADDRESS POINTER (MAP)

7	6	5	4	3	2	1	0
INCR	MAP6	MAP5	MAP4	MAP3	MAP2	MAP1	MAP0

INCR - Auto Increment Address Control Bit

Default = '0'

0 - Disable
1 - Enable

MAP6:MAP0 - Register Address

Note: Reserved registers must not be written to during normal operation. Some reserved registers are used for test modes, which can completely alter the normal operation of the CS8405A.

8. CONTROL PORT REGISTER BIT DEFINITIONS

8.1 Control 1 (01h)

7	6	5	4	3	2	1	0
0	VSET	0	MUTEAES	0	INT1	INT0	TCBLD

VSET - Transmitted Validity bit level

Default = '0'

0 - Indicates data is valid, linear PCM audio data
1 - Indicates data is invalid or not linear PCM audio data

MUTEAES - Mute control for the AES transmitter output

Default = '0'

0 - Not Muted
1 - Muted

INT1:0 - Interrupt output pin (INT) control

Default = '00'

00 - Active high; high output indicates interrupt condition has occurred
01 - Active low, low output indicates an interrupt condition has occurred
10 - Open drain, active low. Requires an external pull-up resistor on the INT pin.
11 - Reserved

TCBLD - Transmit Channel Status Block pin (TCBL) direction specifier

Default = '0'

0 - TCBL is an input
1 - TCBL is an output

8.2 Control 2 (02h)

7	6	5	4	3	2	1	0
0	0	0	0	0	MMT	MMTCS	MMTLR

MMT - Select AES3 transmitter mono or stereo operation

Default = '0'

0 - Normal stereo operation
1 - Output either left or right channel inputs into consecutive subframe outputs (mono mode, left or right is determined by MMTLR bit)

MMTCS - Select A or B channel status data to transmit in mono mode

Default = '0'

0 - Use channel A CS data for the A subframe and use channel B CS data for the B subframe
1 - Use the same CS data for both the A and B subframe outputs. If MMTLR = 0, use the left channel CS data. If MMTLR = 1, use the right channel CS data.

MMTLR - Channel Selection for AES Transmitter mono mode

Default = '0'

0 - Use left channel input data for consecutive subframe outputs
1- Use right channel input data for consecutive subframe outputs

8.3 Data Flow Control (03h)

7	6	5	4	3	2	1	0
0	TXOFF	AESBP	0	0	0	0	0

The Data Flow Control register configures the flow of audio data. The output data should be muted prior to changing bits in this register to avoid transients.

TXOFF - AES3 Transmitter Output Driver Control

Default = '0

0 - AES3 transmitter output pin drivers normal operation
1 - AES3 transmitter output pin drivers drive to 0 V.

AESBP - AES3 bypass mode selection

Default = '0'

0 - Normal operation
1 - Connect the AES3 transmitter driver input directly to the RXP pin, which becomes a normal TTL threshold digital input. The OMCK clock must be present for the bypass mode to work.

8.4 Clock Source Control (04h)

7	6	5	4	3	2	1	0
0	RUN	CLK1	CLK0	0	0	0	0

This register configures the clock sources of various blocks. In conjunction with the Data Flow Control register, various Receiver/Transmitter/Transceiver modes may be selected.

RUN - Controls the internal clocks, allowing the CS8405A to be placed in a "powered down" low current consumption, state.

Default = '0'

0 - Internal clocks are stopped. Internal state machines are reset. The fully static control port registers are operational, allowing registers to be read or changed. Reading and writing the U and C data buffers is not possible. Power consumption is low.
1 - Normal part operation. This bit must be set to 1 to allow the CS8405A to begin operation. All input clocks should be stable in frequency and phase when RUN is set to 1.

CLK1:0 - Output master clock (OMCK) input frequency to output sample rate (Fs) ratio selector. If these bits are changed during normal operation, then always stop the CS8405A first (RUN = 0), write the new value, then start the CS8405A (RUN = 1).

Default = '00'

00 - OMCK frequency is 256*Fs
01 - OMCK frequency is 384*Fs
10 - OMCK frequency is 512*Fs
11 - Reserved

8.5 Serial Audio Input Port Data Format (05h)

7	6	5	4	3	2	1	0
SIMS	SISF	SIRES1	SIRES0	SIJUST	SIDEL	SISPOL	SILRPOL

SIMS - Master/Slave Mode Selector

Default = '0'

0 - Serial audio input port is in slave mode
1 - Serial audio input port is in master mode

SISF - ISCLK frequency (for master mode)

Default = '0'

0 - 64*Fs
1 - 128*Fs

SIRES1:0 - Resolution of the input data, for right-justified formats

Default = '00'

00 - 24-bit resolution
01 - 20-bit resolution
10 - 16-bit resolution
11 - Reserved

SIJUST - Justification of SDIN data relative to ILRCK

Default = '0'

0 - Left-justified
1 - Right-justified

SIDEL - Delay of SDIN data relative to ILRCK, for left-justified data formats

Default = '0'

0 - MSB of SDIN data occurs in the first ISCLK period after the ILRCK edge (left justified mode)
1 - MSB of SDIN data occurs in the second ISCLK period after the ILRCK edge (I²S mode)

SISPOL - ISCLK clock polarity

Default = '0'

0 - SDIN sampled on rising edges of ISCLK
1 - SDIN sampled on falling edges of ISCLK

SILRPOL - ILRCK clock polarity

Default = '0'

0 - SDIN data is for the left channel when ILRCK is high
1 - SDIN data is for the right channel when ILRCK is high

8.6 Interrupt 1 Status (07h) (Read Only)

7	6	5	4	3	2	1	0
TSLIP	0	0	0	0	0	EFTC	0

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register. This register defaults to 00h.

TSLIP - AES3 transmitter source data slip interrupt

In data flows where OMCK, which clocks the AES3 transmitter, is asynchronous to the data source, this bit will go high every time a data sample is dropped or repeated. When TCBL is an input, this bit will go high on receipt of a new TCBL signal.

EFTC - E to F C-buffer transfer interrupt.

The source for this bit is true during the E to F buffer transfer in the C bit buffer management process.

8.7 Interrupt 2 Status (08h) (Read Only)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTU	0	0

For all bits in this register, a “1” means the associated interrupt condition has occurred at least once since the register was last read. A ”0” means the associated interrupt condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0, unless the interrupt mode is set to level and the interrupt source is still true. Status bits that are masked off in the associated mask register will always be “0” in this register. This register defaults to 00h.

EFTU - E to F U-buffer transfer interrupt. (Block Mode only)

The source of this bit is true during the E to F buffer transfer in the U bit buffer management process.

8.8 Interrupt 1 Mask (09h)

7	6	5	4	3	2	1	0
TSLIPM	0	0	0	0	0	EFTCM	0

The bits of this register serve as a mask for the Interrupt 1 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 1 register. This register defaults to 00h.

8.9 Interrupt 1 Mode MSB (0Ah) and Interrupt 1 Mode LSB (0Bh)

7	6	5	4	3	2	1	0
TSLIP1	0	0	0	0	0	EFTC1	0
TSLIP0	0	0	0	0	0	EFTC0	0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Actice High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.10 Interrupt 2 Mask (0Ch)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTUM	0	0

The bits of this register serve as a mask for the Interrupt 2 register. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the INT pin and the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the INT pin or the status register. The bit positions align with the corresponding bits in Interrupt 2 register. This register defaults to 00h.

8.11 Interrupt 2 Mode MSB (0Dh) and Interrupt Mode 2 LSB (0Eh)

7	6	5	4	3	2	1	0
0	0	0	0	0	EFTU1	0	0
0	0	0	0	0	EFTU0	0	0

The two Interrupt Mode registers form a 2-bit code for each Interrupt Register 1 function. There are three ways to set the INT pin active in accordance with the interrupt condition. In the Rising edge active mode, the INT pin becomes active on the arrival of the interrupt condition. In the Falling edge active mode, the INT pin becomes active on the removal of the interrupt condition. In Level active mode, the INT interrupt pin becomes active during the interrupt condition. Be aware that the active level (Active High or Low) only depends on the INT[1:0] bits. These registers default to 00.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

8.12 Channel Status Data Buffer Control (12h)

7	6	5	4	3	2	1	0
0	0	BSEL	0	0	EFTCI	CAM	0

BSEL - Selects the data buffer register addresses to contain User data or Channel Status data

Default = '0'

0 - Data buffer address space contains Channel Status data
1 - Data buffer address space contains User data

Note: There are separate complete buffers for the Channel Status and User bits. This control bit determines which buffer appears in the address space.

EFTCI - E to F C-data buffer transfer inhibit bit.

Default = '0'

0 - Allow C-data E to F buffer transfers
1 - Inhibit C-data E to F buffer transfers

CAM - C-data buffer control port access mode bit

Default = '0'

0 - One byte mode
1 - Two byte mode

8.13 User Data Buffer Control (13h)

7	6	5	4	3	2	1	0
0	0	0	UD	UBM1	UBM0	0	EFTUI

UD - User bit data source specifier

Default = '0'

0 - The U pin is an input. The User bit data is latched in on both rising and falling edges of OLRCK. This setting also chooses the U pin as the source for transmitted U data.
1 - Sets the U data buffer as the source of transmitted U data. The U pin also becomes an indeterminate output.

UBM1:0 - Sets the operating mode of the AES3 User bit manager

Default = '00'

00 - Transmit all zeros mode
01 - Block mode
10 - Reserved
11 - Reserved

EFTUI - E to F U-data buffer transfer inhibit bit (valid in block mode only).

Default = '0'

0 - Allow U-data E to F buffer transfers
1 - Inhibit U-data E to F buffer transfer

8.14 Channel Status bit or User bit Data Buffer (20h - 37h)

Either the channel status data buffer E or the separate user bit data buffer E (provided UBM bits are set to block mode) is accessible through these register addresses.

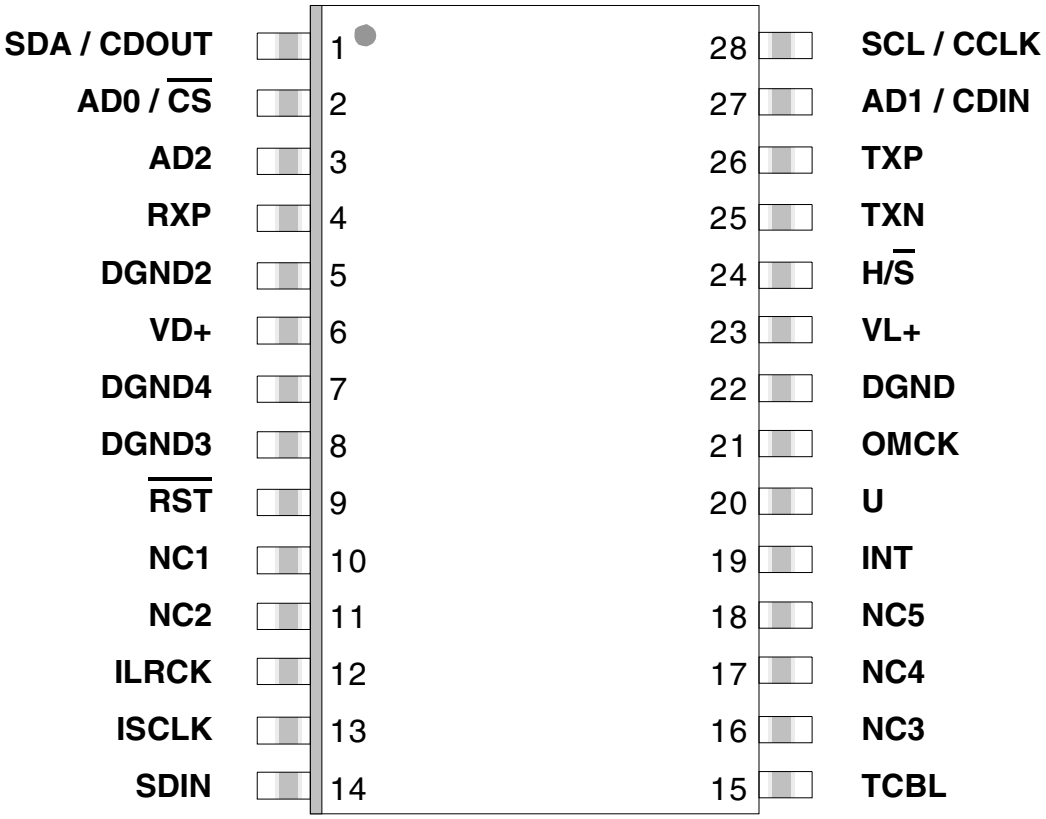
8.15 CS8405A I.D. and Version Register (7Fh) (Read Only)

7	6	5	4	3	2	1	0
ID3	ID2	ID1	ID0	VER3	VER2	VER1	VER0

ID3:0 - ID code for the CS8405A. Permanently set to 0110

VER3:0 - CS8405A revision level. Revision A is coded as 0001

9. PIN DESCRIPTION - SOFTWARE MODE



VD+	6	**Digital Power** (*Input*) - Digital core power supply. Typically +5.0 V.
VL+	23	**Logic Power** (*Input*) - Input/Output power supply. Typically +3.3 V or +5.0 V.
DGND **DGND2** **DGND3** **DGND4**	22 5 8 7	**Ground** (*Input*) - Ground for I/O and core logic.
RST	9	**Reset** (*Input*) - When RST is low, the CS8405A enters a low power mode and all internal states are reset. On initial power up, RST must be held low until the power supply is stable, and all input clocks are stable in frequency and phase. This is particularly true in hardware mode with multiple CS8405A devices, where synchronization between devices is important.
H/S	24	**Hardware/Software Control Mode Select** (*Input*) -Determines the method of controlling the operation of the CS8405A, and the method of accessing Channel Status and User bit data. In software mode, device control and CS and U data access is primarily through the control port, using a microcontroller. Hardware mode provides an alternate mode of operation, and access to CS and U data is provided by dedicated pins. This pin should be permanently tied to VL+ or DGND.
TXN **TXP**	25 26	**Differential Line Drivers** (*Output*) - These pins transmit biphase encoded data. The drivers are pulled low while the CS8405A is in the reset state.
OMCK	21	**Master Clock** (*Input*) - The frequency must be 256x, 384x, or 512x the sample rate.

ISCLK	13	**Serial Audio Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
ILRCK	12	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
SDIN	14	**Serial Audio Data Port** (*Input*) - Audio data serial input pin.
SDA/CDOUT	1	**Serial Control Data I/O (I²C Mode) / Data Out (SPI)** (*Input/Output*) - In I²C Mode, SDA is the control I/O data line. SDA is open drain and requires an external pull-up resistor to VL+. In SPI mode, CDOUT is the output data from the control port interface on the CS8405A
SCL/CCLK	28	**Control Port Clock** (*Input*) - Serial control interface clock and is used to clock control data bits into and out of the CS8405A. In I²C mode, SCL requires an external pull-up resistor to VL+.
AD0/$\overline{\text{CS}}$	2	**Address Bit 0 (I²C Mode) / Control Port Chip Select (SPI)** (*Input)* - A falling edge on this pin puts the CS8405A into SPI control port mode. With no falling edge, the CS8405A defaults to I²C mode. In I²C mode, AD0 is a chip address pin. In SPI mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS8405A
AD1/CDIN	27	**Address Bit 1 (I²C Mode) / Serial Control Data in (SPI)** (*Input*) - In I²C mode, AD1 is a chip address pin. In SPI mode, CDIN is the input data line for the control port interface.
AD2	3	**Address Bit 2 (I²C Mode)** (*Input*) - Determines the AD2 address bit for the control port in I²C mode, and should be connected to DGND or VL+. If SPI mode is used, the AD2 pin should be connected to DGND.
RXP	4	**Auxiliary AES3 Receiver Port** (*Input*) - Input for an alternate, already bi-phase encoded, audio data source.
INT	19	**Interrupt** (*Output*) - Indicates key events during the operation of the CS8405A. All bits affecting INT may be unmasked through bits in the control registers. Indication of the condition(s) that initiated an interrupt are readable in the control registers. The polarity of the INT output, as well as selection of a standard or open drain output, is set through a control register. Once set true, the INT pin goes false only after the interrupt status registers have been read and the interrupt status bits have returned to zero.
TCBL	15	**Transmit Channel Status Block Start** (*Input*/*Output*) - When operated as output, TCBL is high during the first sub-frame of a transmitted channel status block, and low at all other times. When operated as input, driving TCBL high for at least three OMCK clocks will cause the next transmitted sub-frame to be the start of a channel status block.
U	20	**User Data** (*Input*/*Output*) - May optionally be used to input User data for transmission by the AES3 transmitter, see Figure 7 for timing information. Alternatively, the U pin may be set to output, which also selects the internal buffer as the source of transmitted U data. If not driven, a 47 kW pull-down resistor is recommended for the U pin, because the default state of the UD direction bit sets the U pin as an input. The pull-down resistor ensures that the transmitted user data will be zero. If the U pin is always set to be an output, thereby causing the U bit manager to be the source of the U data, then the resistor is not necessary. The U pin should not be tied directly to ground, in case it is programmed to be an output, and subsequently tries to output a logic high. This situation may affect the long term reliability of the device. If the U pin is driven by a logic level output, then a 100 W series resistor is recommended.
NC1 **NC2** **NC3** **NC4** **NC5**	10 11 16 17 18	**No Connect** - These pins should not be connected to any signals or PCB trace. They may be driven high and/or low by the CS8405A.

10. HARDWARE MODE

The CS8405A has a hardware mode that allows the use of the device without a microcontroller. Hardware mode is selected by connecting the H/$\overline{S}$ pin to VL+. The flexibility of the CS8405A is necessarily limited in hardware mode. Various pins change function as described in the hardware mode pin description section.

The hardware mode data flow is shown in Figure 10. Audio data is input through the serial audio input port and routed to the AES3 transmitter.

10.1 Channel Status, User and Validity Data

The transmitted channel status, user and validity data can be input in two methods, determined by the state of the CEN pin. Mode A is selected when the CEN pin is low. In mode A, the user bit data and the validity bit are input through the U and V pins, clocked by both edges of ILRCK. The channel status data is derived from the state of the COPY/C, ORIG, $\overline{EMPH}$, and $\overline{AUDIO}$ pins. Table 2 shows how the COPY/C and ORIG pins map to channel status bits. In consumer mode, the transmitted category code is set to Sample Rate Converter (0101100).

Mode B is selected when the CEN pin is high. In mode B, the channel status, user data bits and the validity bit are input serially through the COPY/C, U and V pins. Data is clocked into these pins at both edges of ILRCK. Figure 7 shows the timing requirements.

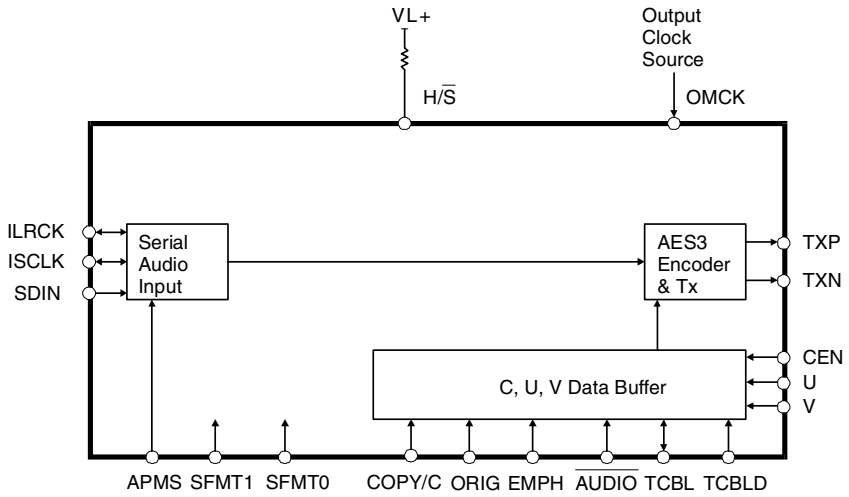
The channel status block pin (TCBL) may be an input or an output, determined by the state of the TCBLD pin.

10.2 Serial Audio Port Formats

The serial audio input port data format is selected as shown in Table 3, and may be set to master or slave by the state of the APMS input pin. Table 4 describes the equivalent software mode, bit settings for each of the available formats. Timing diagrams are shown in Figure 6.

COPY/C	ORIG	Function
0	0	PRO=0, COPY=0, L=0 copyright
0	1	PRO=0, COPY=0, L=1 copyright, pre-recorded
1	0	PRO=0, COPY=1, L=0 non-copyright
1	1	PRO=1

Table 2. Hardware Mode COPY/C and ORIG pin functions



Power supply pins and the reset pin are omitted from this diagram.
Please refer to the Typical Connection Diagram for hook-up details.

Figure 10. Hardware Mode

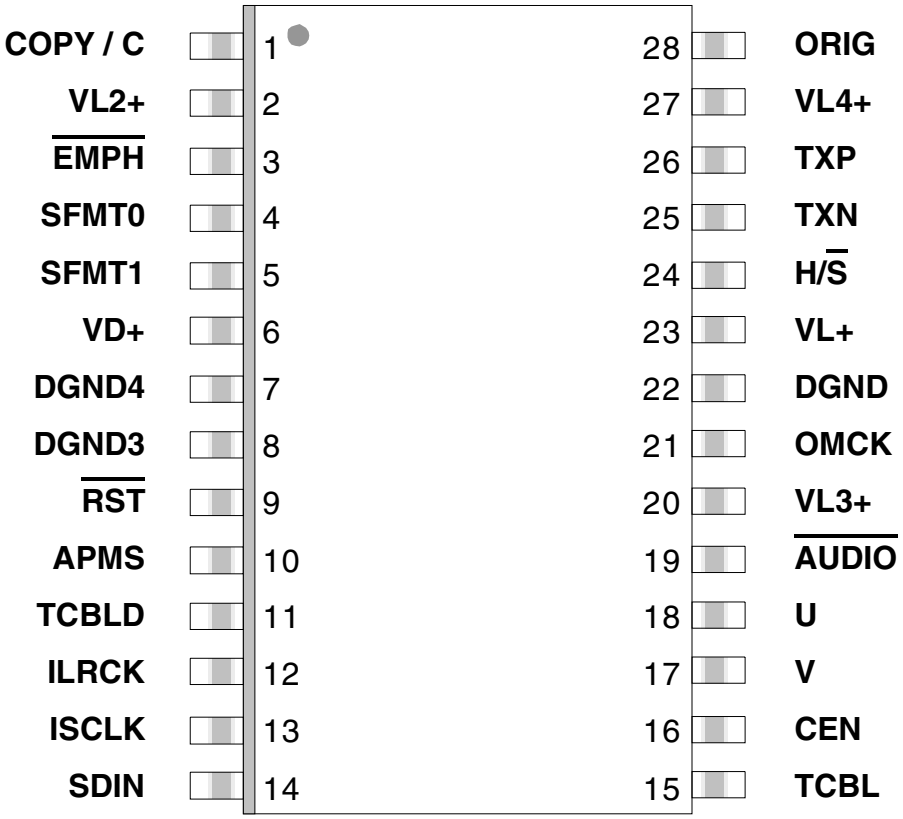
SFMT1	SFMT0	Function
0	0	Serial Input Format IF1 - Left Justified
0	1	Serial Input Format IF2 - I²S
1	0	Serial Input Format IF3 - Right Justified, 24-bit data
1	1	Serial Input Format IF4 - Right Justified, 16-bit data

Table 3. Hardware Mode Serial Audio Port Format Selection

	SISF	SIRES1/0	SIJUST	SIDEL	SISPOL	SILRPOL
IF1 - Left Justified	0	00	0	0	0	0
IF2 - I²S	0	00	0	1	0	1
IF3 - Right Justified, 24-bit data	0	00	1	0	0	0
IF4 - Right Justified, 16-bit data	0	10	1	0	0	0

Table 4. Equivalent Register Settings of Serial Audio Input Formats Available in Hardware Mode

11.PIN DESCRIPTION - HARDWARE MODE



VD+	6	**Digital Power** (*Input*) - Digital core power supply. Typically +5.0 V.
VL+ **VL2+** **VL3+** **VL4+**	23 2 20 27	**Logic Power** (*Input*) - Input/Output power supply. Typically +3.3 V or +5.0 V. All VL+ pins must be at the same voltage.
DGND **DGND3** **DGND4**	22 8 7	**Digital Ground** (*Input*) - Ground for the digital section.
RST	9	**Reset** (*Input*) - When RST is low, the CS8405A enters a low power mode and all internal states are reset. On initial power up, RST must be held low until the power supply is stable, and all input clocks are stable in frequency and phase. This is particularly true in hardware mode with multiple CS8405A devices, where synchronization between devices is important.
H/S	24	**Hardware/Software Control Mode Select** (*Input*) -Determines the method of controlling the operation of the CS8405A, and the method of accessing CS and U data. In software mode, device control and CS and U data access is primarily through the control port, using a microcontroller. Hardware mode provides an alternate mode of operation, and access to CS and U data is provided by dedicated pins. This pin should be permanently tied to VL+ or DGND.
TXN **TXP**	25 26	**Differential Line Drivers** (*Output*) - These pins transmit biphase encoded data. The drivers are pulled low while the CS8405A is in the reset state.

OMCK	21	**Master Clock** (*Input*) - The frequency must be only 256x the sample rate.
ISCLK	13	**Serial Audio Bit Clock** (*Input*/*Output*) - Serial bit clock for audio data on the SDIN pin.
ILRCK	12	**Serial Audio Input Left/Right Clock** (*Input*/*Output*) - Word rate clock for the audio data on the SDIN pin.
SDIN	14	**Serial Audio Data Port** (*Input*) - Audio data serial input pin.
SFMT0 **SFMT1**	4 5	**Serial Audio Data Format Select** (*Input*) - Selecta the serial audio input port format. See Table 3.
APMS	10	**Serial Audio Data Port Master/Slave Select** (*Input*) - APMS should be connected to VL+ to set serial audio input port as a master or connected to DGND to set the port as a slave.
TCBLD	11	**Transmit Channel Status Block Direction** (*Input*) - Connect TCBLD to VL+ to set TCBL as an output. Connect TCBLD to DGND to set TCBL as an input.
TCBL	15	**Transmit Channel Status Block Start** (*Input*/*Output*) - When operated as output, TCBL is high during the first sub-frame of a transmitted channel status block, and low at all other times. When operated as input, driving TCBL high for at least three OMCK clocks will cause the next transmitted sub-frame to be the start of a channel status block.
CEN	16	**C Bit Enable** (*Input*) - Determines how the channel status data bits are input. When CEN is low, hardware mode A is selected, where the COPY/C, ORIG, $\overline{\text{EMPH}}$ and $\overline{\text{AUDIO}}$ pins are used to enter selected channel status data. When CEN is high, hardware mode B is selected, where the COPY/C pin is used to enter serial channel status data.
V	17	**Validity Bit** (*Input*) - In hardware modes A and B, the V pin input determines the state of the validity bit in the outgoing AES3 transmitted data. This pin is sampled on both edges of the ILRCK.
U	18	**User Data Bit** (*Input*) - In hardware modes A and B, the U pin input determines the state of the user data bit in the outgoing AES3 transmitted data. This pin is sampled on both edges of the ILRCK.
COPY/C	1	**COPY Channel Status Bit/C Bit** (Input) - In hardware mode A (CEN = 0), the COPY/C and ORIG pins determine the state of the Copyright, Pro, and L Channel Status bits in the outgoing AES3 data stream, see Table 2. In hardware mode B, the COPY/C pin becomes the direct C bit input data pin.
$\overline{\text{EMPH}}$	3	**Pre-Emphasis Indicator** (*Input*) - In hardware mode A (CEN = 0), the $\overline{\text{EMPH}}$ pin low sets the 3 emphasis channel status bits to indicate 50/15 ms pre-emphasis of the transmitted audio data. If $\overline{\text{EMPH}}$ is high, then the three $\overline{\text{EMPH}}$ channel status bits are set to 000, indicating no pre-emphasis.
$\overline{\text{AUDIO}}$	19	**Audio Channel Status Bit** (*Input*) - In hardware mode A (CEN = 0), the $\overline{\text{AUDIO}}$ pin determines the state of the audio/non audio Channel Status bit in the outgoing AES3 data stream.
ORIG	28	**ORIG Channel Status Bit Control** (*Input*) - In hardware mode A (CEN = 0), the ORIG and COPY/C pins determine the state of the Copyright, Pro, and L Channel Status bits in the outgoing AES3 data stream, see Table 2.

12. APPLICATIONS

12.1 Reset, Power Down and Start-up

When $\overline{RST}$ is low, the CS8405A enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are disabled. When $\overline{RST}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 1 to the RUN bit will then cause the part to leave the low power state and begin operation.

12.2 ID Code and Revision Code

The CS8405A has a register that contains a four-bit code to indicate that the addressed device is a CS8405A. This is useful when other CS84XX family members are resident in the same or similar systems, allowing common software modules.

The CS8405A four-bit revision level code is also available. This allows the software driver for the CS8405A to identify which revision of the device is in a particular system, and modify its behavior accordingly. To allow for future revisions, it is strongly recommended that the revision code is read into a variable area within the microcontroller, and used wherever appropriate as revision details become known.

12.3 Power Supply, Grounding, and PCB layout

For most applications, the CS8405 can be operated from a single +5.0 V supply, following normal supply decoupling practices, see Figure 5. “Recommended Connection Diagram for Software Mode” on page 10. Note that the I²C protocol is supported only in VL+ = 5.0 V mode. The VL+ supplies should be decoupled with a 0.1 µF capacitor to DGND to minimize AES3 transmitter induced transients.

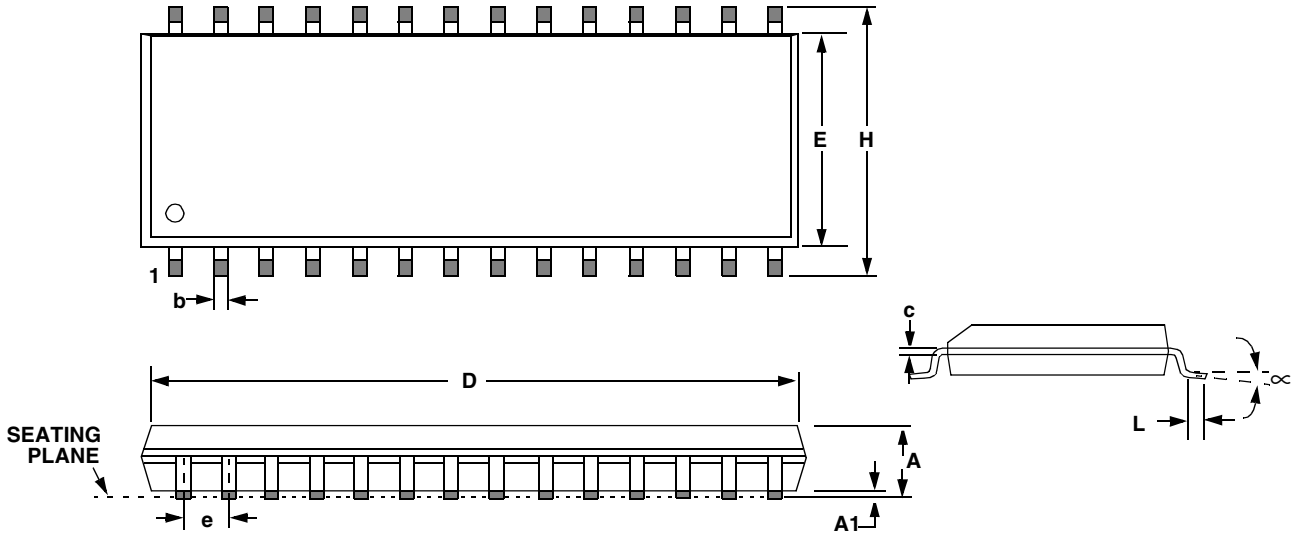
Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be mounted on the same side of the board as the CS8405A to minimize inductance effects, and all decoupling capacitors should be as close to the CS8405A as possible.

12.4 Synchronization of Multiple CS8405As

The AES3 transmitters of multiple CS8405As can be synchronized if all devices share the same master clock, TCBL, and $\overline{RST}$ signals and all exit the reset state on the same master clock falling edge. The TCBL pin is used to synchronize multiple CS8405A AES3 transmitters at the channel status block boundaries. One CS8405A must have its TCBL set to master; the others must be set to slave TCBL. Alternatively, TCBL can be derived from external logic, whereby all CS8405A devices should be set to slave TCBL.

13. PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING

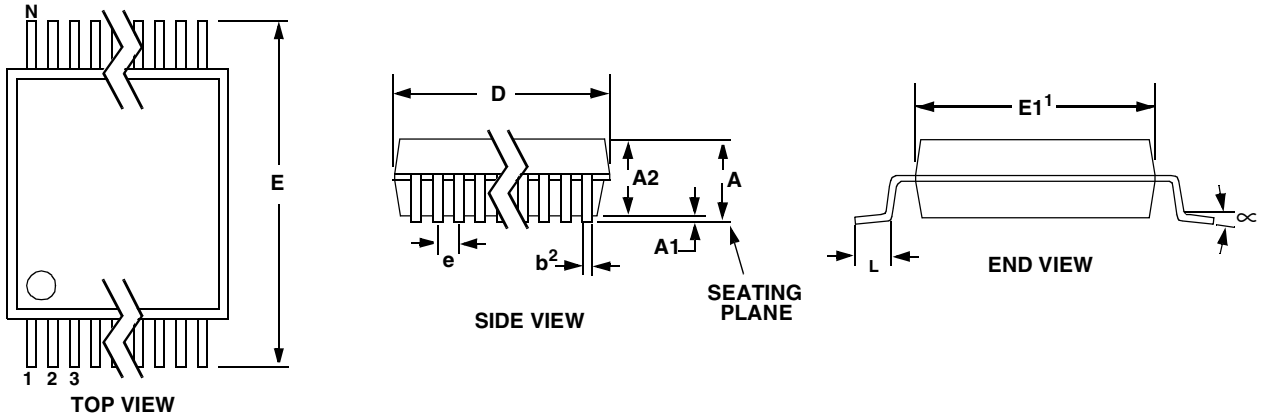


	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.093	0.098	0.104	2.35	2.50	2.65
A1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.013	0.017	0.020	0.33	0.42	0.51
C	0.009	0.011	0.013	0.23	0.28	0.32
D	0.697	0.705	0.713	17.70	17.90	18.10
E	0.291	0.295	0.299	7.40	7.50	7.60
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.394	0.407	0.419	10.00	10.34	10.65
L	0.016	0.026	0.050	0.40	0.65	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-013

Controlling Dimension is Millimeters

28L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.47	--	--	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.029	0.50	0.60	0.75	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1.“D” and “E1” are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2.Dimension “b” does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of “b” dimension at maximum material condition. Dambar intrusion shall not reduce dimension “b” by more than 0.07 mm at least material condition.

3.These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

14. APPENDIX A: EXTERNAL AES3/SPDIF/IEC60958 TRANSMITTER AND RECEIVER COMPONENTS

This section details the external components required to interface the AES3 transmitter and receiver to cables and fiber-optic components.

14.1 AES3 Transmitter External Components

The output drivers on the CS8405A are designed to drive both the professional and consumer interfaces. The AES3 specification for professional/broadcast use calls for a 110 Ω source impedance and a balanced drive capability. Since the transmitter output impedance is very low, a 110 Ω resistor should be placed in series with one of the transmit pins. The specifications call for a balanced output drive of 2-7 V peak-to-peak into a 110 Ω load with no cable attached. Using the circuit in Figure 11, the output of the transformer is short-circuit protected, has the proper source impedance, and provides a 5 V peak-to-peak signal into a 110 Ω load. Lastly, the two output pins should be attached to an XLR connector with male pins and a female shell, and with pin 1 of the connector grounded.

In the case of consumer use, the IEC60958 specifications call for an unbalanced drive circuit with an output impedance of 75 Ω and a output drive level of 0.5 V peak-to-peak ±20% when measured across a 75 Ω load using no cable. The circuit shown in Figure 12 only uses the TXP pin and provides the proper output impedance and drive level using standard 1% resistors. If VL+ is driven from +3.3 V, use resistor values of 243 Ω and 107 Ω. The connector for a consumer application would be an RCA phono socket. This circuit is also short circuit protected.

The TXP pin may be used to drive TTL or CMOS gates as shown in Figure 13. This circuit may be used for optical connectors for digital audio since they usually have TTL or CMOS compatible inputs. This circuit is also useful when driving multiple digital audio outputs since RS422 line drivers have TTL compatible inputs.

14.2 Isolating Transformer Requirements

Please refer to the application note AN134: *AES and SPDIF Recommended Transformers* for resources on transformer selection.

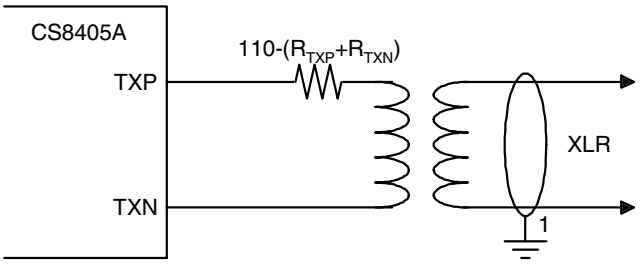


Figure 11. Professional Output Circuit

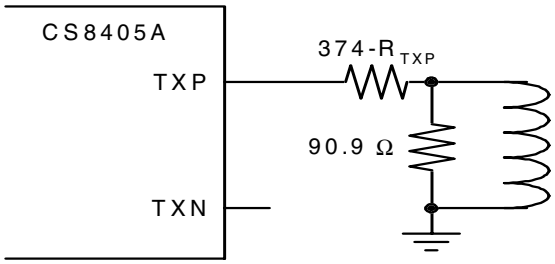


Figure 12. Consumer Output Circuit

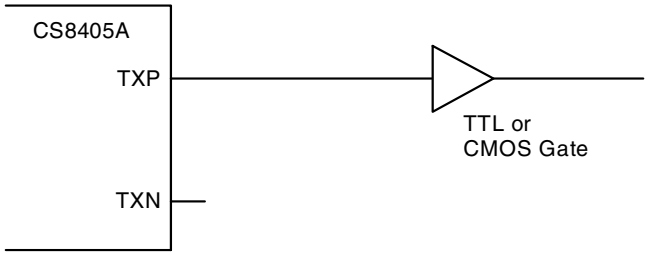


Figure 13. TTL/CMOS Output Circuit

15. APPENDIX B: CHANNEL STATUS AND USER DATA BUFFER MANAGEMENT

The CS8405A has a comprehensive channel status (C) and user (U) data buffering scheme which allows the user to manage the C and U data through the control port.

15.1 AES3 Channel Status(C) Bit Management

The CS8405A contains sufficient RAM to store a full block of C data for both A and B channels (192x2 = 384 bits), and also 384 bits of U information. The user may read from or write to these RAM buffers through the control port.

The CS8405A manages the flow of channel status data at the block level, meaning that entire blocks of channel status information are buffered at the input, synchronized to the output timebase, and then transmitted. The buffering scheme involves a cascade of 2 block-sized buffers, named E and F, as shown in Figure 14. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 20h) is the consumer/professional bit for channel status block A.

The E buffer is accessible from the control port, allowing read and writing of the C data. The F buffer is used as the source of C data for the AES3 transmitter. The F buffer accepts block transfers from the E buffer.

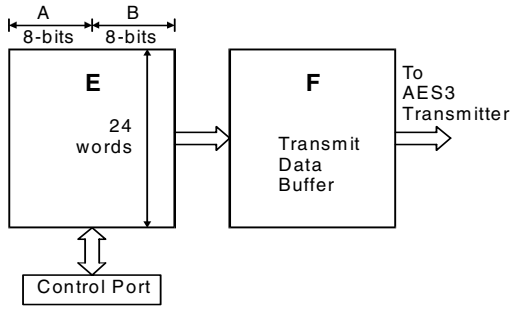


Figure 14. Channel Status Data Buffer Structure

15.1.1 Accessing the E buffer

The user can monitor the data being transferred by reading the E buffer, which is mapped into the register space of the CS8405A, through the control port. The user can modify the data to be transmitted by writing to the E buffer.

The user can configure the interrupt enable register to cause interrupts to occur whenever “E to F” buffer transfers occur. This allows determination of the allowable time periods to interact with the E buffer.

Also provided is an “E to F” inhibit bit. The “E to F” buffer transfer is disabled whenever the user sets this bit. This may be used whenever “long” control port interactions are occurring.

A flowchart for reading and writing to the E buffer is shown in Figure 15. For writing, the sequence starts after a E to F transfer, which is based on the output timebase.

If the channel status block to transmit indicates PRO mode, then the CRCC byte is automatically calculated by the CS8405A, and does not have to be written into the last byte of the block by the host microcontroller. This is also true if the channel status data is entered serially through the COPY/C pin when the part is in hardware mode.

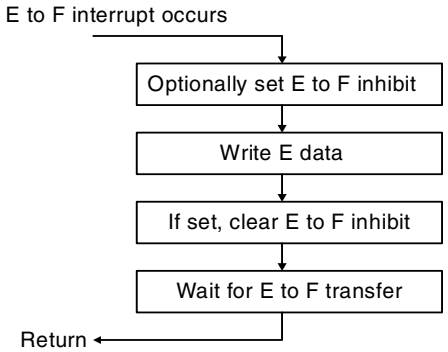


Figure 15. Flowchart for Writing the E Buffer

15.1.2 Serial Copy Management System (SCMS)

In software mode, the CS8405A allows read/modify/write access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to manipulate the Category Code, Copy bit and L bit appropriately.

In hardware mode, the SCMS protocol can be followed by either using the COPY and ORIG input pins, or by using the C bit serial input pin. These options are documented in the hardware mode section of this data sheet.

15.1.3 Channel Status Data E Buffer Access

The E buffer is organized as 24 x 16-bit words. For each word the MS Byte is the A channel data, and the LS Byte is the B channel data (see Figure 14).

There are two methods of accessing this memory, known as one byte mode and two byte mode. The desired mode is selected through a control register bit.

15.1.3.1 One Byte mode

In many applications, the channel status blocks for the A and B channels will be identical. In this situation, if the user reads a byte from one of the channel's blocks, the corresponding byte for the other channel will be the same. Similarly, if the user wrote a byte to one channel's block, it would be necessary to write the same byte to the other block. One byte mode takes advantage of the often identical nature of A and B channel status data.

When reading data in one byte mode, a single byte is returned, which can be from channel A or B data, depending on a register control bit. If a write is being done, the CS8405A expects a single byte to be input to its control port. This byte will be written to both the A and B locations in the addressed word.

One byte mode saves the user substantial control port access time, as it effectively accesses 2 bytes worth of information in 1 byte's worth of access time. If the control port's auto increment addressing is used in combination with this mode, multi-byte accesses such as full-block reads or writes can be done especially efficiently.

15.1.3.2 Two Byte mode

There are those applications in which the A and B channel status blocks will not be the same, and the user is interested in accessing both blocks. In these situations, two byte mode should be used to access the E buffer.

In this mode, a read will cause the CS8405A to output two bytes from its control port. The first byte out will represent the A channel status data, and the 2nd byte will represent the B channel status data. Writing is similar, in that two bytes must now be input to the CS8405A's control port. The A channel status data is first, B channel status data second.

15.2 AES3 User (U) Bit Management

The CS8405A U bit manager has two operating modes:
Mode 1. Transmit all zeros.
Mode 2. Block mode.

15.2.1 Mode 1: Transmit All Zeros

Mode 1 causes only zeros to be transmitted in the output U data, regardless of E buffer contents. This mode is intended for the user who wants the output U channel to contain no data.

15.2.2 Mode 2: Block Mode

Mode 2 is very similar to the scheme used to control the C bits. Entire blocks of U data are buffered using 2 block-sized RAMs to perform the buffering. The user has access to the first buffer, denoted the E buffer, through the control port. It is the only mode in which the user can merge his own U data into the transmitted AES3 data stream. The U buffer access only operates in two byte mode, since there is no concept of A and B blocks for user data. The arrangement of the data is as follows: Bit15[A7]Bit14[B7]Bit13[A6]Bit12[B6]...Bit1[A0] Bit0[B0]. The arrangement of the data in each byte is that the MSB is the first transmitted bit. The bit for the A subframe is followed by the bit for the B subframe.

16. REVISION HISTORY

Release	Date	Changes
PP1	November 1999	1st Preliminary Release
PP2	November 2000	2nd Preliminary Release
PP3	May 2001	3rd Preliminary Release
PP4	June 2002	4th Preliminary Release
PP5	March 2003	5th Preliminary Release
F1	January 2004	Final Release
F2	August 2004	Added lead-free device ordering information.

Table 5. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**