

Power MOSFET

-20 V, -5.8 A, Single P-Channel, TSOP-6

Features

- Low $R_{DS(on)}$ in TSOP-6 Package
- 1.8 V Gate Rating
- Fast Switching
- This is a Pb-Free Device

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- High Side Load Switch
- Switching Circuits for Game Consoles, Camera Phone, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DS}	-20	V
Gate-to-Source Voltage			V_{GS}	± 8.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-5.1	A
		$T_A = 85^\circ\text{C}$		-3.6	
	$t \leq 5 \text{ s}$	$T_A = 25^\circ\text{C}$		-5.8	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.25	W
	$t \leq 5 \text{ s}$			1.6	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-3.7	A
		$T_A = 85^\circ\text{C}$		-2.7	
Power Dissipation (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$		I_{DM}	-20	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

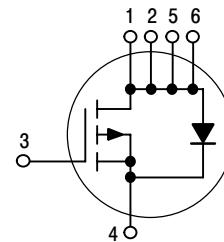


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$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
-20 V	25 m Ω @ -4.5 V	-5.1 A
	32 m Ω @ -2.5 V	-4.5 A
	41 m Ω @ -1.8 V	-2.5 A

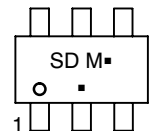
P-Channel



MARKING DIAGRAM

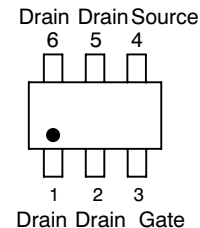


TSOP-6
CASE 318G
STYLE 1



SD = Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NTGS3136PT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTGS3136P

热阻/电阻率/最大额定值

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	77	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	185	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
 4. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μA	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μA , Reference 25°C		-13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = -20$ V			-1.0	μA
					-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 0.1	μA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μA	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -5.1$ A		25	33	m Ω
		$V_{GS} = -2.5$ V, $I_D = -4.5$ A		32	40	
		$V_{GS} = -1.8$ V, $I_D = -2.5$ A		41	51	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0$ V, $I_D = -5.1$ A		22		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -10$ V		1901		pF
Output Capacitance	C_{OSS}			274		
Reverse Transfer Capacitance	C_{RSS}			175		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V; $I_D = -5.1$ A		18	29	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate-to-Source Charge	Q_{GS}			2.4		
Gate-to-Drain Charge	Q_{GD}			4.3		
Gate Resistance	R_G			7.6		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DD} = -10$ V, $I_D = -1.0$ A, $R_G = 6.0$ Ω		9	19	ns
Rise Time	T_r			9	19	
Turn-Off Delay Time	$t_{d(OFF)}$			99	160	
Fall Time	T_f			48	79	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = -1.7$ A	$T_J = 25^\circ\text{C}$		-0.7	-1.2	V
			$T_J = 125^\circ\text{C}$		-0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ μs , $I_S = -1.7$ A			37	60	ns

5. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$
 6. Switching characteristics are independent of operating junction temperatures

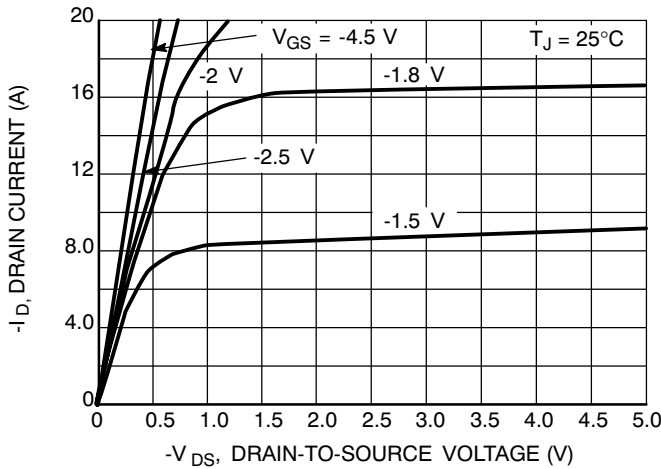


Figure 1. On-Region Characteristics

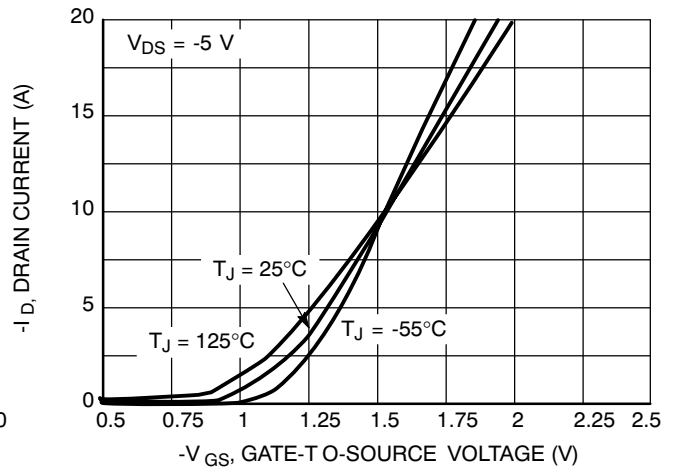


Figure 2. Transfer Characteristics

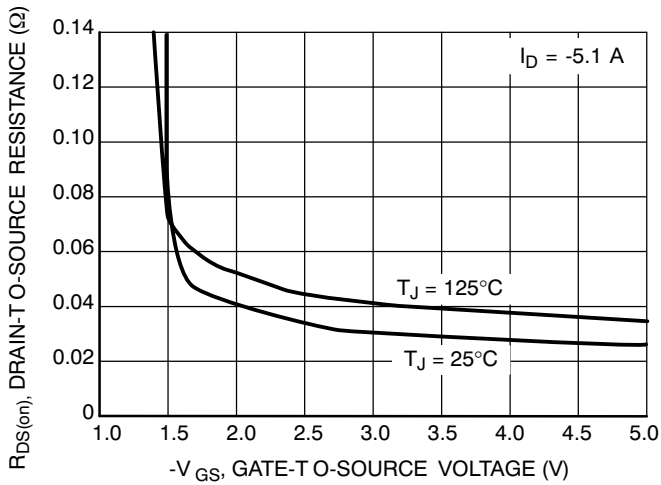


Figure 3. On-Resistance vs. Gate-to-Source Voltage

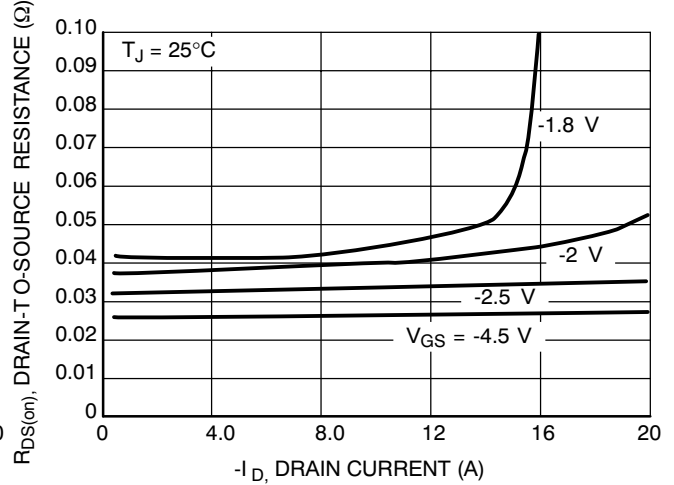


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

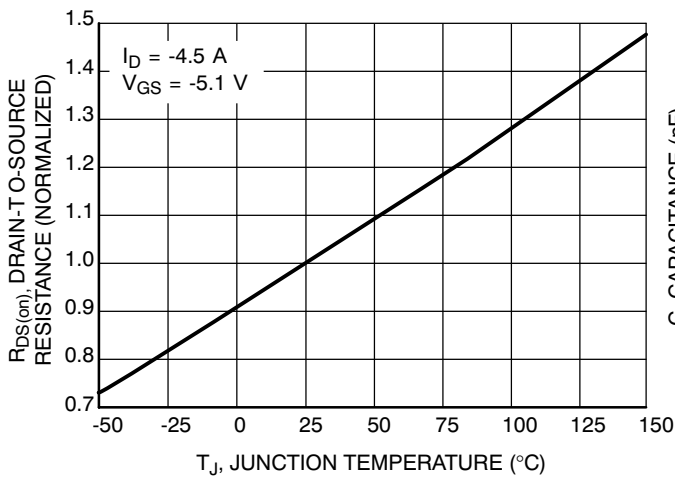


Figure 5. On-Resistance Variation with Temperature

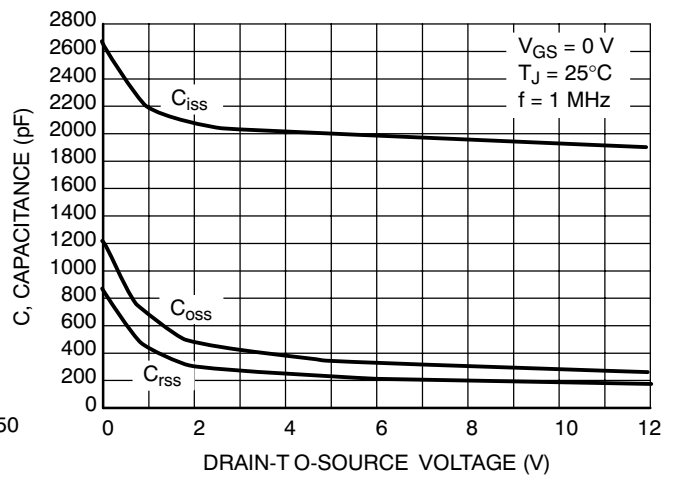


Figure 6. Capacitance Variation

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TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

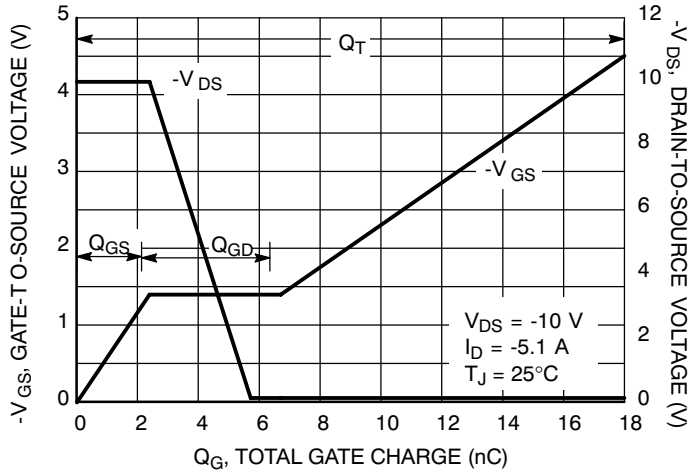


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

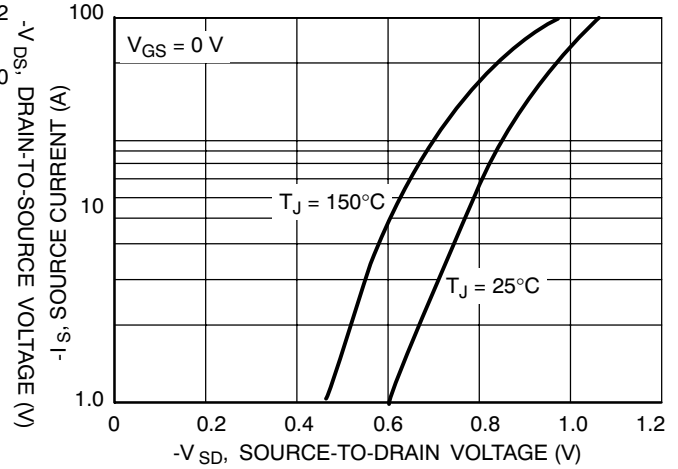


Figure 8. Diode Forward Voltage vs. Current

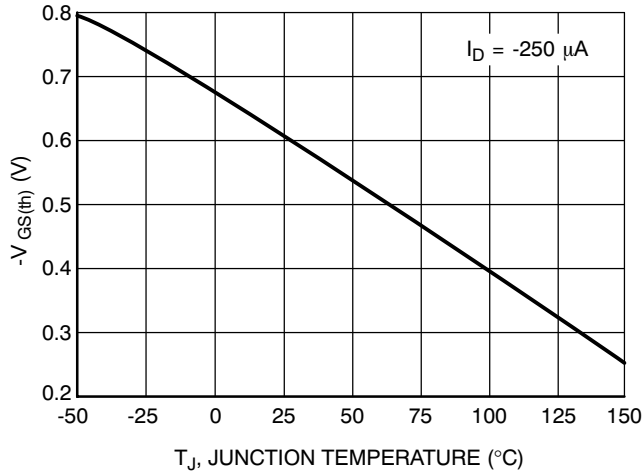


Figure 9. Threshold Voltage

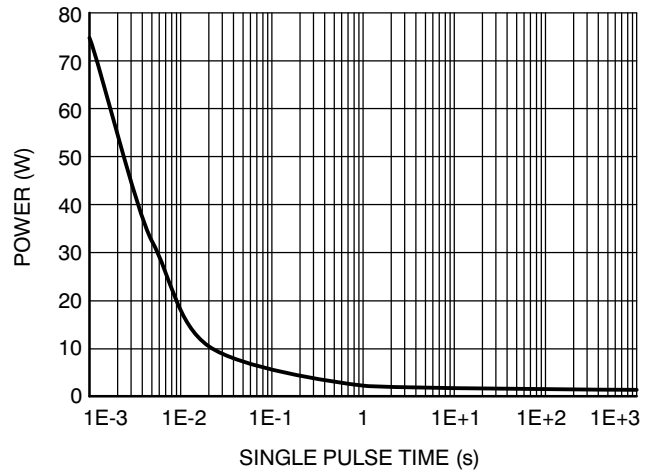


Figure 10. Single Pulse Maximum Power Dissipation

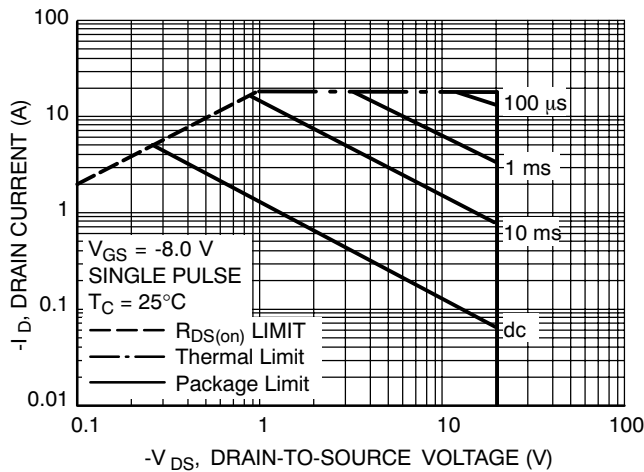


Figure 11. Maximum Rated Forward Biased Safe Operating Area

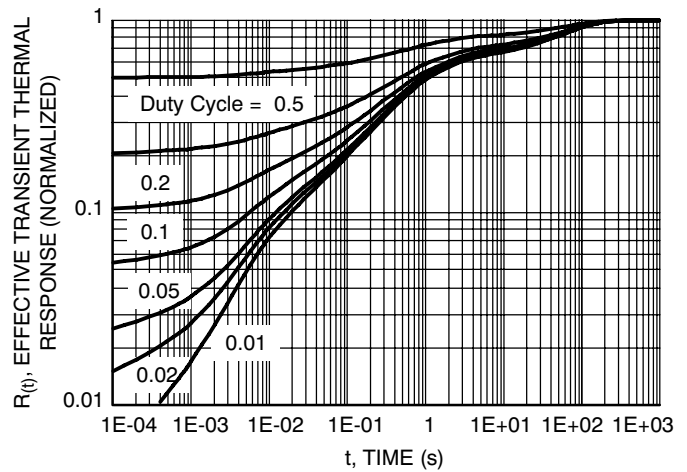


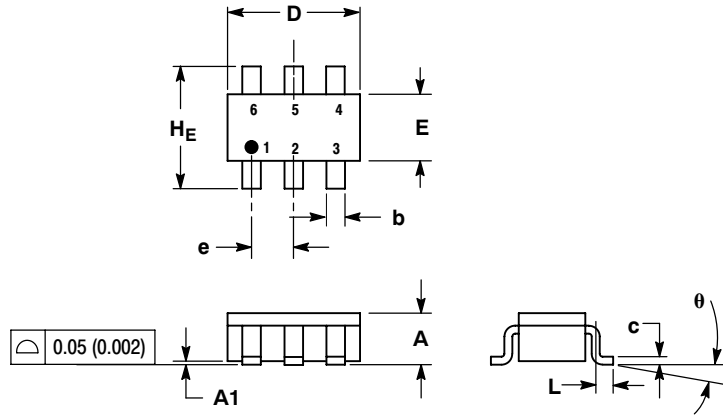
Figure 12. FET Thermal Response

NTGS3136P

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PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE S



NOTES:

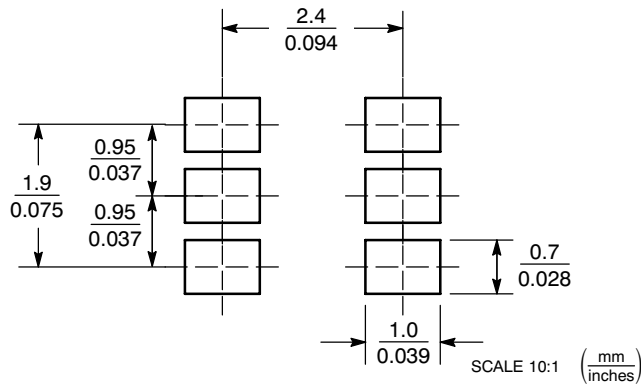
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°


STYLE 1:

- PIN 1. DRAIN
- 2. DRAIN
- 3. GATE
- 4. SOURCE
- 5. DRAIN
- 6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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