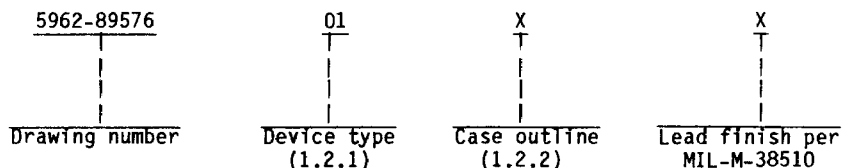




1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	UT1553B RTR	Remote terminal interface with 1K X 16 RAM

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

<u>Outline letter</u>	<u>Case outline</u>
X	P-BC, (68-pin, 1.135" x 1.135" x .345"), pin grid array package
Y	C-G5, (68-terminal, .960" x .960" x .135"), leaded chip carrier with unformed leads
Z	C-7, (68-terminal, .962" x .962" x .120"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range, ( $V_{DD}$ )	- - - - -	-0.3 V dc minimum to +7.0 V dc maximum
DC input/dc output voltage range	- - - - -	-0.3 V dc minimum to +7.3 V dc maximum
Storage temperature range	- - - - -	-65°C to +150°C
Maximum power dissipation, ( $P_D$ )	- - - - -	300 mW 1/
Maximum junction temperature ( $T_J$ )	- - - - -	+175°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ )	- - - - -	See MIL-M-38510, appendix C
Latchup immunity ( $I_{LU}$ )	- - - - -	±150 mA
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C

1.4 Recommended operating conditions.

Supply voltage ( $V_{DD}$ )	- - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage ( $V_{IH}$ )	- - - - -	5.5 V dc
Maximum low level input voltage ( $V_{IL}$ )	- - - - -	0.0 V dc
Case operating temperature range ( $T_C$ )	- - - - -	-55°C to +125°C
Operating frequency ( $F_0$ )	- - - - -	12 MHz

1/ Must withstand the added  $P_D$  due to short circuit test, e.g.,  $I_{OS}$ .

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET <b>2</b>

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 3

**TABLE I. Electrical performance characteristics.**

Test	Symbol	Conditions 4.5 V < V <sub>DD</sub> < 5.5 V -55°C < T <sub>C</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
Low level input voltage	V <sub>IL</sub>		1,2,3		0.8	V
High level input voltage	V <sub>IH</sub>			2.0		
Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub> V <sub>IN</sub> = V <sub>DD</sub> V <sub>IN</sub> = V <sub>SS</sub>		-1 110 -2000	1 2000 -110	μA
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA			0.4	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA		2.4		
Three-state output leakage current	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>DD</sub> or V <sub>SS</sub>		-10	10	μA
Short-circuit output current <u>1/</u> <u>2/</u>	I <sub>OS</sub>	V <sub>DD</sub> = 5.5 V, V <sub>O</sub> = V <sub>DD</sub> V <sub>DD</sub> = 5.5 V, V <sub>O</sub> = 0 V		-90	90	mA
Quiescent current <u>3/</u>	I <sub>IDD</sub>				1.5	
Average operating current <u>1/4/</u>	I <sub>DD</sub>	F = 12 MHz, C <sub>L</sub> = 50 pF			50	
Input capacitance	C <sub>IN</sub>	See 4.3.1.c	4		10	pF
Output capacitance	C <sub>OUT</sub>				15	
Bidirectional I/O capacitance	C <sub>I/O</sub>				20	
Functional tests		See 4.3.1.d	7,8			

See footnotes at the end of table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET <b>4</b>

TABLE I Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V < V <sub>DD</sub> < 5.5 V -55°C < T <sub>C</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{CTRL}(H)$ set up wrt $\overline{CS}(L)$ 5/	t <sub>1</sub>	See figure 3 1/ Microprocessor RAM read cycle	9,10,11	10		ns
RD/ $\overline{WR}(H)$ set up wrt $\overline{CS}(L)$	t <sub>2</sub>			10		
ADDR(9:0) valid to $\overline{CS}(L)$ (address set up)	t <sub>3</sub>			10		
$\overline{CS}(L)$ to DATA(15:0) valid 5/	t <sub>4</sub>				155	
$\overline{OE}(L)$ to DATA(15:0) don't care (active)	t <sub>5</sub>				65	
$\overline{CS}(H)$ to $\overline{CTRL}$ don't care	t <sub>6</sub>			0		
$\overline{CS}(H)$ to ADDR(9:0) don't care	t <sub>7</sub>			0		
$\overline{OE}(H)$ to DATA(15:0) high impedance	t <sub>8</sub>				40	
$\overline{CS}(L)$ to $\overline{CS}(H)$ 6/	t <sub>9</sub>			220	5500	
$\overline{CS}(H)$ to $\overline{CS}(L)$	t <sub>10</sub>			85		
$\overline{CS}(H)$ to RD/ $\overline{WR}$ don't care	t <sub>11</sub>			0		
$\overline{CS}(H)$ to DATA(15:0) invalid 7/	t <sub>12</sub>			25		
$\overline{OE}(L)$ to $\overline{OE}(H)$	t <sub>13</sub>			65		

See footnotes at the end of the table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V < V <sub>DD</sub> < 5.5 V -55°C < T <sub>C</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
$\overline{CTRL}$ (H) set up wrt $\overline{CS}$ (L)	t <sub>1</sub>	See figure 3 1/ Microprocessor RAM write cycle	9,10,11	10		ns
RD/ $\overline{WR}$ (L) set up wrt $\overline{CS}$ (L)	t <sub>14</sub>			10		
ADDR(9:0) valid to $\overline{CS}$ (L) (address set up)	t <sub>3</sub>			10		
DATA(15:0) valid to $\overline{CS}$ (L) (DATA set up)	t <sub>15</sub>			0		
$\overline{OE}$ (H) to DATA(15:0) high impedance	t <sub>16</sub>			40		
$\overline{CS}$ (H) to RD/ $\overline{WR}$ don't care	t <sub>11</sub>			0		
$\overline{CS}$ (H) to ADDR(9:0) don't care	t <sub>7</sub>			0		
$\overline{CS}$ (H) to DATA(15:0) don't care	t <sub>17</sub>			20		
$\overline{CS}$ (L) to $\overline{CS}$ (H) 6/	t <sub>18</sub>			180	5500	
$\overline{CS}$ (H) to $\overline{CS}$ (L)	t <sub>10</sub>			85		
$\overline{CS}$ (H) to $\overline{CTRL}$ don't care	t <sub>6</sub>			0		

See footnotes at the end of the table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 6

TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V ≤ V <sub>DD</sub> ≤ 5.5 V -55°C < T <sub>c</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
CTRL(L) set up wrt CS(L)	t <sub>19</sub>	See figure 3 1/ Control register write cycle	9,10,11	0		ns
RD/WR(L) set up wrt CS(L)	t <sub>20</sub>			0		
CS(L) to CS(H) 6/	t <sub>21</sub>			50	5500	
CS(H) to DATA(15:0) don't care (hold time)	t <sub>22</sub>			0		
CS(H) to CTRL don't care	t <sub>6</sub>			0		
CS(H) to RD/WR don't care	t <sub>11</sub>			0		
OE(H) to DATA(15:0) high impedance	t <sub>23</sub>			40		
DATA(15:0) valid to CS(L) (DATA setup)	t <sub>15</sub>			0		
CTRL(L) set up wrt CS (L)	t <sub>19</sub>			See figure 3 1/ Status register read cycle		
CS(L) to CS(H) 6/	t <sub>24</sub>	65	5500			
RD/WR(H) set up wrt CS(L)	t <sub>25</sub>	0				
CS(L) to DATA(15:0) valid	t <sub>26</sub>		65			
CS(H) to CTRL don't care	t <sub>27</sub>	5				
CS(H) to RD/WR don't care	t <sub>28</sub>	5				
OE(L) to DATA(15:0) valid 5/ don't care(active)	t <sub>5</sub>		65			
OE(H) to DATA(15:0) high impedance	t <sub>8</sub>		40			

See footnotes at the end of the table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 7

DESC FORM 193A  
SEP 87

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V < V <sub>DD</sub> < 5.5 V -55°C < T <sub>C</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
OE(L) to OE(H)	t <sub>13</sub>	See figure 3 1/ Status register read cycle	9,10,11	65		
CS(L) to DATA(15:0) don't care	t <sub>29</sub>			25		
VALMSG(H) before TIMERON(L)	t <sub>30</sub>	See figure 3 1/ RT failsafe timer signal relationships		0	35	ns
TIMERON(L) before first biphase out zero(H)	t <sub>31</sub>				1.2	μs
TIMERON low pulse width (time-out)	t <sub>32</sub>			727.3	727.4	
COMSTR(L) to TIMERON(H)	t <sub>33</sub>				25	ns
VALMSG(H) to ILLCOM(H) 8/	t <sub>34</sub>				3.3	μs
COMSTR(L) to ILLCOM(H) 9/	t <sub>35</sub>			664	ns	
COMSTR(L) to ILLCOM(H) 9/	t <sub>35</sub>			18.2	μs	
ILLCOM(H) to ILLCOM(L) 10/	t <sub>36</sub>			500	ns	
12MHz(H) to MC/SA valid	t <sub>37</sub>	See figure 3 Status output timing		0	14	ns
Command word to MC/SA Valid 1/ 11/	t <sub>38</sub>			2.1	2.8	μs
12MHz(H) to COMSTR(L)	t <sub>39</sub>			0	17	ns
Command word to COMSTR(L) 1/ 11/	t <sub>40</sub>			3.2	3.7	μs
12MHz(H) to BRDCST(L)	t <sub>41</sub>			0	32	ns
Command word to BRDCST(L) 1/ 11/	t <sub>42</sub>			2.6	3.2	μs

See footnotes at the end of the table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 8

DESC FORM 193A  
SEP 87

\* U. S. GOVERNMENT PRINTING OFFICE: 1988-549-904



TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4.5 V < V <sub>DD</sub> < 5.5 V -55°C < T <sub>C</sub> < 125°C unless otherwise specified	Group A subgroups	Limits		Units
				Min	Max	
12MHz(H) to T/R valid	t43	See figure 3 Status output timing	9,10,11	0	57	ns
Command word to T/R valid <u>1/ 11/</u>	t44			2.2	2.7	μs
12MHz(H) to VALMSG(H)	t45			0	32	ns
Command word to VALMSG(H) <u>1/ 11/ 12/</u>	t46			6.2	6.7	μs
12MHz(H) to MERR(H)	t47			0	37	ns
COMSTR(L) to COMSTR(H) <u>1/</u>	t48			485	500	
12MHz(H) to RBUSY(H) <u>1/</u>	t49			0	37	
Command word to RBUSY(H) <u>1/</u>	t50			3.2	3.8	μs
12MHz(H) to TERACTION(L)	t51			0	37	ns
Command word to TERACTION(L) <u>1/ 11/</u>	t52			3.1	3.7	μs
12MHz(H) to RTRT(H)	t53			0	32	ns
Command word to RTRT(H) <u>1/ 11/</u>	t54			21.0	22.0	μs
MRST(L) to MRST(H) <u>1/</u>	t55			500		ns
RBUSY(H) to RBUSY(L) (2.7 μs) <u>1/ 6/</u> (5.7 μs)	t56				5.5 8.5	μs
RBUSY(L) to RBUSY(H) (2.7 μs) <u>1/ 6/</u> (5.7 μs)	t57				3.10 240	μs ns

See footnotes at the end of table.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89756
	REVISION LEVEL	SHEET 9

- 1/ Guaranteed to the limits specified in table I, if not tested
- 2/ Not more than one output may be shorted at a time for a maximum duration of one second.
- 3/ All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.
- 4/ Includes current input pull-ups. Instantaneous surge currents on the order of 1.0 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
- 5/ "wrt" defined as "with respect to".
- 6/ The maximum amount of time that  $\overline{CS}$  can be held low is 5500 ns if the user has selected the 5.7  $\mu s$  RBUSY option. For the 2.7  $\mu s$  RBUSY option, the maximum  $\overline{CS}$  low time is 2500 ns.
- 7/ Assumes  $\overline{OE}$  is asserted.
- 8/ The ILLCOM pin must be asserted within 3.3  $\mu s$  after VALMSG goes to a logic 1 if the RTR is to respond with the message error bit of the status word at a logic 1.
- 9/ If the illegal command is mode code 2, 4, 5, 6, 7 or 18, the ILLCOM pin must be asserted within 664 ns after command strobe (COMSTR) transitions to logic 0. Asserting the ILLCOM pin within the 664 ns inhibits the mode code function.  
For an illegal receive command, the ILLCOM pin is asserted within 18.2  $\mu s$  after the COMSTR transitions to a logic 0 in order to suppress data words from being stored. In addition, the ILLCOM pin must be at a logic 1 throughout the reception of the message until VALMSG is asserted. This does not apply to illegal transmit commands since the status word is transmitted first.
- 10/ For transmit command illegalization.
- 11/ Command word measured from mid-bit crossing.
- 12/ Receive last data word to Valid Message active (VALMSG(H)).  
Transmit command word to Valid Message active (VALMSG(H)).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 10

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A2	MCSA1	C11	DATA14	J10	DATA3
A3	MCSA2	D1	ADDR7	J11	DATA4
A4	MCSA4	D2	ADDR8	K1	RD/WR
A5	MERR	D10	DATA11	K2	CS
A6	TERACT	D11	DATA12	K3	MRST
A7	BRDCST	E1	V <sub>DD</sub>	K4	RTA3
A8	2MHZ	E2	ADDR6	K5	RTA1
A9	TBZ	E10	DATA9	K6	RTPTY
A10	TAZ	E11	DATA10	K7	RBO
B1	MC/SA	F1	ADDR5	K8	RAO
B2	MCSA0	F2	V <sub>SS</sub>	K9	ILLCOM
B3	MCSA3	F10	V <sub>DD</sub>	K10	DATA1
B4	T/R	F11	DATA8	K11	DATA2
B5	TXERR	G1	ADDR3	L2	12MHZ
B6	TIMERON	G2	ADDR4	L3	RTA4
B7	RTRT	G10	DATA7	L4	RTA2
B8	COMSTR	G11	V <sub>SS</sub>	L5	RTA0
B9	TBO	H1	ADDR1	L6	RBZ
B10	TA0	H2	ADDR2	L7	RAZ
B11	DATA15	H10	DATA5	L8	VALMSG
C1	ADDR9	H11	DATA6	L9	DE
C2	RBUSY	J1	CTRL	L10	DATA0
C10	DATA13	J2	ADDRO		

FIGURE 1. Terminal connections.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576	
		REVISION LEVEL	SHEET 11

Device type		01			
Case outlines		Y and Z			
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
01	VSS	24	ILLCOM	47	TBZ
02	ADDR5	25	OE	48	COMSTR
03	ADDR4	26	DATA0	49	2MHZ
04	ADDR3	27	DATA1	50	RTRT
05	ADDR2	28	DATA2	51	BRDCST
06	ADDR1	29	DATA3	52	TIMERON
07	ADDR0	30	DATA4	53	TERACT
08	CTRE	31	DATA5	54	TXERR
09	RD/WR	32	DATA6	55	MERR
10	CS	33	DATA7	56	T/R
11	12MHZ	34	VSS	57	MCSA4
12	MRST	35	VDD	58	MCSA3
13	RTA4	36	DATA8	59	MCSA2
14	RTA3	37	DATA9	60	MCSA1
15	RTA2	38	DATA10	61	MCSA0
16	RTA1	39	DATA11	62	MC/SA
17	RTA0	40	DATA12	63	RBUSY
18	RTPTY	41	DATA13	64	ADDR9
19	RBZ	42	DATA14	65	ADDR8
20	RBO	43	DATA15	66	ADDR7
21	RAZ	44	TAO	67	ADDR6
22	RAO	45	TAZ	68	VDD
23	VALMSG	46	TBO		

FIGURE 1. Terminal connections - Continued.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 12

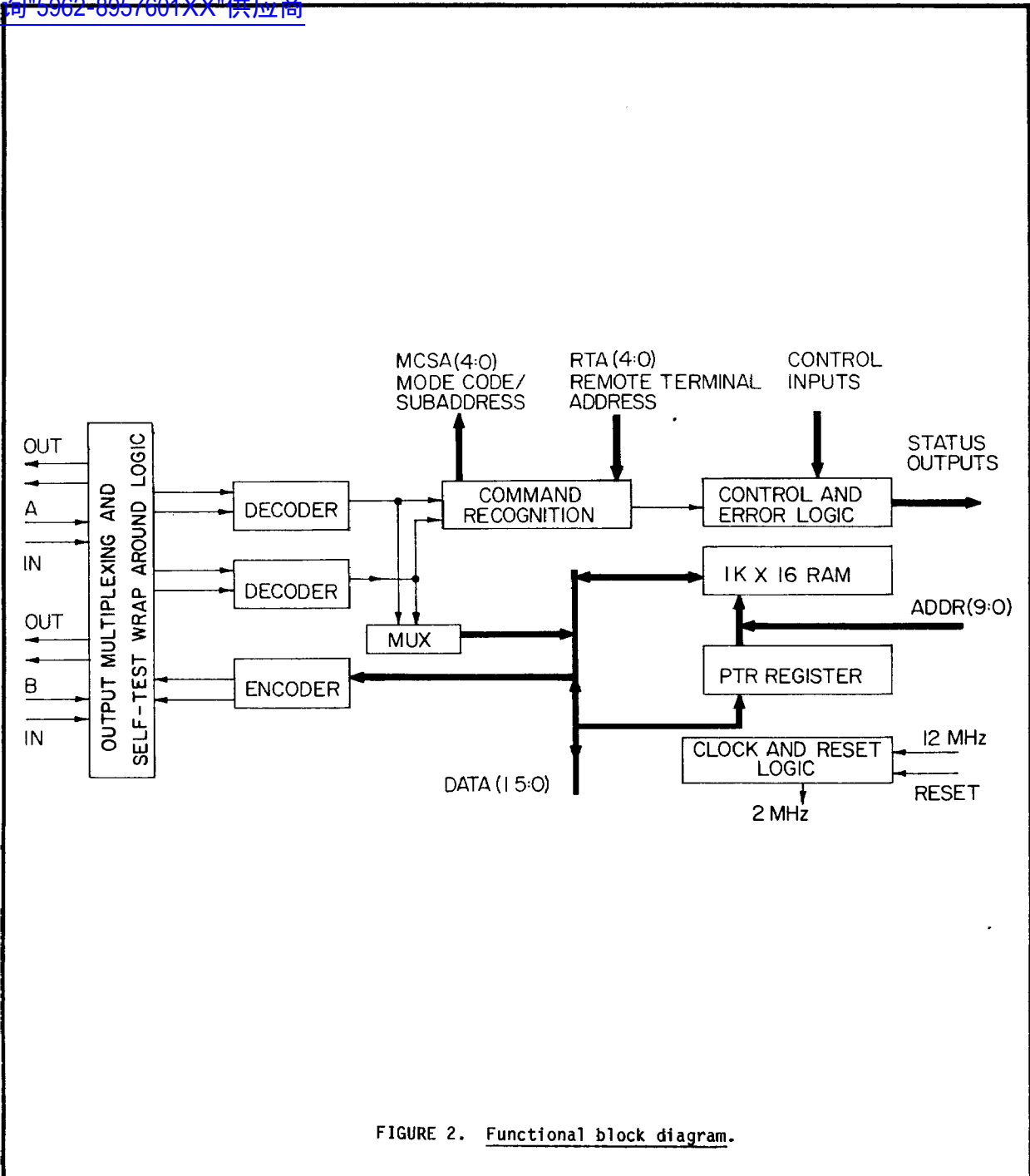
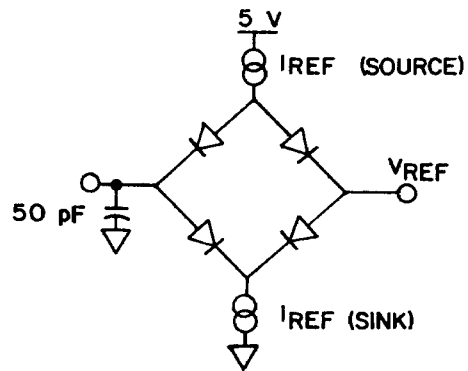


FIGURE 2. Functional block diagram.

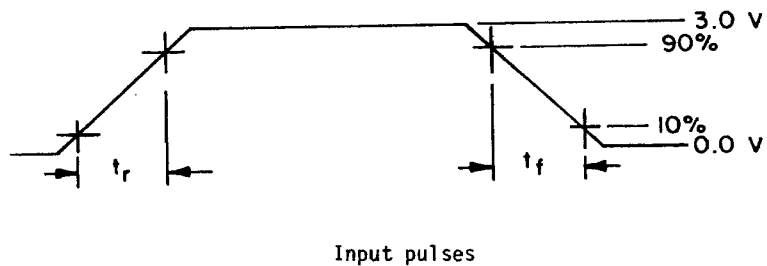
<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 13

DESC FORM 193A  
SEP 87

U. S. GOVERNMENT PRINTING OFFICE: 1988-550-547



NOTE: 50 pF including scope probe and test socket,  
 $V_{REF} = (V_{OL \text{ maximum}} + V_{OH \text{ minimum}})/2$



NOTE:  $t_r = t_f < 2 \text{ ns}$

FIGURE 3. Switching test circuit and waveforms.

<b>STANDARDIZED                  MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 14

DESC FORM 193A  
 SEP 87

\* U. S. GOVERNMENT PRINTING OFFICE: 1988-550-547

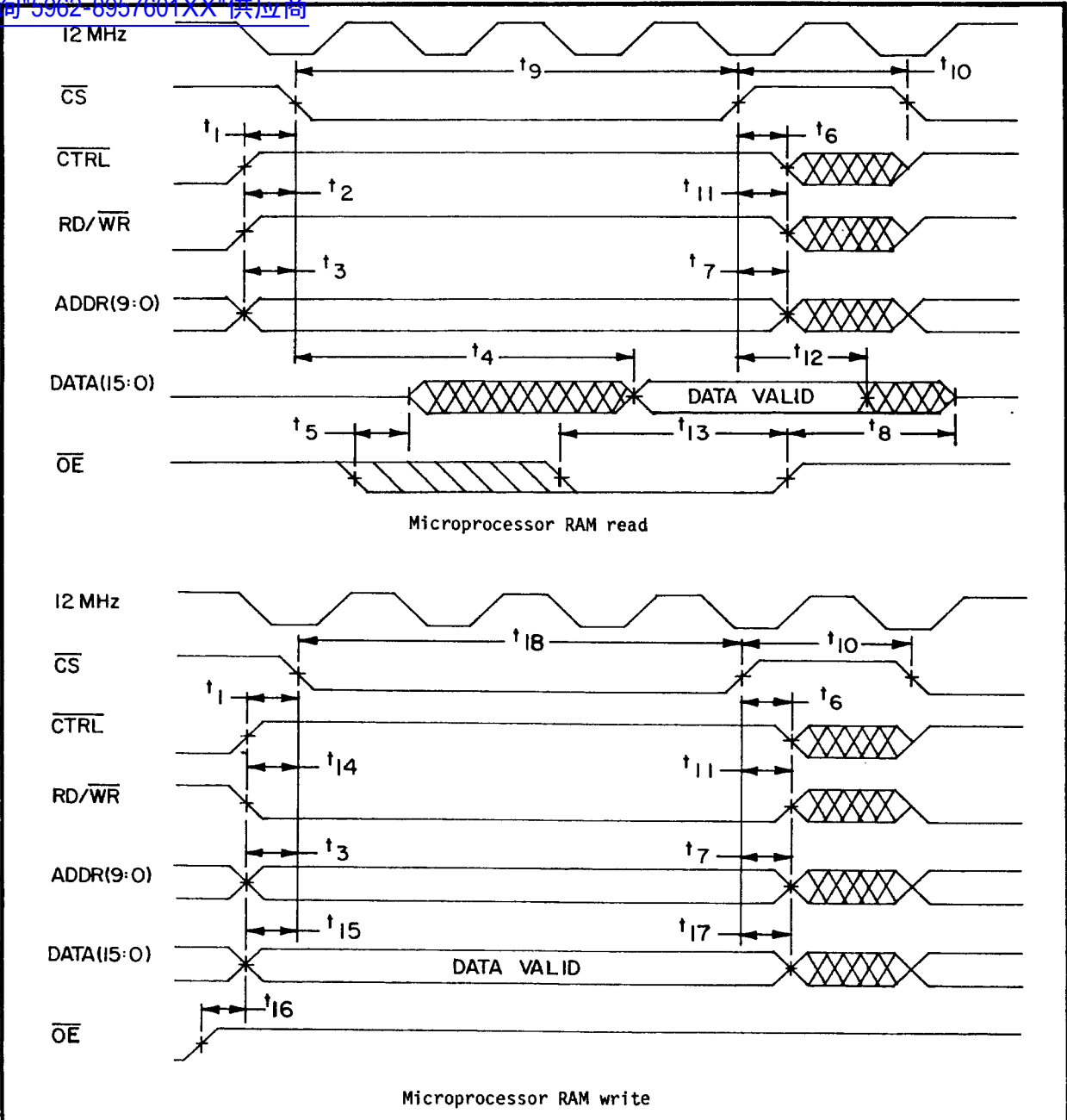
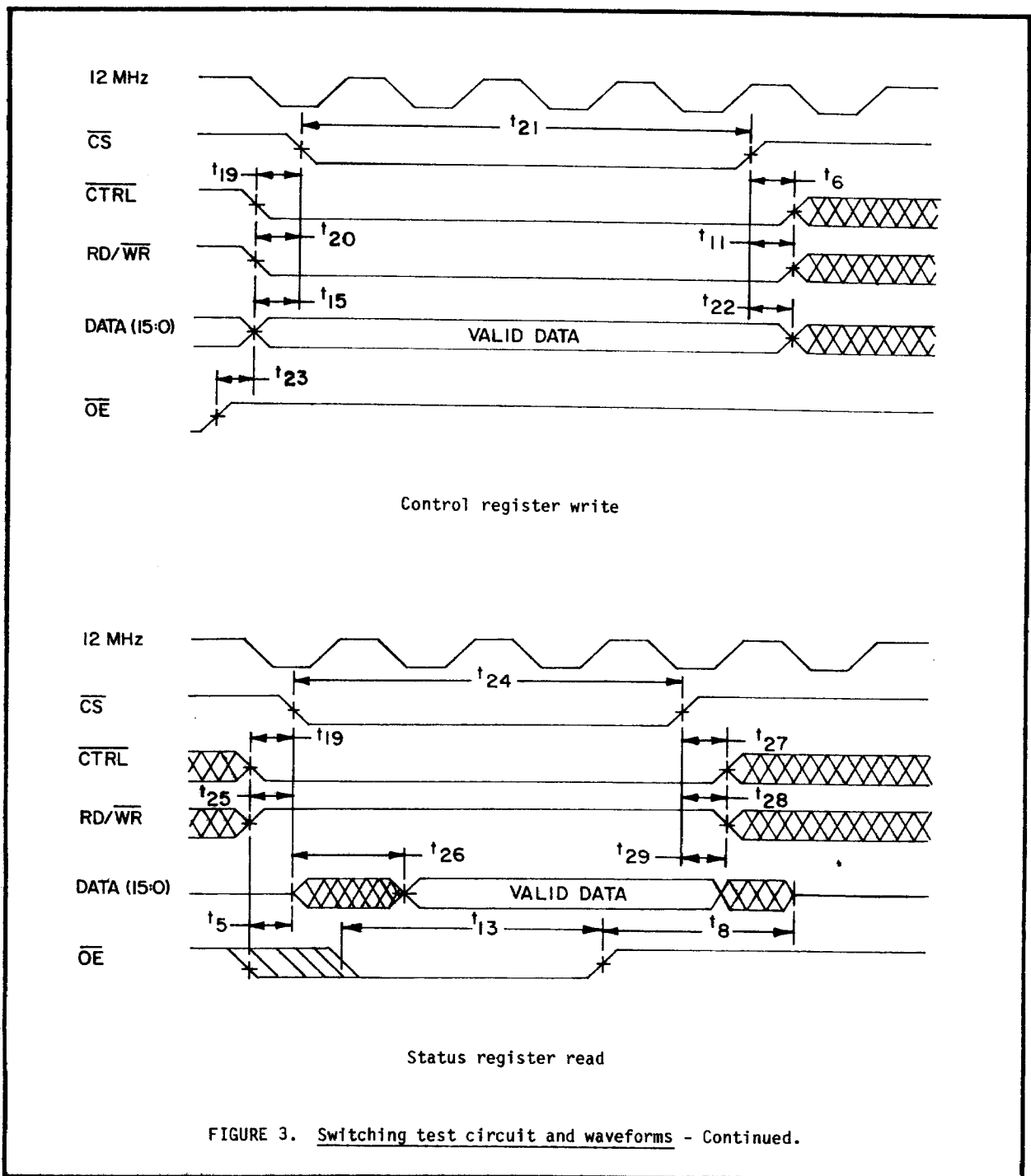


FIGURE 3. Switching test circuit and waveforms - Continued.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 15

DESC FORM 193A  
SEP 87

U. S. GOVERNMENT PRINTING OFFICE: 1988-550-547

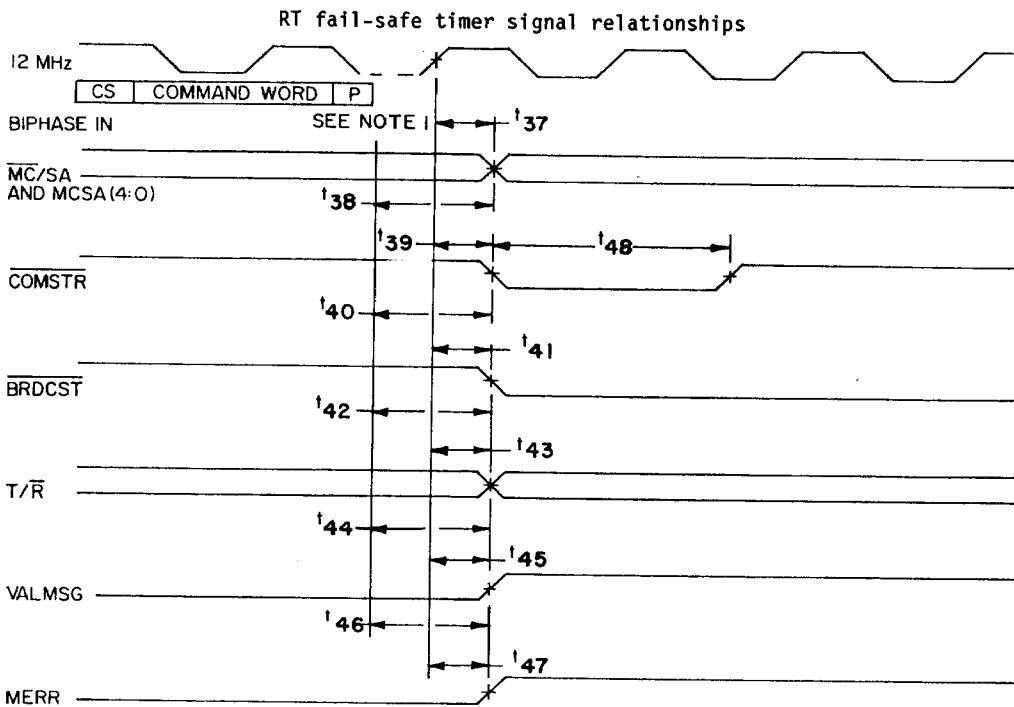
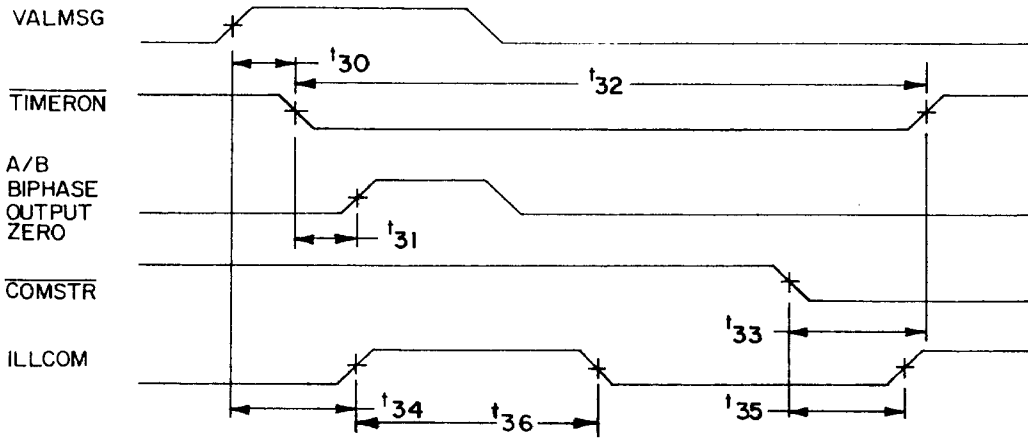


<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 16

DESC FORM 193A  
SEP 87

U. S. GOVERNMENT PRINTING OFFICE: 1988-550-547





NOTE: Measured from the mid-bit parity crossing.

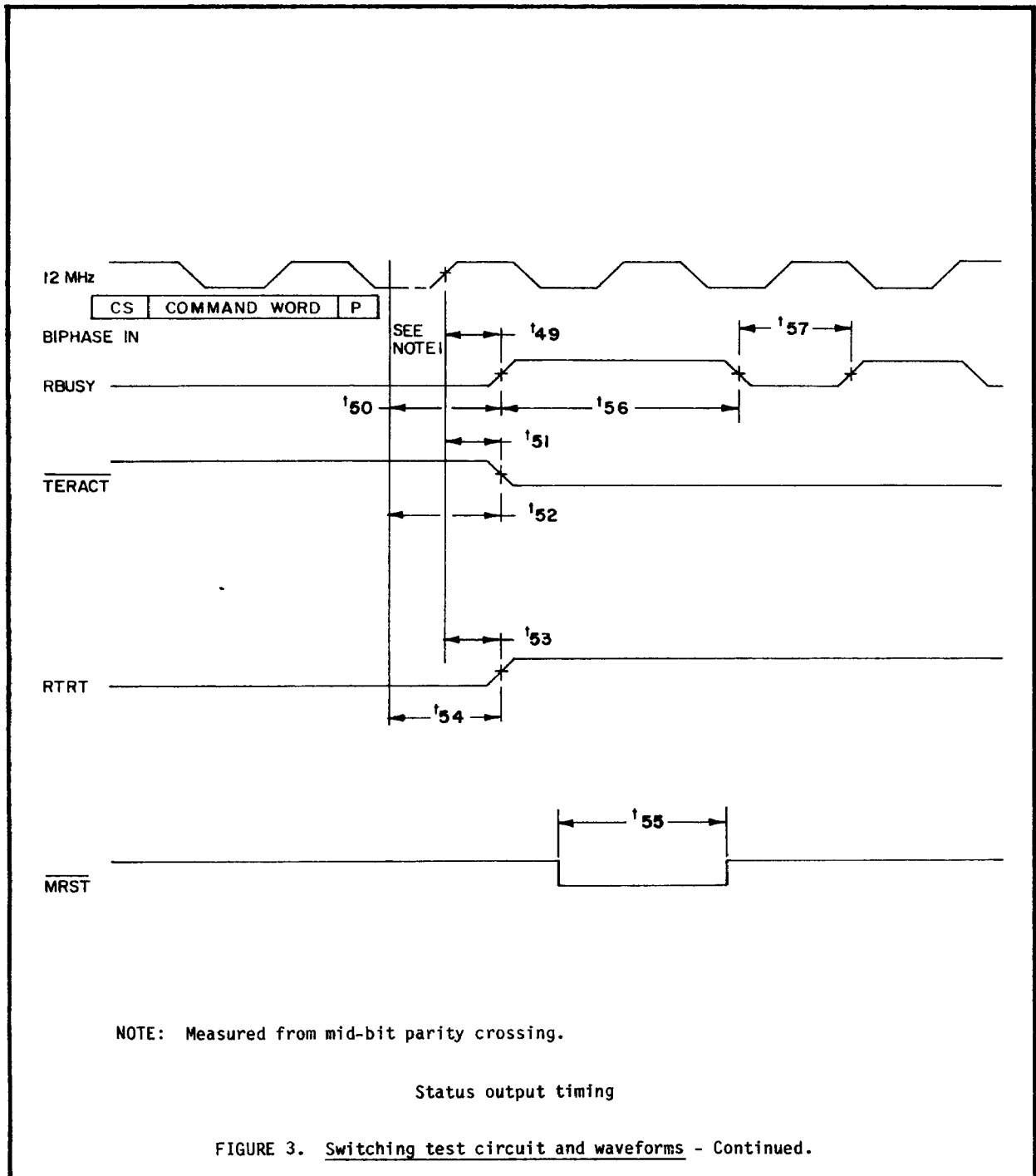
Status output timing

FIGURE 3. Switching test circuit and waveforms - Continued.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 17

DESC FORM 193A  
SEP 87

\* U. S. GOVERNMENT PRINTING OFFICE: 1988-550-547



<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 18

DESC FORM 193A  
SEP 87

U. S. GOVERNMENT PRINTING OFFICE: 1968-550-547

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 or table IV, method 5010 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 or method 5010 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 or table IV method 5010 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$ ,  $C_{IO}$ ) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 10 devices with zero rejects shall be required.
- d. Subgroups 7 and 8 shall consist of verifying the functionality of the device. It forms a part of the vendor/s test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 19

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I or 5010, table IV)
Interim electrical parameters (method 5004 or 5010)	---
Final electrical test parameters (method 5004 or 5010)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005 or 5010)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005 or 5010)	1, 2, 7, 8A

\* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-8526.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8526.

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		5962-89576
		REVISION LEVEL	SHEET 20

Name	Type	Active	Description
DATA(15)	TTB		Bit 15(MSB) of the bidirectional data bus
DATA(14)	TTB		Bit 14 of the bidirectional data bus
DATA(13)	TTB		Bit 13 of the bidirectional data bus
DATA(12)	TTB		Bit 12 of the bidirectional data bus
DATA(11)	TTB		Bit 11 of the bidirectional data bus
DATA(10)	TTB		Bit 10 of the bidirectional data bus
DATA(9)	TTB		Bit 9 of the bidirectional data bus
DATA(8)	TTB		Bit 8 of the bidirectional data bus
DATA(7)	TTB		Bit 7 of the bidirectional data bus
DATA(6)	TTB		Bit 6 of the bidirectional data bus
DATA(5)	TTB		Bit 5 of the bidirectional data bus
DATA(4)	TTB		Bit 4 of the bidirectional data bus
DATA(3)	TTB		Bit 3 of the bidirectional data bus
DATA(2)	TTB		Bit 2 of the bidirectional data bus
DATA(1)	TTB		Bit 1 of the bidirectional data bus
DATA(0)	TTB		Bit 0 (LSB) of the bidirectional data bus
ADDR(9)	TI		Bit 9 (MSB) of the address bus
ADDR(8)	TI		Bit 8 of the address bus
ADDR(7)	TI		Bit 7 of the address bus
ADDR(6)	TI		Bit 6 of the address bus
ADDR(5)	TI		Bit 5 of the address bus
ADDR(4)	TI		Bit 4 of the address bus
ADDR(3)	TI		Bit 3 of the address bus
ADDR(2)	TI		Bit 2 of the address bus
ADDR(1)	TI		Bit 1 of the address bus
ADDR(0)	TI		Bit 0 (LSB) of the address bus
CS	TI	AL	Chip select
RD/W $\overline{R}$	TI		Read/write
CTRL	TI	AL	Control
OE	TI	AL	Output enable
BRDCST 1*	TO	AL	Broadcast
T/R 0*	TO		Transmit/receive
RTRT 0*	TO	AH	Remote terminal to remote terminal
VALMSG 0*	TO	AH	Valid message
RBUSY 0*	TO	AH	RTR busy
ILLCOM	TDI	AH	Illegal command
MERR 0*	TO	AH	Message error
TXERR 0*	TO	AH	Transmission error
TIMERON 1*	TO	AL	Fail-safe timer
COMSTR 1*	TO	AL	Command strobe
TERACT 1*	TO	AL	Terminal active
MC/SA 0*	TO		Mode code/subaddress indicator
MCSA0 0*	TO		Mode code/subaddress output 0
MCSA1 0*	TO		Mode code/subaddress output 1
MCSA2 0*	TO		Mode code/subaddress output 2
MCSA3 0*	TO		Mode code/subaddress output 3
MCSA4 0*	TO		Mode code/subaddress output 4

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 21

6.6 Pin descriptions - continued			
Name	Type	Active	Description
RTA4	TUI		Remote terminal address bit 4 (MSB)
RTA3	TUI		Remote terminal address bit 3
RTA2	TUI		Remote terminal address bit 2
RTA1	TUI		Remote terminal address bit 1
RTA0	TUI		Remote terminal address bit 0 (LSB)
RTPTY	TUI		Remote terminal address parity
RAZ	TI		Receiver-channel A, zero input
RAO	TI		Receiver-channel A, one input
RBZ	TI		Receiver-channel B, zero input
RBO	TI		Receiver-channel B, one input
TAZ 0*	TO		Transmitter-channel A, zero output
TAO 0*	TO		Transmitter-channel A, one output
TBZ 0*	TO		Transmitter-channel B, zero output
TBO 0*	TO		Transmitter-channel B, one output
MRST	TUI	AL	Master reset
12MHz	TI		12 MHz input clock
2MHz	TO		2 MHz output clock
VDD	PWR		+5 V dc power
	PWR		+5 V dc power
VSS	GND		Reference ground
	GND		Reference ground

NOTES:  
 TI = TTL Input  
 TUI = TTL Input (pull-up)  
 TDI = TTL Input (pull-down)  
 TO = TTL Output  
 TTO = Three-state TTL Output  
 TTB = Three-state TTL Bidirectional  
 AH = Active high  
 AL = Active low  
 \* = Values marked with asterisks indicate the initialized values of these bits.

<b>STANDARDIZED                  MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
	REVISION LEVEL	SHEET 22

查询"5962-8957601XX"供应商

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number <u>1/</u>
5962-8957601XX	65342	UT1553B RTR G
5962-8957601YX	65342	UT1553B RTR W
5962-8957601ZX	65342	UT1553B RTR A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

65342

Vendor name and address

United Technologies Microelectronics Center  
1575 Garden of the Gods  
Colorado Springs, Colorado 80907

<b>STANDARDIZED MILITARY DRAWING</b> DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>	5962-89576
		REVISION LEVEL SHEET 23

DESC FORM 193A  
SEP 87

★ U. S. GOVERNMENT PRINTING OFFICE: 1988-549-904