

16-bit bus transceiver with direction pin; 30Ω series termination resistors; 5V Input/Outputs tolerant (3-State)

74LVC162245A/
74LVCH162245A

FEATURES

- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74LVCH162245A only)
- Integrated 30Ω termination resistors

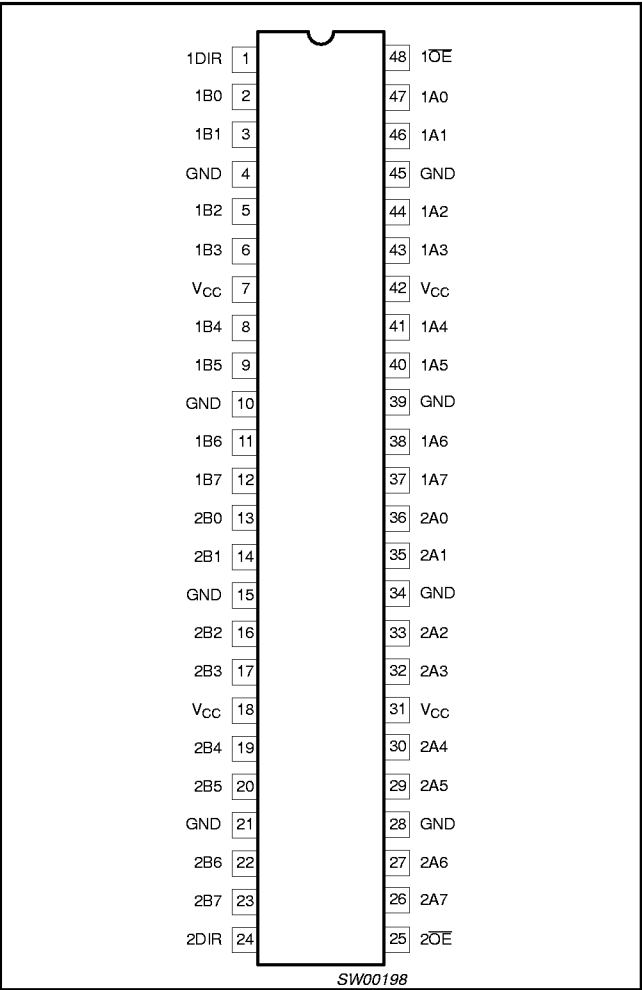
DESCRIPTION

The 74LVC(H)162245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC(H)162245A is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LVC(H)162245A features two output enable ($\overline{nOE}$) inputs for easy cascading and two send/receive ($\overline{nDIR}$) inputs for direction control. $\overline{nOE}$ controls the outputs so that the buses are effectively isolated. The 74LVC(H)162245A is design with 30Ω series termination resistors in both HIGH and LOW output stages to reduce line noise. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74LVCH162245A bus hold data inputs eliminates the need for extreme pull up resistors to hold unused inputs.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVC162245A DL	VC162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVC162245A DGG	VC162245A DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74LVCH162245A DL	VCH162245A DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74LVCH162245A DGG	VCH162245A DGG	SOT362-1

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; t_r = t_f ≤ 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay An to Bn; Bn to An	C _L = 50pF V _{CC} = 3.3V	3.3	ns
C _I	Input capacitance		5.0	pF
C _{I/O}	Input/output capacitance		10	pF
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
P_D = C_{PD} × V_{CC}² × f_i + ∑ (C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz; C_L = output load capacity in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
∑ (C_L × V_{CC}² × f_o) = sum of the outputs.

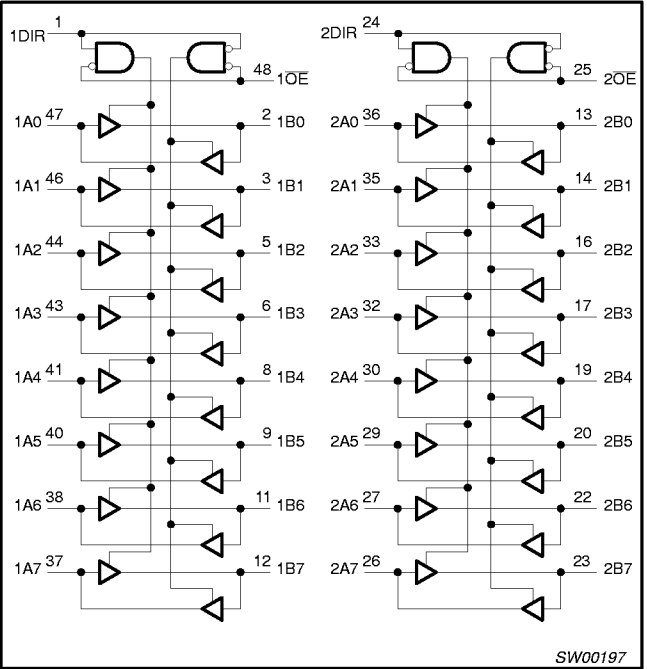
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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1DIR	Direction control
2, 3, 5, 6, 8, 9, 11, 12	1B0 to 1B7	Data inputs/outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage
13, 14, 16, 17, 19, 20, 22, 23	2B0 to 2B7	Data inputs/outputs
24	2DIR	Direction control
25	2OE	Output enable input (active LOW)
36, 35, 33, 32, 30, 29, 27, 26	2A0 to 2A7	Data inputs/outputs
47, 46, 44, 43, 41, 40, 38, 37	1A0 to 1A7	Data inputs/outputs
48	1OE	Output enable input (active LOW)

LOGIC SYMBOL

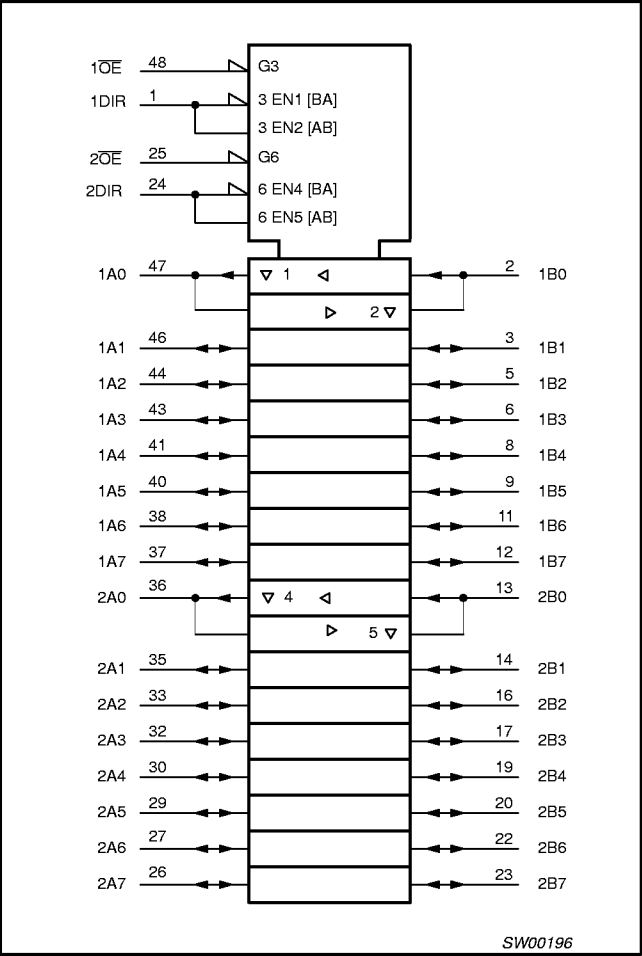


FUNCTION TABLE

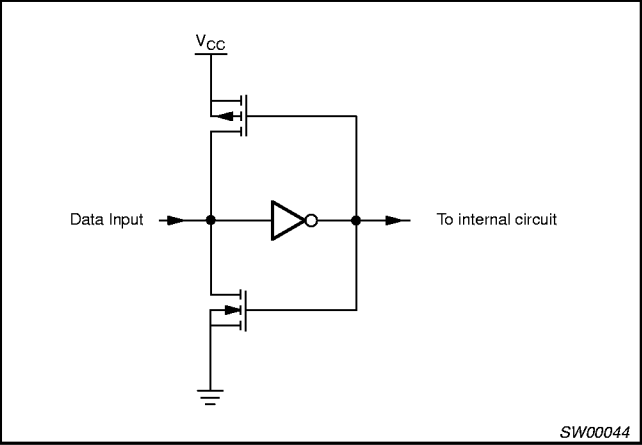
INPUTS		INPUTS/OUTPUT	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUSHOLD CIRCUIT



16-bit bus transceiver with direction pin; 30Ω series
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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range		0	5.5	V
V_O	DC output voltage range; output HIGH or LOW state		0	V_{CC}	V
V_O	DC output voltage range; output 3-State		0	5.5	V
T_{amb}	Operating ambient temperature range in free air		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.2$ to 2.7 V $V_{CC} = 2.7$ to 3.6 V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	$V_I < 0$	—	-50	mA
V_I	DC input voltage	Note 2	-0.5	+6.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	—	± 50	mA
V_O	DC output voltage; output HIGH or LOW state	Note 2	-0.5	$V_{CC} + 0.5$	V
V_O	DC output voltage; output 3-State	Note 2	-0.5	6.5	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	—	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		—	± 100	mA
T_{stg}	Storage temperature range		-65	+150	°C
P_{tot}	Power dissipation per package — SSOP and TSSOP package	Above +60°C derate linearly 5.5mW/K		500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V	
		V _{CC} = 2.7 to 3.6V	2.0				
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V	
		V _{CC} = 2.7 to 3.6V			0.8		
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} - 0.5			V	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} - 0.2	V _{CC}			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.8				
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 6mA			0.40	V	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100μA			0.20		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.55		
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND ⁶			± 0.1	± 5	μA
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	V _{CC} = 3.6V; V _I = 5.5V or GND	Output disabled		± 0.1	± 10	μA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND ⁶			0.1	± 10	μA
I _{off}	Power off leakage supply	V _{CC} = 0.0V; V _I or V _O = 5.5V			0.1	± 10	μA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			0.1	40	μA
ΔI _{CC}	Additional quiescent supply current per control pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0			5	500	μA
ΔI _{CC}	Additional quiescent supply current per data input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0			150	750	μA
I _{BHL}	Bus hold LOW sustaining current	V _{CC} = 3.0V; V _I = 0.8V ^{2, 3, 4}		75			μA
I _{BHH}	Bus hold HIGH sustaining current	V _{CC} = 3.0V; V _I = 2.0V ^{2, 3, 4}		-75			μA
I _{BHLO}	Bus hold LOW overdrive current	V _{CC} = 3.6V ^{2, 3, 5}		450			μA
I _{BHHO}	Bus hold HIGH overdrive current	V _{CC} = 3.6V ^{2, 3, 5}		-450			μA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts (LVCH16-A) only.
3. For data inputs only, control inputs do not have a bus hold circuit.
4. The specified sustaining current at the data input holds the input below the specified V_I level.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.
6. For bus hold parts, the bus hold circuit is switched off when V_I exceeds V_{CC} allowing 5.5V on the input terminal.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			V _{CC} = 3.3V ±0.3V			V _{CC} = 2.7V		
			MIN	TYP ¹	MAX	MIN	MAX	
t _{PHL} t _{PLH}	Propagation delay nAn to nBn; nBn to nAn	1	1.5	3.3	6.3	1.5	7.3	ns
t _{PZH} t _{PZL}	3-State output enable time n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn	2, 3	1.5	4.3	8.3	1.5	9.3	ns
t _{PHZ} t _{PLZ}	3-State output disable time n $\overline{\text{OE}}$ to nAn; n $\overline{\text{OE}}$ to nBn	2, 3	1.5	4.0	6.5	1.5	7.5	ns

NOTE:

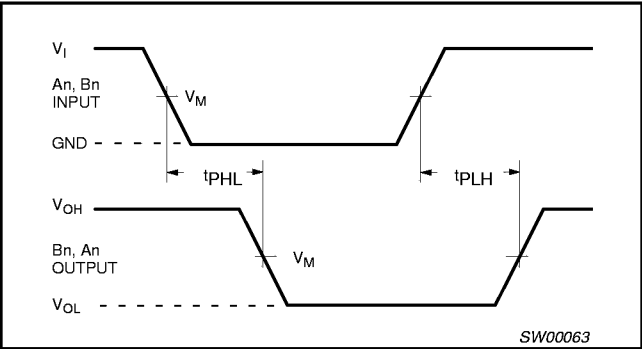
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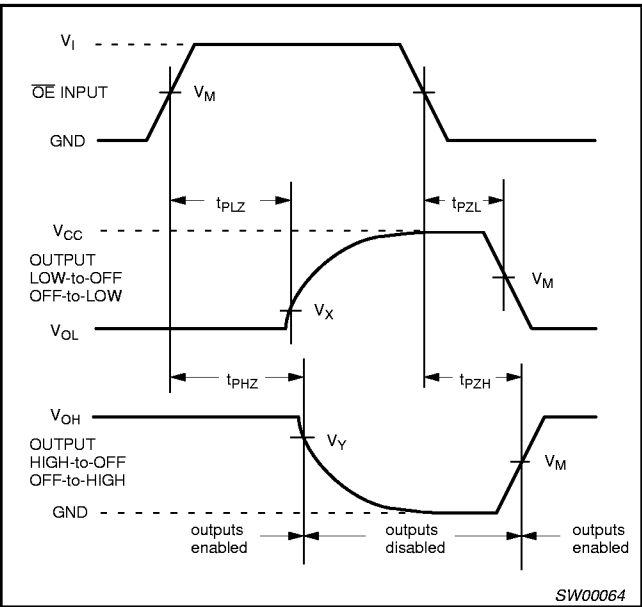
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AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$

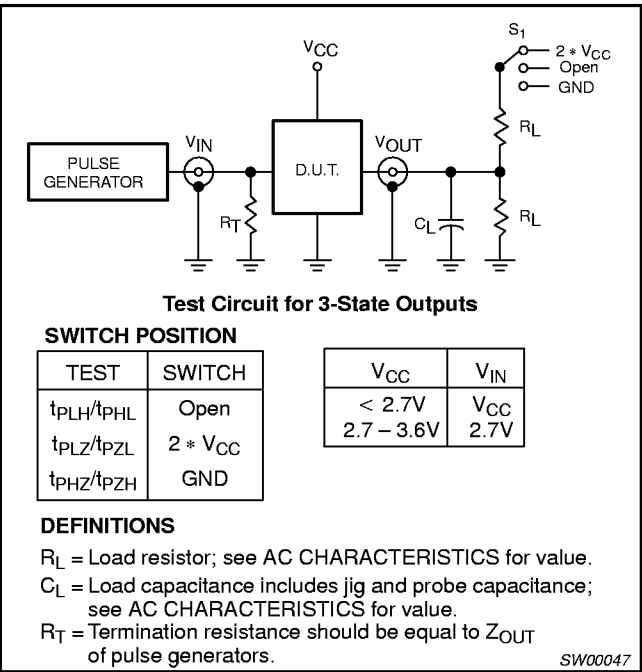


Waveform 1. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT



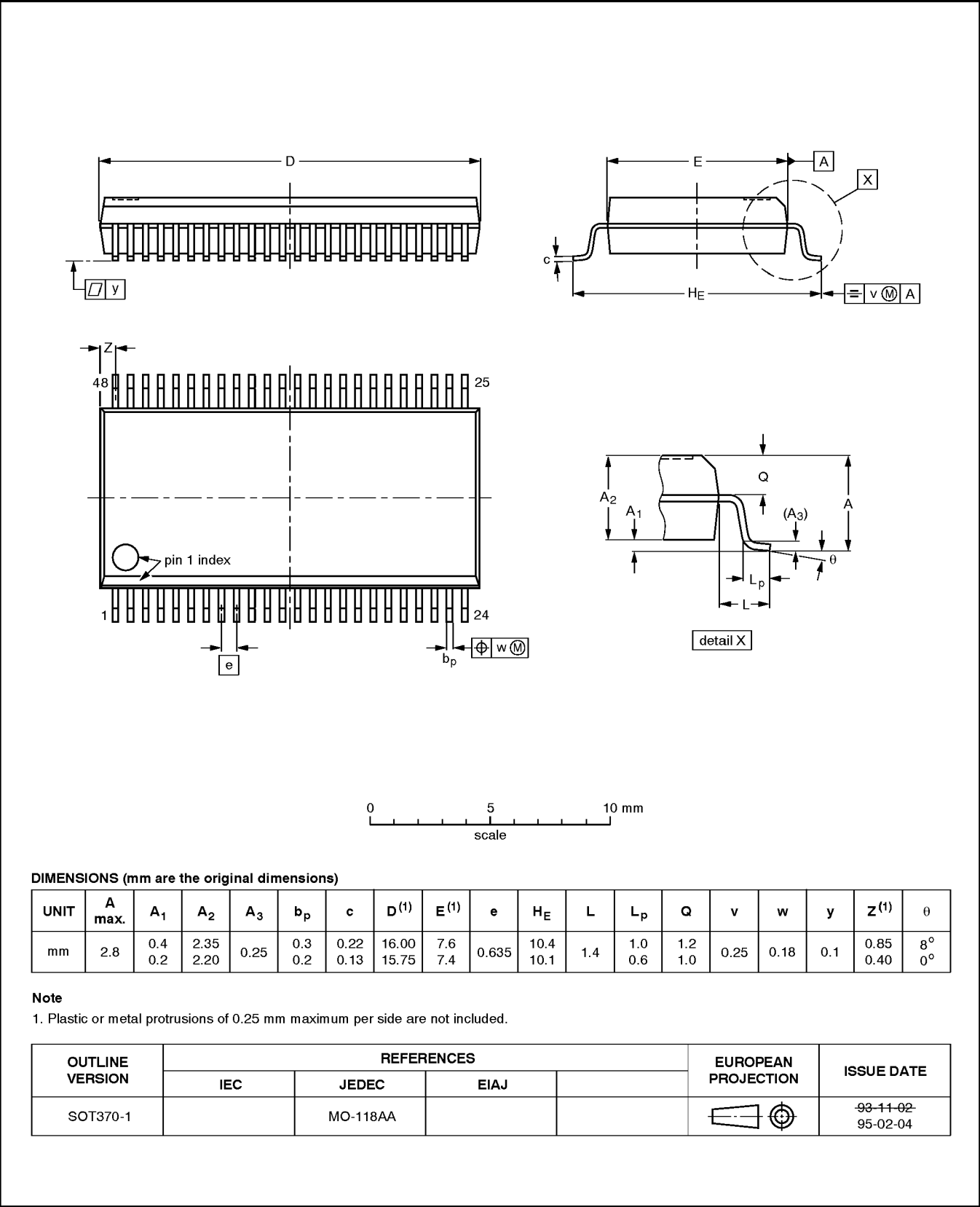
Waveform 3. Load circuitry for switching times

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

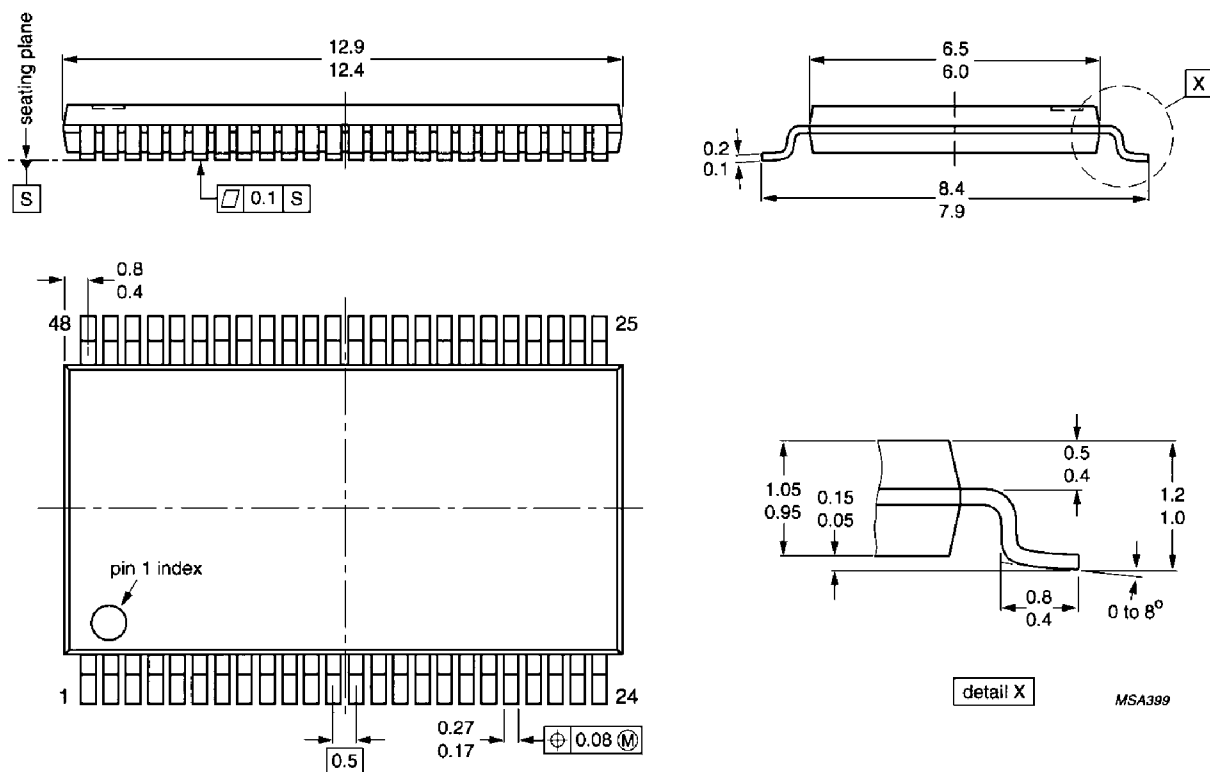


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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



Dimensions in mm.