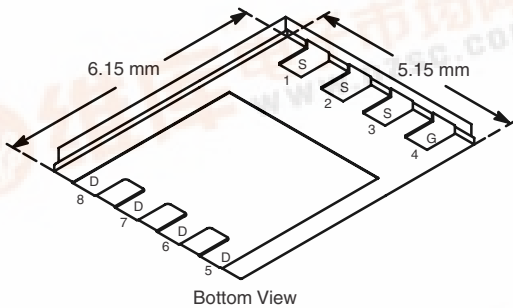


P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
- 30	0.0052 at V _{GS} = - 10 V	- 50 ^d	51 nC
	0.0094 at V _{GS} = - 4.5 V	- 50 ^d	

PowerPAK SO-8



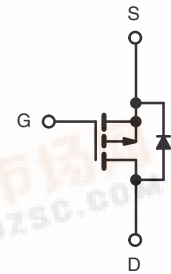
FEATURES

- Halogen-free
- TrenchFET[®] Power MOSFET
- 100% R_g Tested
- 100% UIS Tested

RoHS
COMPLIANT

APPLICATIONS

- Battery and Load Switching
- Notebook Computers
- Notebook Battery Packs



Ordering Information: Si7149DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 30	V	
Gate-Source Voltage	V _{GS}	± 25		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 50 ^d	
		T _C = 70 °C	- 50 ^d	
		T _A = 25 °C	- 23.7 ^{a, b}	
		T _A = 70 °C	- 18.7 ^{a, b}	
Pulsed Drain Current	I _{DM}	- 70	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		- 50 ^d
		T _A = 25 °C		- 4.3 ^{a, b}
Avalanche Current	I _{AS}	- 20	mJ	
Single-Pulse Avalanche Energy	E _{AS}	20		
Maximum Power Dissipation	P _D	T _C = 25 °C	69	
		T _C = 70 °C	44.4	
		T _A = 25 °C	5.2 ^{a, b}	
		T _A = 70 °C	3.3 ^{a, b}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	19	24	°C/W
Maximum Junction-to-Case	R _{thJC}	1.2	1.8	

Notes:

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 65 °C/W.
- Package limited.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	- 30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\ \mu\text{A}$		- 32		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			6.0		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	- 1.2		- 2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			- 1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			- 5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	- 30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -15\text{ A}$		0.0042	0.0052	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		0.0075	0.0094	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}, I_D = -15\text{ A}$		47		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4590		pF
Output Capacitance	C_{oss}			795		
Reverse Transfer Capacitance	C_{rss}			765		
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -10\text{ A}$		98	147	nC
				51	77	
Gate-Source Charge	Q_{gs}	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$		11.7		
Gate-Drain Charge	Q_{gd}			25		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.4	2.0	4.0	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\ \Omega$		15	30	ns
Rise Time	t_r			14	28	
Turn-Off Delay Time	$t_{d(off)}$			58	110	
Fall Time	t_f			16	32	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\ \Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\ \Omega$		79	140	
Rise Time	t_r			135	220	
Turn-Off Delay Time	$t_{d(off)}$			52	100	
Fall Time	t_f			36	70	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			- 50	A
Pulse Diode Forward Current	I_{SM}				- 70	
Body Diode Voltage	V_{SD}	$I_S = -3\text{ A}, V_{GS} = 0\text{ V}$		- 0.72	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		49	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			47	86	nC
Reverse Recovery Fall Time	t_a			22		ns
Reverse Recovery Rise Time	t_b			27		

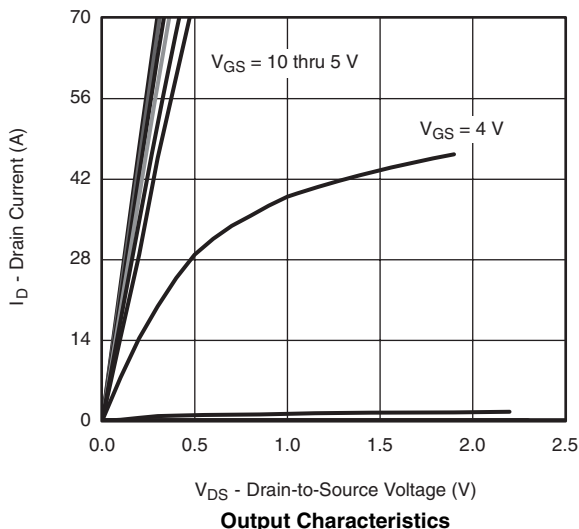
Notes:

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

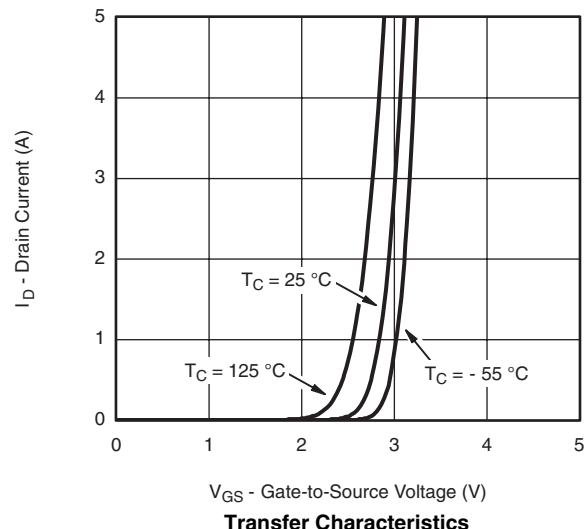
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



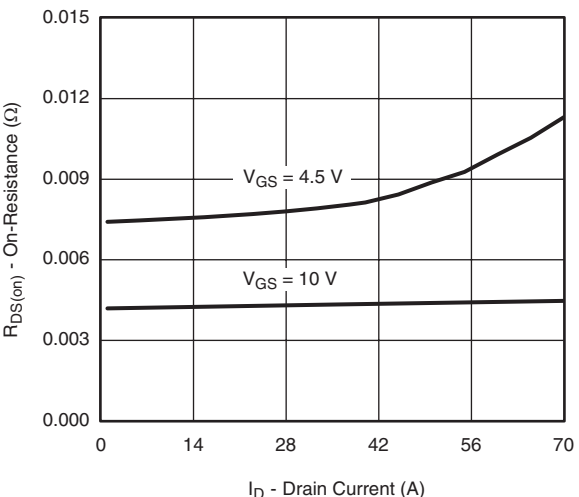
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



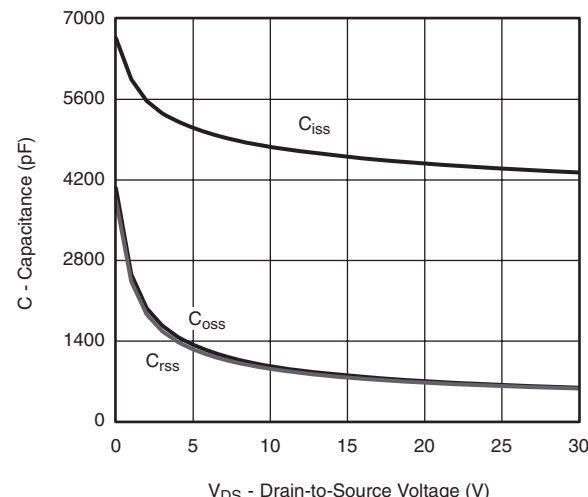
Output Characteristics



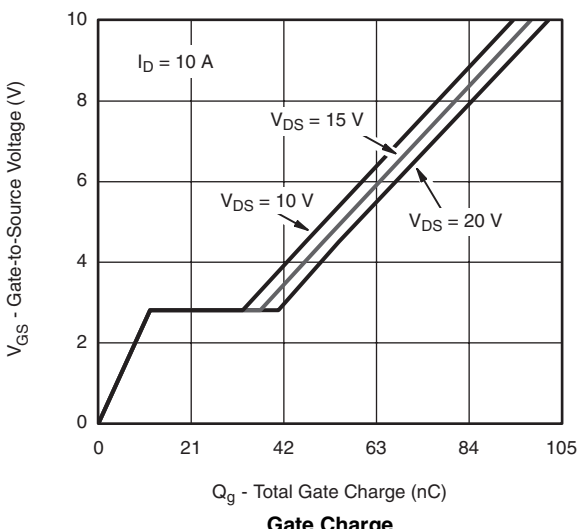
Transfer Characteristics



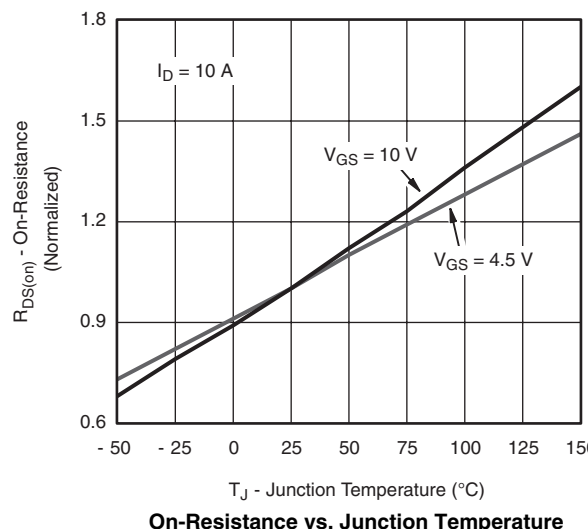
On-Resistance vs. Drain Current



Capacitance



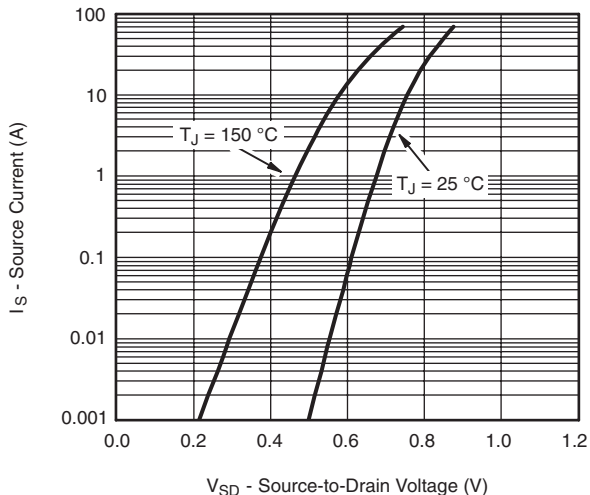
Gate Charge



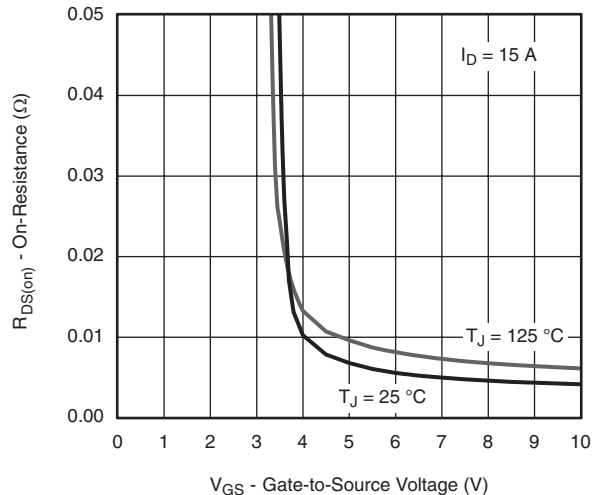
On-Resistance vs. Junction Temperature



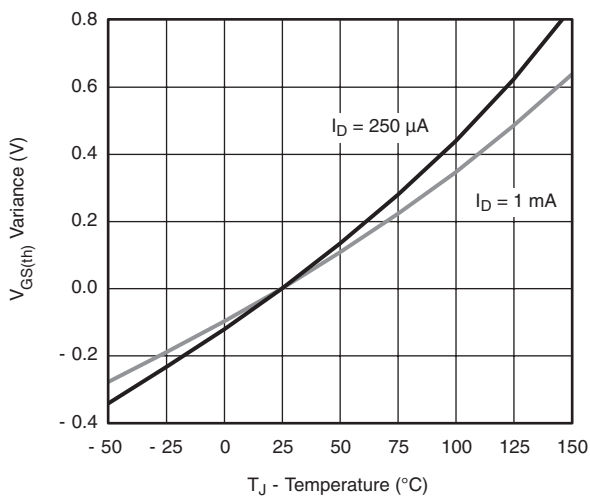
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



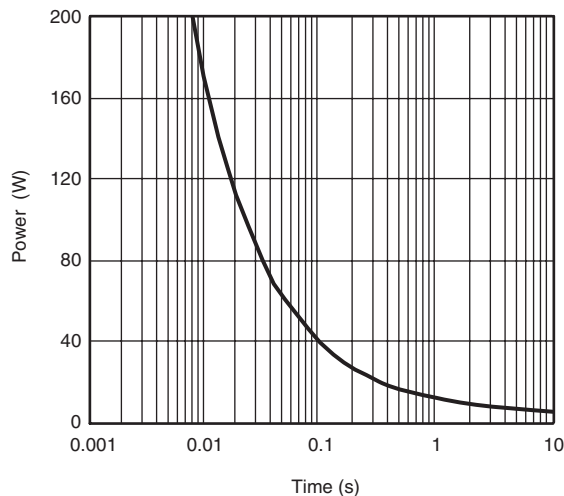
Source-Drain Diode Forward Voltage



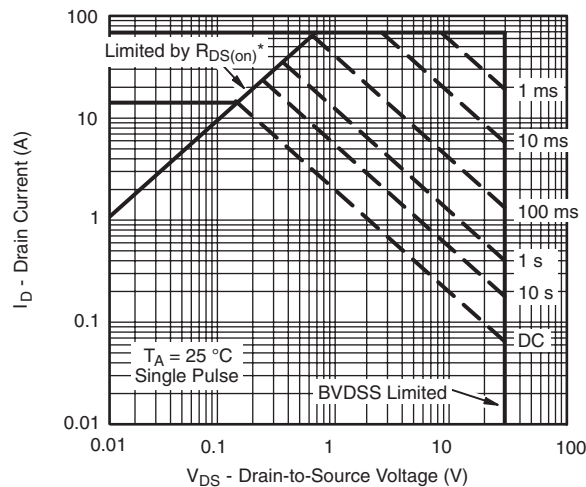
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

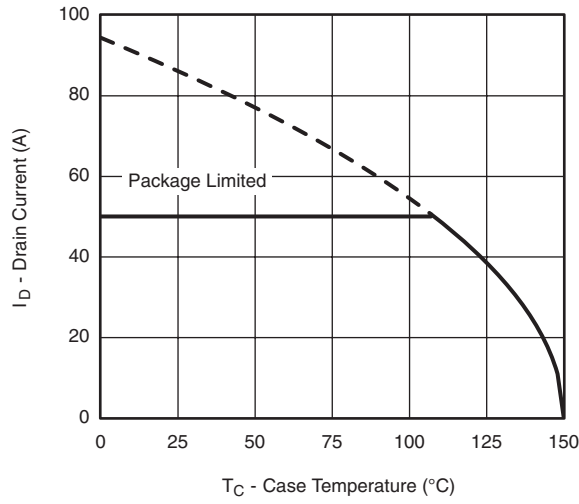


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

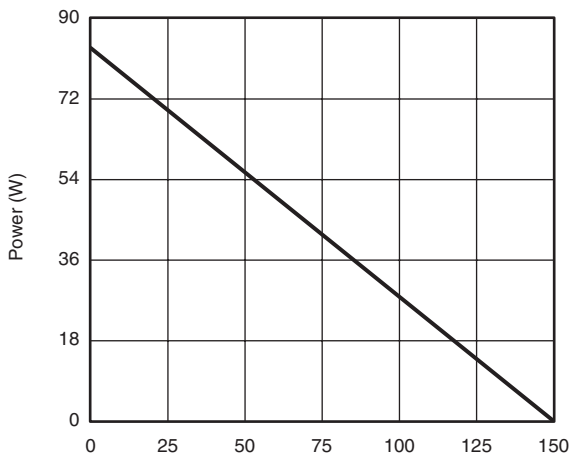
Safe Operating Area



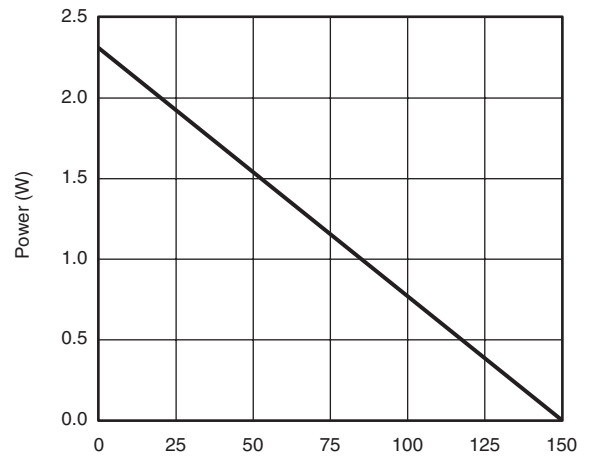
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



Power, Junction-to-Case

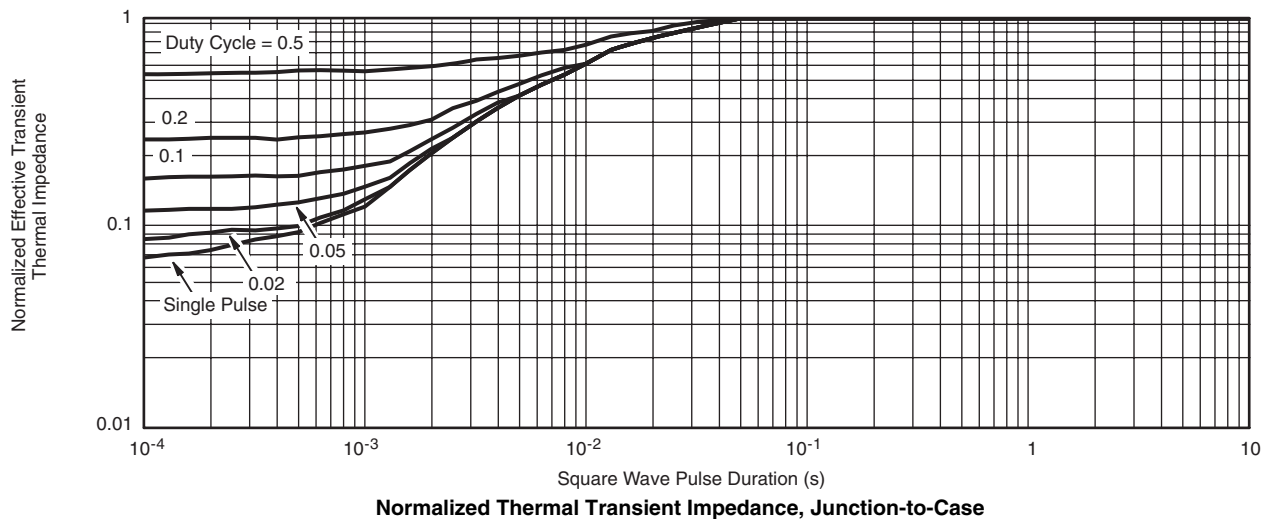
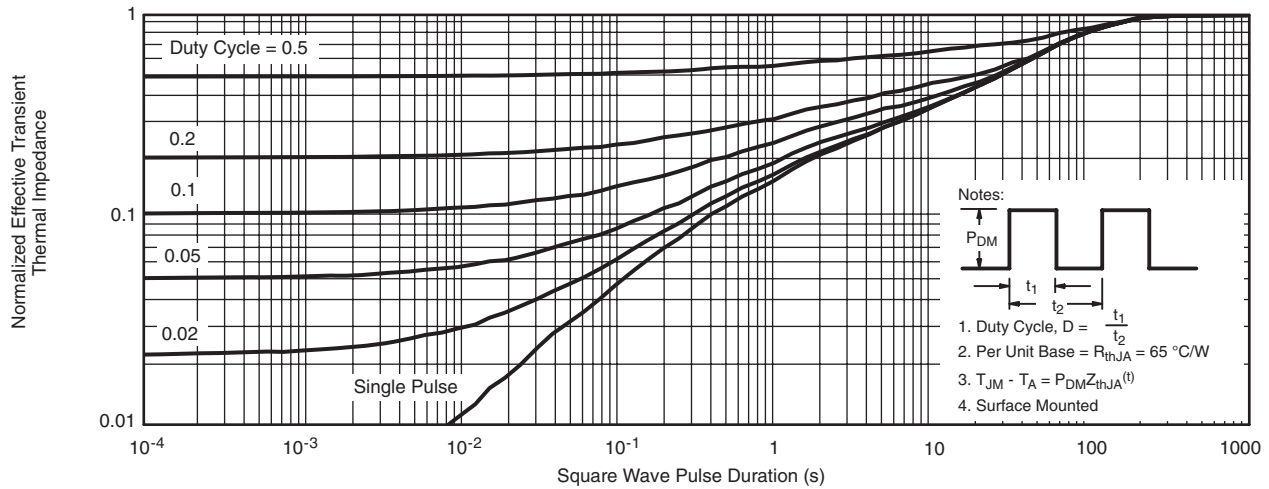


Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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