NCP1595, NCP1595A

Current Mode PWM Converter for Low Voltage Outputs

The NCP1595/NCP1595A is a current mode PWM buck converter with integrated power switch and synchronous rectifier. It can provide up to 1.5 A output current with high conversion efficiency. High frequency PWM control scheme can provide a low output ripple noise. Thus, it allows the usage of small size passive components to reduce the board space. In a low load condition, the controller will automatically change to PFM mode for provides a higher efficiency at low load. Additionally, the device includes soft−start, thermal shutdown with hysteresis, cycle−by−cycle current limit, and short circuit protection. This device is available in compact 3x3 DFN package.

Features

- High Efficiency 95% @ 3.375 V
- Synchronous Rectification for Higher Efficiency in PWM Mode
- Integrated MOSFET
- Fully Internal Compensation
- High Switching Frequency, 1.0 MHz
- Low Output Ripple
- Cycle−by−cycle Current Limit
- Current Mode Control
- Short Circuit Protection
- Built−in Slope Compensation for Current Mode PWM Converter
- ±1.5% Reference Voltage
- Thermal Shutdown with Hysteresis
- Ext. Adjustable Output Voltage
- Fast Transient Response
- Low Profile and Minimum External Components
- Designed for Use with Ceramic Capacitor
- Compact 3x3 DFN Package
- These are Pb−Free Devices

Typical Applications

- Hard Disk Drives
- USB Power Device
- Wireless and DSL Modems

ON Semiconductor®

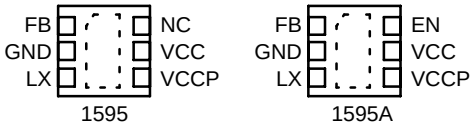
http://onsemi.com

DFN6 3*3 MM, 0.95 PITCH
CASE 506AH

MARKING DIAGRAMS

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

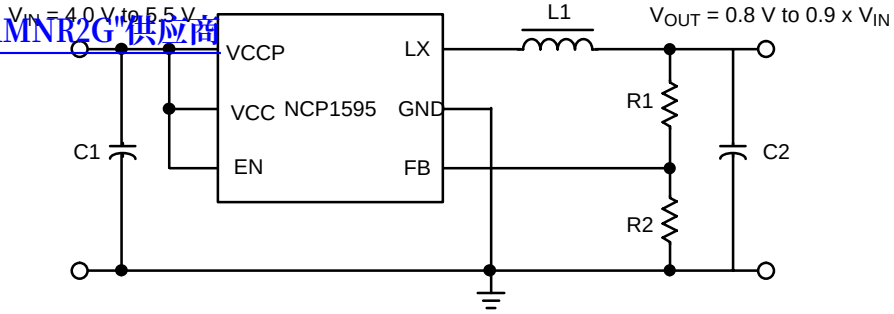


Figure 1. Typical Operating Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pin 4, 5)	V_{IN}	7.0 −0.3 (DC) −1.0 (100 ns)	V
Input / Output Pins Pin 1,3,6	V_{IO}	6.5, −0.3 (DC) −1.0 (100 ns)	V
Thermal Characteristics 3x3 DFN Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 1450 68.5	 mW °C/W
Operating Junction Temperature Range (Note 4)	T_J	−40 to + 150	°C
Operating Ambient Temperature Range	T_A	−40 to + 85	°C
Storage Temperature Range	T_{stg}	− 55 to +150	°C
Moisture Sensitivity Level (Note 3)		1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: ESD data available upon request.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) 2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) 200 V per JEDEC standard: JESD22−A115.
2. Latchup Current Maximum Rating: 150 mA per JEDEC standard: JESD78.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
4. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS
(V_{IN} = 5.0 V, V_{OUT} = 1.2 V, T_A = 25°C for typical value, −40°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	4.0	−	5.5	V
Under Voltage Lockout Threshold	V_{UVLO}	3.2	3.5	3.8	V
Under Voltage Lockout hysteresis	V_{UVLO_HYS}		180		mV
P FET Leakage Current (Pin 5, 4) T_A = 25°C T_A = −40°C to 85°C	I_{LEAK-P}		1.0	 10 15	μA
N FET Leakage Current (Pin 3, 2) T_A = 25°C T_A = −40°C to 85°C	I_{LEAK-N}		1.0	 10 15	μA
FEEDBACK VOLTAGE					
FB Input Threshold (T_A = −40°C to 85°C)	V_{FB}	0.788	0.800	0.812	V
FB Input Current	I_{FB}		10	100	nA
Overvoltage Protect Higher than FB Threshold (T_A = 25°C)	V_{OVP}	2.0	5.0	10.0	%
THERMAL SHUTDOWN					
Thermal Shutdown Threshold (Note 5)	T_{SHDN}	TBD	160	−	°C
Hysteresis	T_{SDHYS}		30		°C
PWM SMPS MODE					
Minimum ON−Time	TON_{MIN}		100		ns
Switching Frequency (T_A = −40°C to 85°C)	F_{OSC}	0.8	1.0	1.2	MHz
Internal PFET ON−Resistance (I_{LX} = 100 mA, V_{IN} = 5.0 V, T_A = 25°C) (Note 5)	$R_{DS(ON)\_P}$	−	0.2	0.3	Ω
Internal NFET ON−Resistance (I_{LX} = 100 mA, V_{IN} = 5.0 V, T_A = 25°C) (Note 5)	$R_{DS(ON)\_N}$	−	0.15	0.22	Ω
Maximum Duty Cycle	D_{MAX}	−	−	100	%
Soft−Start Time (V_{IN} = 5.0 V, V_o = 1.2 V, I_{LOAD} = 0 mA, T_A = 25°C) (Note 6)	T_{SS}	−	1.0	−	ms
Main PFET Switch Current Limit (Note 5)	I_{LIM}	2.0	2.5		A
ENABLE (NCP1595A)					
Enable Threshold High (NCP1595A Only)	V_{EN_H}	1.8			V
Enable Threshold Low	V_{EN_L}			0.4	V
Enable bias current (EN = 0 V)	I_{EN}		500	TBD	nA
Total Device					
Quiescent Current Into V_{CCP} (V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CCP}		10		μA
Quiescent Current Into V_{CC} (V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CC}		900		μA
Shutdown Quiescent Current into V_{CC} and V_{CCP} (NCP1595A Only) (EN = 0, V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CC_SD}		1.5	3.0	μA

5. Values are design guarantee.
6. Design guarantee, value depends on voltage at V_{OUT}.

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
NCP1595		
1	FB	Feedback pin. Part is internally compensated. Only necessary to place a voltage divider or connect the output directly to this pin.
2	GND	Ground
3	LX	Pin connected internally to power switch. Connect externally to inductor.
4	VCCP	Power connection to the power switch.
5	VCC	IC power connection.
6	NC	No Connection
NCP1595A		
1	FB	Feedback pin. Part is internally compensated. Only necessary to place a voltage divider or connect the output directly to this pin.
2	GND	Ground
3	LX	Pin connected internally to power switch. Connect externally to inductor.
4	VCCP	Power connection to the power switch.
5	VCC	IC power connection.
6	EN	Device Enable pin. This pin has an internal current source pull up. No connect is enable the device. With this pin pulled down below 0.4 V, the device is disabled and enters the shutdown mode.

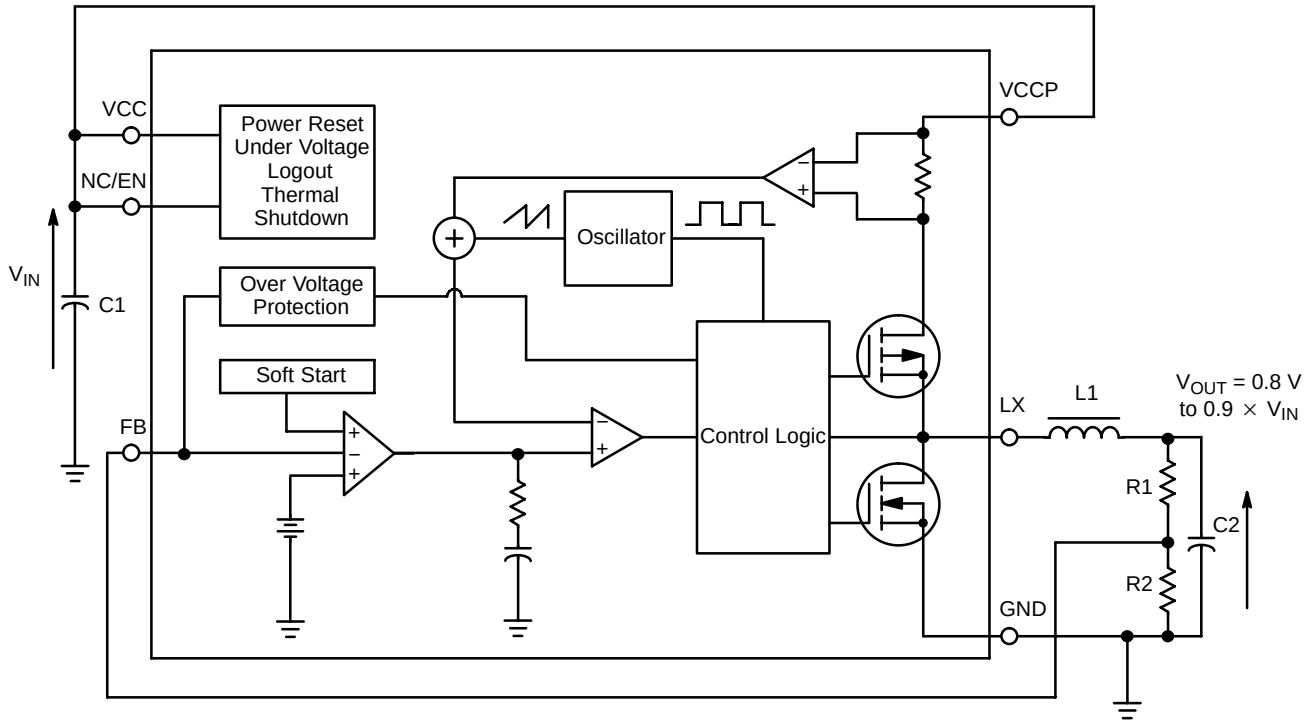


Figure 2. Detail Block Diagram

EXTERNAL COMPONENT REFERENCE DATA

Device	V_{OUT}	Inductor Model	Inductor (L1)	C_{IN} (C1)	C_{OUT} (C2)	R1	R2
NCP1595/ NCP1595A	3.3 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	22 μF 22 μF x 2	22 μF 22 μF x 2	31 k	10 k
NCP1595/ NCP1595A	2.5 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	22 μF 22 μF x 2	22 μF 22 μF x 2	21 k	10 k
NCP1595/ NCP1595A	1.5 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	22 μF 22 μF x 2	22 μF 22 μF x 2	8 k	10 k
NCP1595/ NCP1595A	1.2 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	22 μF 22 μF x 2	22 μF 22 μF x 2	5 k	10 k

TYPICAL OPERATING CHARACTERISTICS

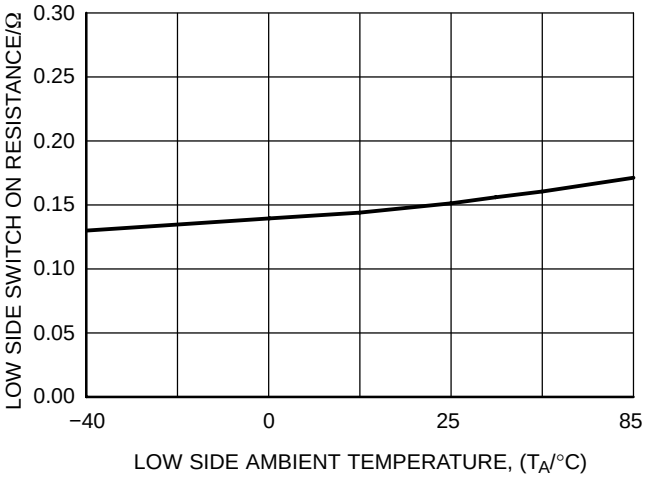


Figure 3. Switch ON Resistance vs. Temperature

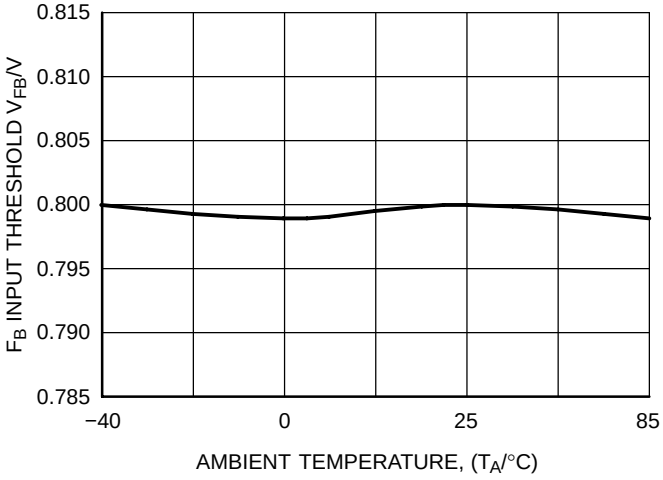


Figure 4. Feedback Input Threshold vs. Temperature

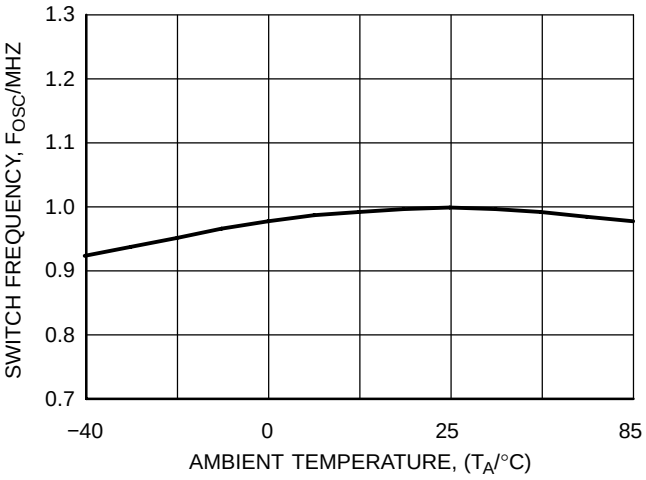


Figure 5. Switching Frequency vs. Temperature

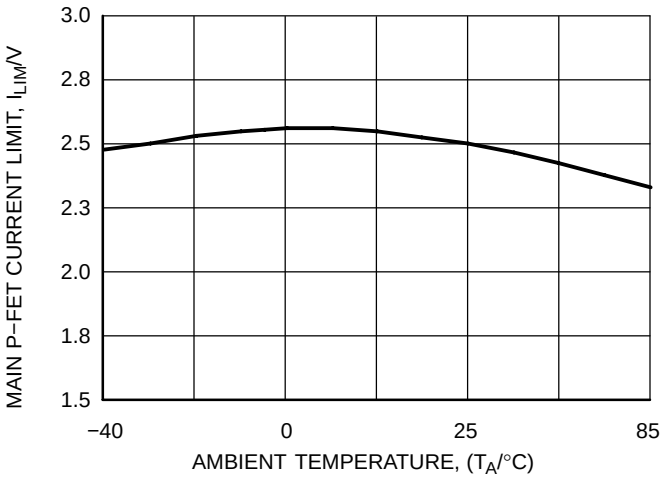


Figure 6. Main P−FET Current Limit vs. Temperature

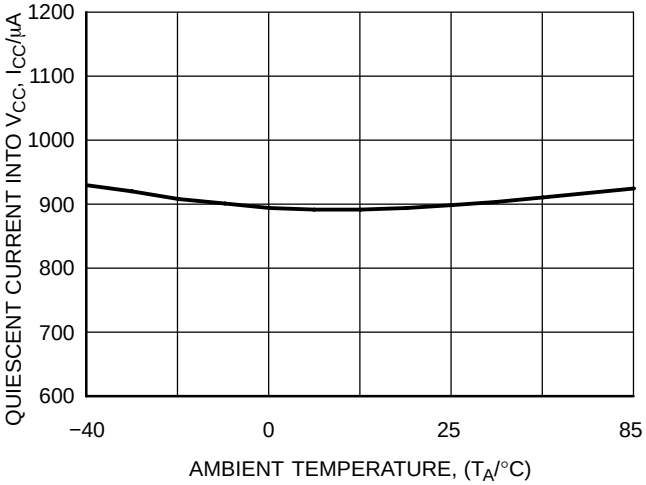


Figure 7. Quiescent Current Into V_{CC} vs. Temperature

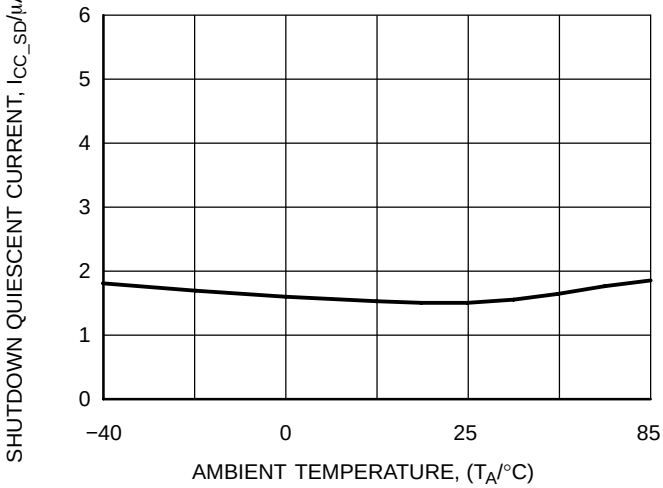


Figure 8. Shutdown Quiescent Current vs. Temperature

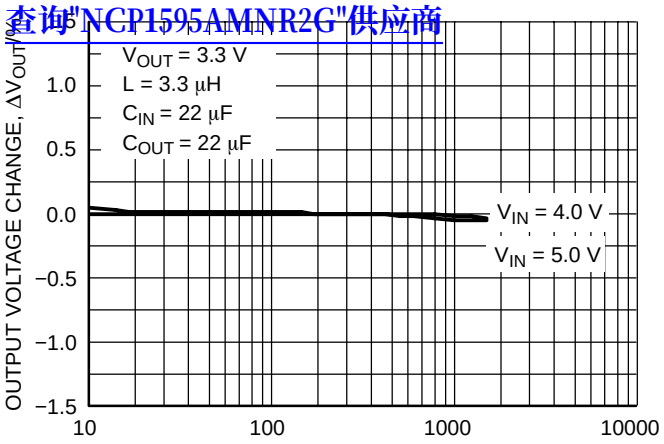


Figure 9. Output Voltage Change vs. Output Current

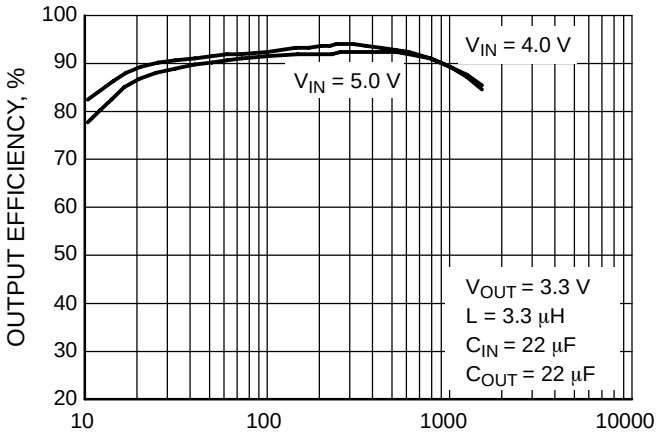


Figure 10. Efficiency vs. Output Current

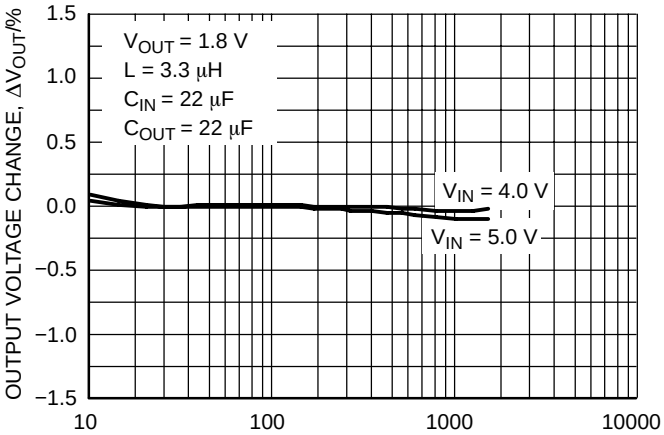


Figure 11. Output Voltage Change vs. Output Current

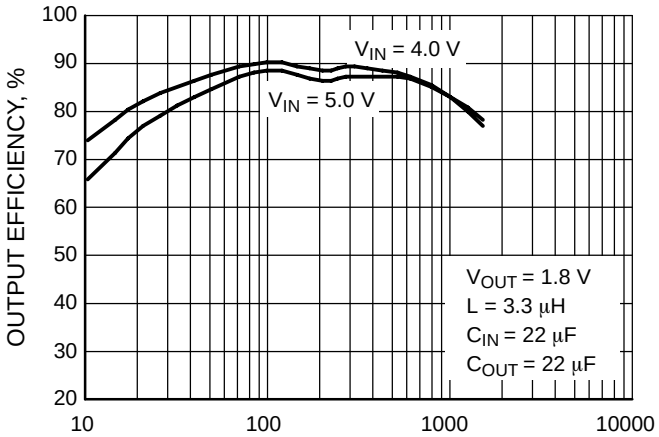


Figure 12. Efficiency vs. Output Current

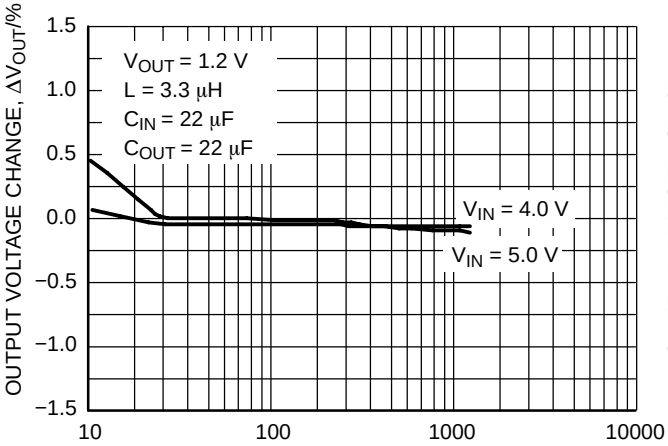


Figure 14. Output Voltage Change vs. Output Current

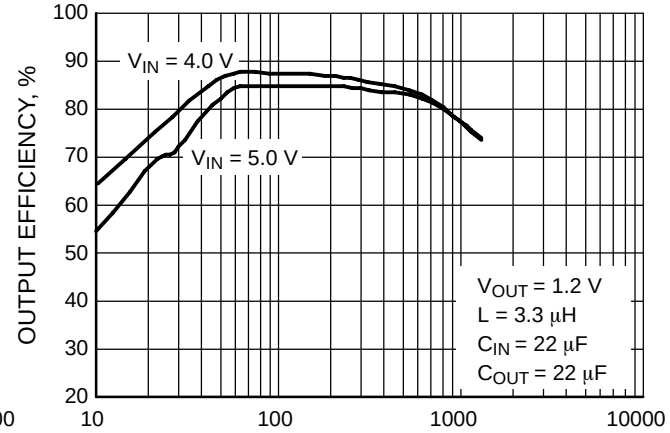
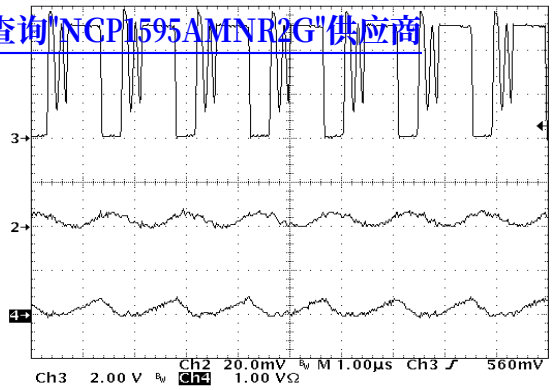
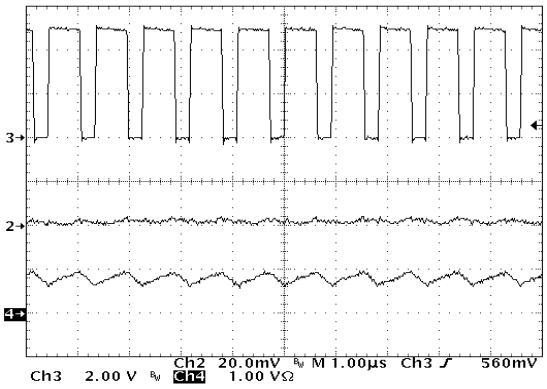


Figure 13. Efficiency vs. Output Current



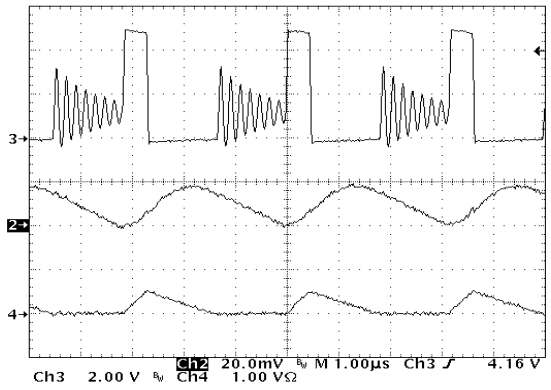
(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 3.3 µH, C_{OUT} = 20 µF)
Upper Trace: L_X Pin Switching Waveform, 2 V / div.
Middle Trace: Output Ripple Voltage, 20 mV / div.
Lower Trace: Inductor Current, 1 A / div.

Figure 15. DCM Switching Waveform for V_{OUT} = 3.3 V



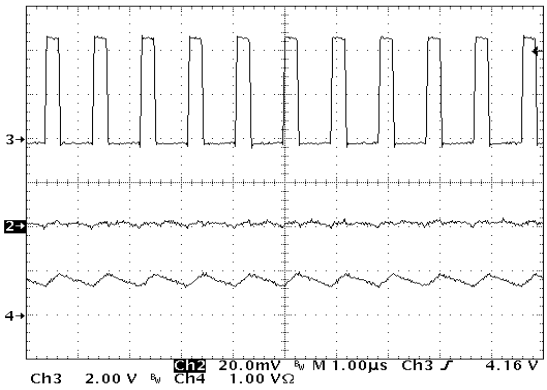
(V_{IN} = 5 V, I_{LOAD} = 700 mA, L = 3.3 µH, C_{OUT} = 20 µF)
Upper Trace: L_X Pin Switching Waveform, 2 V / div.
Middle Trace: Output Ripple Voltage, 20 mV / div.
Lower Trace: Inductor Current, 1 A / div.

Figure 16. CCM Switching Waveform for V_{OUT} = 3.3 V



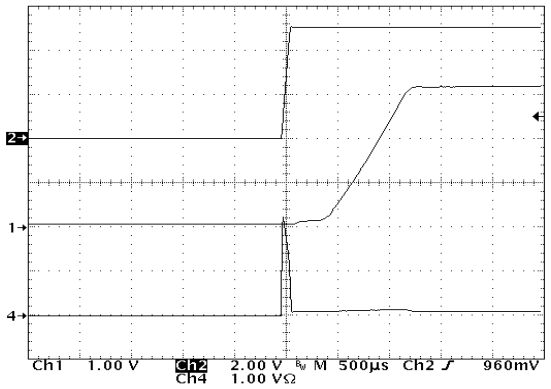
(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 3.3 µH, C_{OUT} = 20 µF)
Upper Trace: L_X Pin Switching Waveform, 2 V / div.
Middle Trace: Output Ripple Voltage, 20 mV / div.
Lower Trace: Inductor Current, 1 A / div.

Figure 17. DCM Switching Waveform for V_{OUT} = 1.2 V



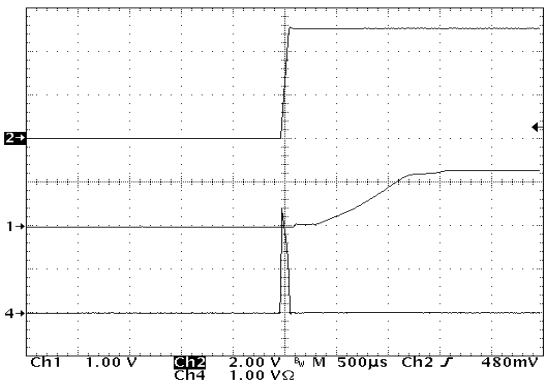
(V_{IN} = 5 V, I_{LOAD} = 700 mA, L = 3.3 µH, C_{OUT} = 20 µF)
Upper Trace: L_X Pin Switching Waveform, 2 V / div.
Middle Trace: Output Ripple Voltage, 20 mV / div.
Lower Trace: Inductor Current, 1 A / div.

Figure 18. CCM Switching Waveform for V_{OUT} = 1.2 V



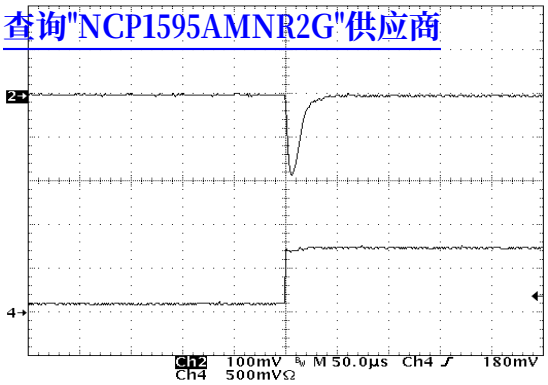
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 µH, C_{OUT} = 20 µF x 2)
Upper Trace: Input Voltage, 2 V/ div.
Middle Trace: Output Voltage, 1 V/ div.
Lower Trace: Input Current, 1 A / div.

Figure 19. Soft−Start Waveforms for V_{OUT} = 3.3 V



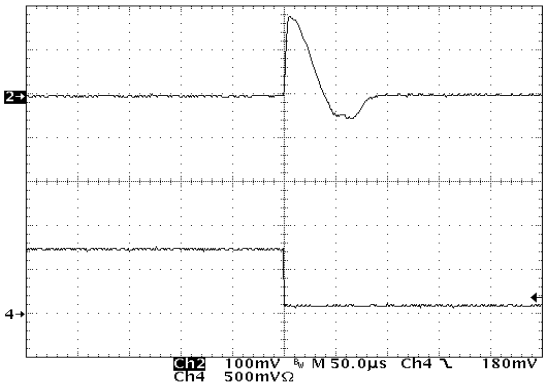
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 µH, C_{OUT} = 20 µF x 2)
Upper Trace: Input Voltage, 2 V/ div.
Middle Trace: Output Voltage, 1 V / div.
Lower Trace: Input Current, 1 A / div.

Figure 20. Soft−Start Waveforms for V_{OUT} = 1.2 V



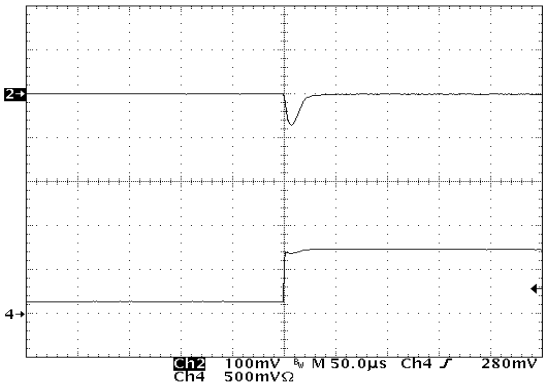
(V_{IN} = 5 V, L = 3.3 µH, C_{OUT} = 20 µF x 2)
Upper Trace: Output Dynamic Voltage, 100 mV / div.
Lower Trace: Output Current, 500 mA / div.

Figure 21. Load Regulation for V_{OUT} = 3.3 V



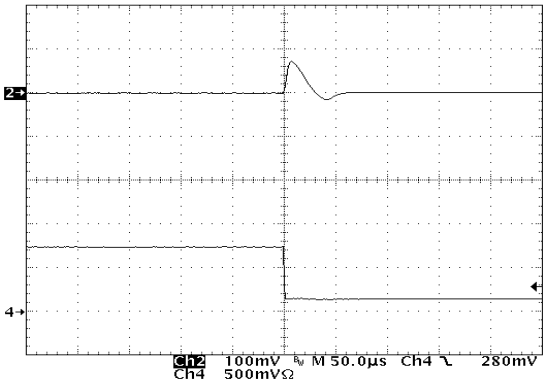
(V_{IN} = 5 V, L = 3.3 µH, C_{OUT} = 20 µF x 2)
Upper Trace: Output Dynamic Voltage, 100 mV / div.
Lower Trace: Output Current, 500 mA / div.

Figure 22. Load Regulation for V_{OUT} = 3.3 V



(V_{IN} = 5 V, L = 3.3 H, C_{OUT} = 20 µF x 2)
Upper Trace: Output Dynamic Voltage, 100 mV / div.
Lower Trace: Output Current, 500 mA / div.

Figure 23. Load Regulation for V_{OUT} = 1.2 V



(V_{IN} = 5 V, L = 3.3 H, C_{OUT} = 20 µF x 2)
Upper Trace: Output Dynamic Voltage, 100 mV / div.
Lower Trace: Output Current, 500 mA / div.

Figure 24. Load Regulation for V_{OUT} = 1.2 V

DETAILED OPERATING DESCRIPTION

Introduction

NCP1595 operates as a current mode buck converter with switching frequency at 1.0 MHz. The P−Channel main switch is set by the positive edge of the clock cycle going into the PWM latch. The main switch is reset by the PWM latch in the following three cases:

1. PWM comparator output trips as the peak inductor current signal reaches a threshold level established by the error amplifier.
2. The inductor current has reached the current limit.
3. Overvoltage at output occurs.

After a minimum dead time, the N−Channel synchronized switch will turn on and the inductor current will ramp down. If the inductor current ramps down to zero before the initiation of next clock cycle, the regulator runs at discontinuous conduction mode (DCM). Otherwise the regulator is at continuous conduction mode (CCM). The N−Channel switch will turn off when the clock cycle starts. The duty cycle is given by the ratio of output voltage to input voltage. The duty cycle is allowed to go to 100% to increase transient load response when going from light load to heavy load.

Error Amplifier and Slope Compensation

A fully internal compensated error amplifier is provided inside NCP1595. No external circuitry is needed to stabilize the device. The error amplifier provides an error signal to the PWM comparator by comparing the feedback voltage (800 mV) with internal voltage reference of 1.2 V.

Current mode converter can exhibit instability at duty cycles over 50%. A slope compensation circuit is provided inside NCP1595 to overcome the potential instability. Slope compensation consists of a ramp signal generated by the synchronization block and adding this to the inductor current signal. The summed signal is then applied to the PWM comparator.

Soft−Start and Current Limit

A soft start circuit is internally implemented to reduce the in−rush current during startup. This helps to reduce the output voltage overshoot.

The current limit is set to allow peak switch current in excess of 2 A. The intended output current of the system is 1.5 A. The ripple current is calculated to be approximately 350 mA with a 3.3 μH inductor. Therefore, the peak current at 1.5 A output will be approximately 1.7 A. A 2 A set point will allow for transient currents during load step. The current limit circuit is implemented as a cycle−by−cycle current limit. Each on−cycle is treated as a separate situation. Current limiting is implemented by monitoring the P−Channel switch current buildup during conduction with a current limit comparator. The output of the current limit comparator resets the PWM latch, immediately terminating the current cycle.

Over−Voltage Protection

Overvoltage occurs when the feedback voltage exceeds 5% of its regulated voltage. In this case, the P−Channel main switch will be reset and the N−Channel synchronized switch is turn on to sink current from the output voltage which helps to drop its feedback voltage back to the regulated voltage.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event when maximum junction temperature is exceeded. When activated, typically at 160°C, the shutdown signal will disable the P−Channel and N−Channel switch. The thermal shutdown circuit is designed with 30°C of hysteresis. This means that the switching will not start until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended as a substitute for proper heat sinking**. NCP1595 is contained in the thermally enhanced DFN package.

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connect from V_{OUT} to FB then to GND.

For internal compensation and noise immunity, the resistor from FB to GND should be in 10 k to 20 k ranges. The relationship between the output voltage and feedback resistor is given by:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 1)}$$

V_{OUT}: Output voltage
V_{FB}: Feedback Voltage
R1: Feedback resistor from V_{OUT} to FB.
R2: Feedback resistor from FB to GND.

Input Capacitor selection

In the PWM buck converter, the input current is pulsating current with switching noise. Therefore, a bypass input capacitor must choose for reduce the peak current drawn from the power supply. For NCP1595, low ESR ceramic capacitor of 10 μF should be used for most of cases. Also, the input capacitor should be placed as close as possible to the V_{CCA} pin for effective bypass the supply noise.

Inductor selection

The inductor parameters are including three items, which are DC resistance, inductor value and saturation current. Inductor DC resistance will effect the convector overall efficiency, low DC resistor value can provide a higher efficiency. Thus, inductor value are depend on the inductor ripple current, input voltage, output voltage, output current and operation frequency, the inductor value is given by:

$$\Delta_{IL} = \frac{V_{OUT}}{L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 2)}$$

ΔIL : peak to peak inductor ripple current
L: inductor value
FSW: switching frequency

After selected a suitable value of the inductor, it should be check out the inductor saturation current. The saturation current of the inductor should be higher than the maximum load plus the ripple current.

$$\Delta_{IL(MAX)} = \Delta_{IOUT(MAX)} + \frac{\Delta_{IL}}{2} \quad \text{(eq. 3)}$$

$\Delta_{IL(MAX)}$: Maximum inductor current
$\Delta_{IOUT(MAX)}$: Maximum output current

Output Capacitor selection

Output capacitor value is based on the target output ripple voltage. For NCP1595, the output capacitor is required a ceramic capacitors with low ESR value. Assume buck converter duty cycle is 50%. The output ripple voltage in PWM mode is given by:

$$\Delta_{VOUT} \approx \Delta_{IL} \times \left(\frac{1}{4 \times FSW \times C_{OUT}} + ESR\right) \quad \text{(eq. 4)}$$

In general, value of ceramic capacitor using 20 μF should be a good choice.

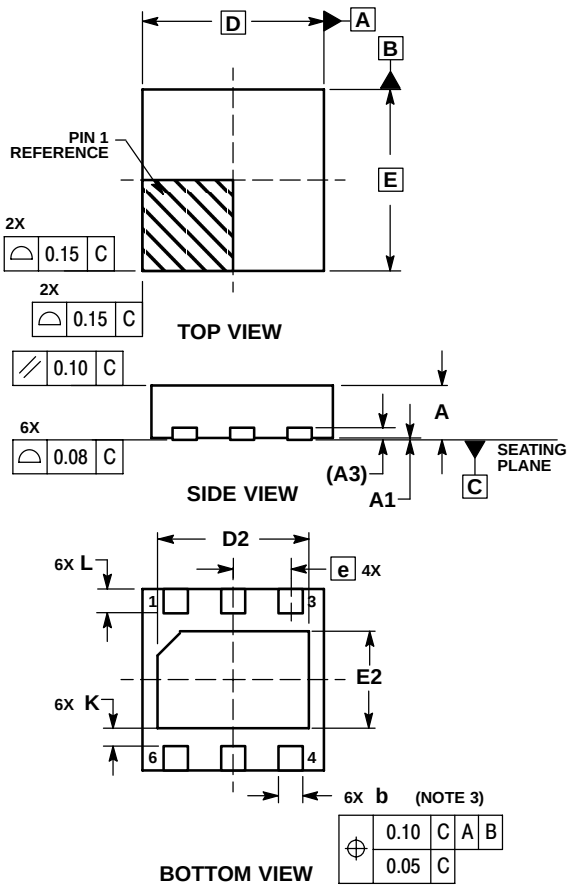
ORDERING INFORMATION

Device	Package	Shipping†
NCP1595MNR2G	DFN−6 (Pb−Free)	3000 / Tape & Reel
NCP1595AMNR2G	DFN−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

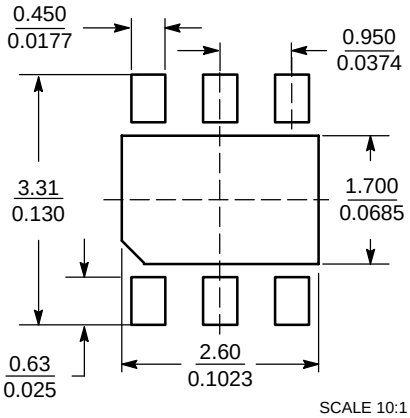
DFN6 3*3 MM, 0.95 PITCH
CASE 506AH−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.50	1.60	1.70
e		0.95 BSC	
K	0.21	−−−	−−−
L	0.30	0.40	0.50

SOLDERING FOOTPRINT*



SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative